# KS8993M / KS8993MI‡
# Integrated 3-Ports 10/100 Managed Switch with PHY

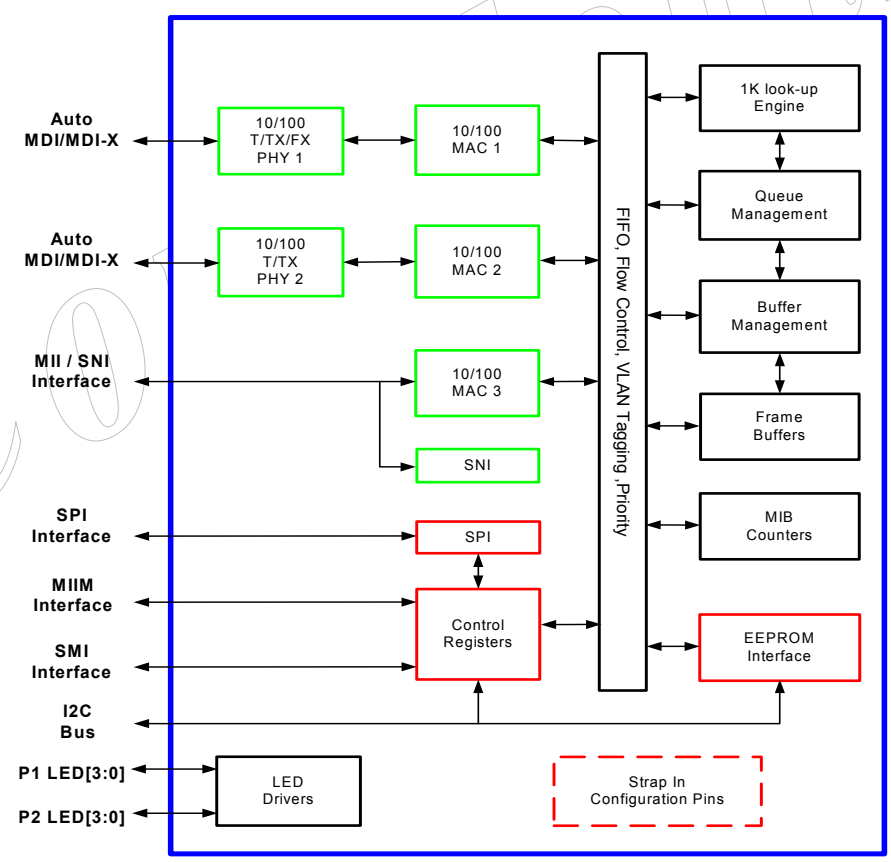
**Confidential Information** **Revision 1.02**

## Overview

The KS8993M, a highly integrated layer-2 managed switch, is designed for low port count, cost-sensitive 10/100 Mbps switch systems. It offers an extensive feature set that includes tag/port-based VLAN, QoS priority, management, MIB counters, MII/SNI interface and CPU control/data interfaces to effectively address both current and emerging Fast Ethernet applications.

The KS8993M contains two 10/100 transceivers with *patented mixed-signal low-power technology*, three MAC (Media Access Control) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

Both PHY units support 10BaseT and 100BaseTX. In addition, one of the PHY unit supports 100BaseFX.




**KS8993M**

**Note: ‡ KS8993MI will be available from Q1 2004**

## Feature Highlights

- **Proven 2nd generation of Integrated 3-Ports 10/100 Ethernet Switch with 3 MACs and 2 PHYs fully compliant to IEEE 802.3u Standard**
  - ✓ Non-blocking switch fabric assures fast packet delivery by utilizing an 1K MAC Address lookup table and a store-and-forward architecture
  - ✓ Full duplex IEEE 802.3x flow control (Pause) with force mode option
  - ✓ Half duplex back pressure flow control
  - ✓ Automatic MDI / MDI-X crossover with disable and enable option
  - ✓ 100BaseFX support on port 1
  - ✓ MII interface supports both MAC mode and PHY mode
  - ✓ 7-wire SNI support for legacy MAC
  - ✓ Comprehensive LED Indicator support for link, activity, full/half duplex and 10/100 speed
- **Comprehensive Configuration Register access**
  - ✓ Serial Management Interface (SMI) to all internal registers NEW
  - ✓ MII Management (MIIM) Interface to PHY registers
  - ✓ SPI and I2C Interface to all internal registers
  - ✓ I/0 Pins Strapping and EEPROM to program selective registers in unmanaged switch mode
  - ✓ Control registers configurable on the fly (port-priority, 802.1p/d/q, AN…)
- **QoS / CoS packets prioritization support**
  - ✓ per-port, 802.1p and DiffServ based
  - ✓ Re-mapping of 802.1p priority field per-port basis NEW
- **Advanced Switch Features**
  - ✓ IEEE 802.1q VLAN support for up to 16 groups (full-range of VLAN ID)

- ✓ VLAN ID tag/untag options, per-port basis
- ✓ IEEE 802.1p/q tag insertion or removal on a per port basis (egress)
- ✓ Programmable Rate Limiting from 0 to 100 Mbps at the ingress & egress port, rate options for high & low priority, per port basis
- ✓ Broadcast storm protection with % control (global & per-port basis)
- ✓ IEEE 802.1d Spanning Tree Protocol support
- ✓ Upstream Special Tagging Mode to inform the processor which ingress port a packet is received on
- ✓ IGMP v1/v2 Snooping support for multicast packet filtering
- ✓ Double Tagging support **NEW**

- **Switch Management Features:**
  - ✓ Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII
  - ✓ MIB (Management Information Base) counters for fully compliant statistics gathering, 34 MIB counters per port
  - ✓ Loop back modes for remote diagnostic of failure
- **Low Power Dissipation: < 0.8 Watts (includes PHY transmit drivers)**
  - ✓ Full-chip hardware power-down (register configuration not saved)
  - ✓ Per-port based software power-save on PHY (idle link detection, register configuration preserved)
  - ✓ 0.18um CMOS technology
  - ✓ Voltages: Core 1.8V

    I/O and Transceiver 3.3V or 2.5V
- **Industrial Temperature (available from Q1 2004)**
- **128-pins PQFP Package**

# Applications

- **Universal Solutions**
  - Broadband Gateway / Firewall / VPN
  - Integrated DSL or Cable Modem Multi-port Router
  - Wireless LAN Access Point + Gateway
  - Residential & Enterprise VoIP Gateway / Phone
  - Set-Top / Game Box
  - Home Networking Expansion
  - Standalone 10/100 Switch
  - FTTx Customer Premise Equipment
  - Fiber Broadband Gateway
- **Upgradeable Solutions**[1]
  - Unmanaged Switch with future option to migrate to a Managed Solution
  - Single PHY alternative with future expansion option for two ports
- **Industrial Solutions**
  - Applications requiring port redundancy and port monitoring
  - Sensor Devices in Redundant Ring Topology

Note: [1] Save the cost and time of PCB re-spin

# Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.00 | 5/14/03 | Initial Release |
| 1.01 | 5/28/03 | Added KS8993MI availability in Q4 2003 |
| 1.02 | 12/8/03 | Changed VDDIO, VDDATX and VDDARX supply voltages from 3.3V to (3.3V or 2.5V).<br>Changed [PS1,PS0] = [1,1] setting from Reserved to SMI mode.<br>Changed Special Tagging Mode to Upstream Special Tagging Mode (Switch Port 3 to Processor support only).<br>Updated recommended magnetic manufacturer list.<br>Added 25 MHz crystal/oscillator clock's ppm spec. in pin description.<br>Updated I2C Slave Serial Bus Configuration section.<br>Updated KS8993MI availability to from Q1 2004. |

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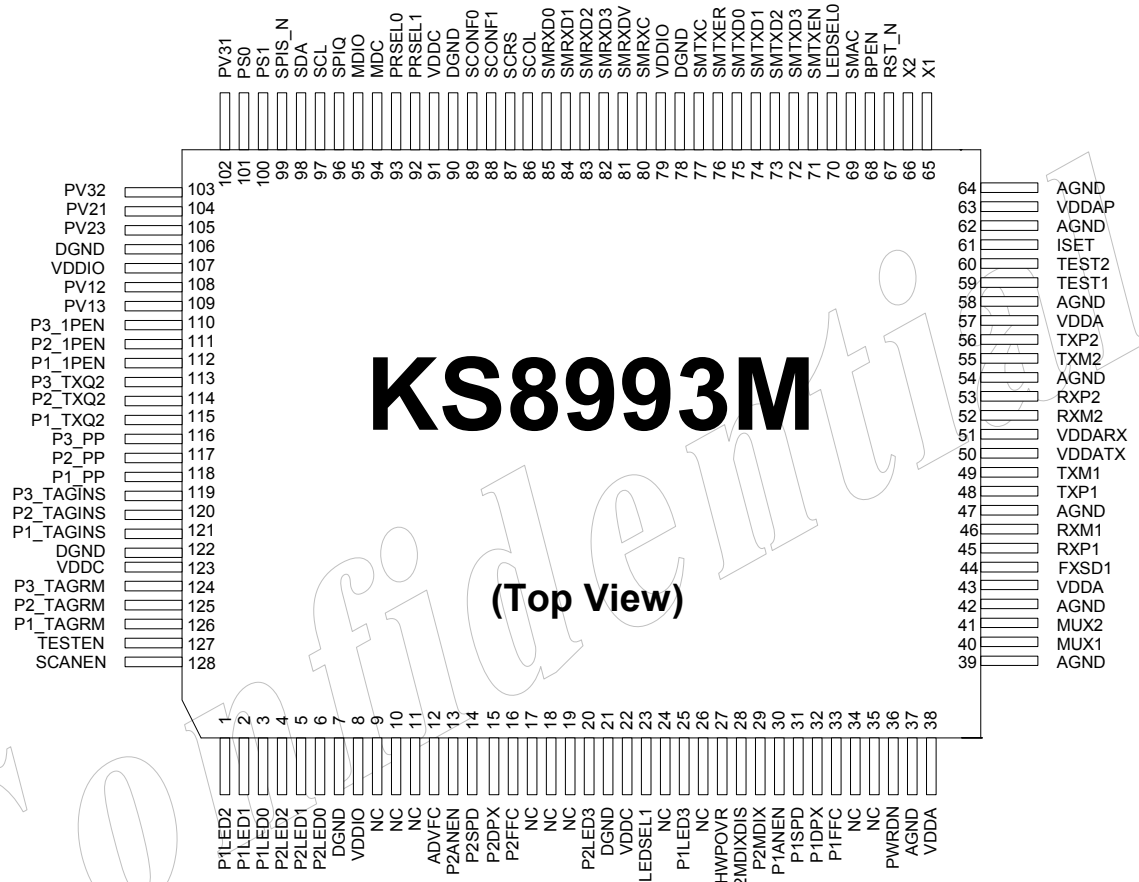
# 1.0 Signal Description

## 1.1 KS8993M Pin Diagram



## 1.2 KS8993M Pin Description and I/O Assignment

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>P1LED2</td><td>Ipu / O</td><td rowspan="3">Port 1 LED Indicators, defined as below:<br><br>
<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th><th>[0, 1]</th></tr>
<tr><td>P1LED3</td><td>------</td><td>------</td></tr>
<tr><td>P1LED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr>
<tr><td>P1LED1</td><td>FULL_DPX/COL</td><td>10LINK/ACT</td></tr>
<tr><td>P1LED0</td><td>SPEED</td><td>FULL_DPX</td></tr>
</table>
<br>
<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>P1LED3</td><td>ACT</td><td>------</td></tr>
<tr><td>P1LED2</td><td>LINK</td><td>------</td></tr>
<tr><td>P1LED1</td><td>FULL_DPX/COL</td><td>------</td></tr>
<tr><td>P1LED0</td><td>SPEED</td><td>------</td></tr>
</table>
<br>
Notes:<br>
LEDSEL0 is external strap-in pin #70.<br>
LEDSEL1 is external strap-in pin #23.<br>
P1LED3 is pin #25.<br>
During reset, P1LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>2</td><td>P1LED1</td><td>Ipu / O</td></tr>
<tr><td>3</td><td>P1LED0</td><td>Ipu / O</td></tr>
<tr><td>4</td><td>P2LED2</td><td>Ipu / O</td><td rowspan="3">Port 2 LED Indicators, defined as below:<br><br>
<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th><th>[0, 1]</th></tr>
<tr><td>P2LED3</td><td>------</td><td>------</td></tr>
<tr><td>P2LED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr>
<tr><td>P2LED1</td><td>FULL_DPX/COL</td><td>10LINK/ACT</td></tr>
<tr><td>P2LED0</td><td>SPEED</td><td>FULL_DPX</td></tr>
</table>
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<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>P2LED3</td><td>ACT</td><td>------</td></tr>
<tr><td>P2LED2</td><td>LINK</td><td>------</td></tr>
<tr><td>P2LED1</td><td>FULL_DPX/COL</td><td>------</td></tr>
<tr><td>P2LED0</td><td>SPEED</td><td>------</td></tr>
</table>
<br>
Notes:<br>
LEDSEL0 is external strap-in pin #70.<br>
LEDSEL1 is external strap-in pin #23.<br>
P2LED3 is pin #20.<br>
During reset, P2LED[2:0] are inputs for internal testing.</td></tr>
<tr><td>5</td><td>P2LED1</td><td>Ipu / O</td></tr>
<tr><td>6</td><td>P2LED0</td><td>Ipu / O</td></tr>
<tr><td>7</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>8</td><td>VDDIO</td><td>Pwr</td><td>3.3V or 2.5V digital VDD</td></tr>
<tr><td>9</td><td>NC</td><td>Ipd</td><td>NC</td></tr>
</table>

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 10 | NC | Ipd | NC |
| 11 | NC | Ipu | NC |
| 12 | ADVFC | Ipu | 1 = advertise the switch's flow control capability via auto negotiation.<br>0 = will not advertise the switch's flow control capability via auto negotiation. |
| 13 | P2ANEN | Ipu | 1 = enable auto negotiation on port 2<br>0 = disable auto negotiation on port 2 |
| 14 | P2SPD | Ipd | 1 = Force port 2 to 100BT if P2ANEN = 0.<br>0 = Force port 2 to 10BT if P2ANEN = 0. |
| 15 | P2DPX | Ipd | 1 = port 2 default to full duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in full duplex mode if P2ANEN = 0.<br>0 = port 2 default to half duplex mode if P2ANEN = 1 and auto negotiation fails. Force port 2 in half duplex mode if P2ANEN = 0. |
| 16 | P2FFC | Ipd | 1 = always enable (force) port 2 flow control feature<br>0 = port 2 flow control feature enable is determined by auto negotiation result. |
| 17 | NC | Opu | NC |
| 18 | NC | Ipd | NC |
| 19 | NC | Ipd | NC |
| 20 | P2LED3 | Opd | Port 2 LED Indicator<br>Note: Internal pull down is weak; it will not turn ON the LED.<br><br>*See description in pin# (4).* |
| 21 | DGND | Gnd | Digital ground |
| 22 | VDDC | Pwr | 1.8V digital core VDD |
| 23 | LEDSEL1 | Ipd | LED display mode select<br><br>*See description in pin# (1,4).* |
| 24 | NC | O | NC |
| 25 | P1LED3 | O | Port 1 LED Indicator<br><br>*See description in pin# (1).* |
| 26 | NC | O | NC |
| 27 | HWPOVR | Ipd | Hardware Pin Overwrite<br>0 = Disable. All strap-in pins configurations are overwritten by the EEPROM configuration data<br>1 = Enable. All strap-in pins configurations are overwritten by the EEPROM configuration data, except for register 0x2C bits [7:5], (port 2: auto-negotiation enable, force speed, force duplex). |
| 28 | P2MDIXDIS | Ipd | Port 2 auto MDI/MDI-X<br>PD (default) = enable<br>PU = disable |
| 29 | P2MDIX | Ipd | Port 2 MDI/MDI-X setting when auto MDI/MDI-X is disabled<br>PD (default) = MDI<br>PU = MDI-X |

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 30 | P1ANEN | Ipu | 1 = enable auto negotiation on port 1<br>0 = disable auto negotiation on port 1 |
| 31 | P1SPD | Ipd | 1 = Force port 1 to 100BT if P1ANEN = 0<br>0 = Force port 1 to 10BT if P1ANEN = 0 |
| 32 | P1DPX | Ipd | 1 = port 1 default to full duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in full duplex mode if P1ANEN = 0.<br>0 = port 1 default to half duplex mode if P1ANEN = 1 and auto negotiation fails. Force port 1 in half duplex mode if P1ANEN = 0. |
| 33 | P1FFC | Ipd | 1 = always enable (force) port 1 flow control feature<br>0 = port 1 flow control feature enable is determined by auto negotiation result. |
| 34 | NC | Ipd | NC |
| 35 | NC | Ipd | NC |
| 36 | PWRDN | Ipu | Chip power down input (active low) |
| 37 | AGND | Gnd | Analog ground |
| 38 | VDDA | Pwr | 1.8V analog VDD |
| 39 | AGND | Gnd | Analog ground |
| 40 | MUX1 | I | Factory test pin - float for normal operation |
| 41 | MUX2 | I | Factory test pin - float for normal operation |
| 42 | AGND | Gnd | Analog ground |
| 43 | VDDA | Pwr | 1.8V analog VDD |
| 44 | FXSD1 | I | Fiber Signal Detect / Factory test pin |
| 45 | RXP1 | I / O | Physical receive or transmit signal (+ differential) |
| 46 | RXM1 | I / O | Physical receive or transmit signal (– differential) |
| 47 | AGND | Gnd | Analog ground |
| 48 | TXP1 | I / O | Physical transmit or receive signal (+ differential) |
| 49 | TXM1 | I / O | Physical transmit or receive signal (– differential) |
| 50 | VDDATX | Pwr | 3.3V or 2.5V analog VDD |
| 51 | VDDARX | Pwr | 3.3V or 2.5V analog VDD |
| 52 | RXM2 | I / O | Physical receive or transmit signal (– differential) |
| 53 | RXP2 | I / O | Physical receive or transmit signal (+ differential) |
| 54 | AGND | Gnd | Analog ground |
| 55 | TXM2 | I / O | Physical transmit or receive signal (– differential) |
| 56 | TXP2 | I / O | Physical transmit or receive signal (+ differential) |
| 57 | VDDA | Pwr | 1.8 analog VDD |
| 58 | AGND | Gnd | Analog ground |
| 59 | TEST1 | I | Factory test pin - float for normal operation |
| 60 | TEST2 | Ipu | Factory test pin - float or pull up for normal operation |
| 61 | ISET | O | Set physical transmit output current.<br>Pull down this pin with a 3.01K 1% resistor to ground. |
| 62 | AGND | Gnd | Analog ground |
| 63 | VDDAP | Pwr | 1.8V analog VDD for PLL |
| 64 | AGND | Gnd | Analog ground |
| 65 | X1 | I | 25 MHz crystal/oscillator clock connections<br>Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect.<br><br>**Note:** Clock is +/- 100ppm for both crystal and oscillator. |
| 66 | X2 | O | |

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 67 | RST_N | Ipu | Hardware reset pin (active low) |
| 68 | BPEN | Ipd | Half Duplex Backpressure<br>1 = enable<br>0 = disable |
| 69 | SMAC | Ipd | Special Mac Mode<br>In this mode, the switch will do faster backoffs than normal.<br>1 = enable<br>0 = disable |
| 70 | LEDSEL0 | Ipd | LED display mode select<br><br>*See description in pin# (1,4).* |
| 71 | SMTXEN | Ipd | Switch MII transmit enable |
| 72 | SMTXD3 | Ipd | Switch MII transmit data bit 3 |
| 73 | SMTXD2 | Ipd | Switch MII transmit data bit 2 |
| 74 | SMTXD1 | Ipd | Switch MII transmit data bit 1 |
| 75 | SMTXD0 | Ipd | Switch MII transmit data bit 0 |
| 76 | SMTXER | Ipd | Switch MII transmit error |
| 77 | SMTXC | Ipd / O | Switch MII transmit clock.<br>Output in PHY MII mode<br>Input in MAC MII mode |
| 78 | DGND | Gnd | Digital ground |
| 79 | VDDIO | Pwr | 3.3V or 2.5V digital VDD |
| 80 | SMRXC | Ipd / O | Switch MII receive clock.<br>Output in PHY MII mode<br>Input in MAC MII mode |
| 81 | SMRXDV | O | Switch MII receive data valid |
| 82 | SMRXD3 | Ipd / O | Switch MII receive data bit 3<br><br>Strap option: Switch MII full duplex flow control<br>PD (default) = disable<br>PU = enable |
| 83 | SMRXD2 | Ipd / O | Switch MII receive bit 2<br><br>Strap option: Switch MII is in<br>PD (default) = full duplex mode<br>PU = half duplex mode |
| 84 | SMRXD1 | Ipd / O | Switch MII receive bit 1<br><br>Strap option: Switch MII is in<br>PD (default) = 100Mbps mode;<br>PU = 10Mbps mode |
| 85 | SMRXD0 | Ipd / O | Switch MII receive bit 0<br><br>Strap option: Switch will accept packet size up to<br>PD (default) = 1536 bytes (inclusive);<br>PU = 1522 bytes (tagged), 1518 bytes (untagged) |
| 86 | SCOL | Ipd / O | Switch MII collision detect |
| 87 | SCRS | Ipd / O | Switch MII carrier sense |

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>88</td><td>SCONF1</td><td>Ipd</td><td rowspan="2">Switch MII interface configuration<br><br><table><tr><td>(SCONF1, SCONF0)</td><td>Description</td></tr><tr><td>(0,0)</td><td>disable, outputs tri-stated</td></tr><tr><td>(0,1)</td><td>PHY mode MII</td></tr><tr><td>(1,0)</td><td>MAC mode MII</td></tr><tr><td>(1,1)</td><td>PHY mode SNI</td></tr></table></td></tr>
<tr><td>89</td><td>SCONF0</td><td>Ipd</td></tr>
<tr><td>90</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>91</td><td>VDDC</td><td>Pwr</td><td>1.8V digital VDD</td></tr>
<tr><td>92</td><td>PRSEL1</td><td>Ipd</td><td rowspan="2">Priority Select Select queue servicing if using split queues. Use the table below to select the desired servicing. Note that this selection effects all split transmit queue ports in the same way.<br><br><table><tr><td>(PRSEL1, PRSEL0)</td><td>Description</td></tr><tr><td>(0,0)</td><td>Transmit all high priority before low priority</td></tr><tr><td>(0,1)</td><td>Transmit high priority and low priority at 10:1 ratio.</td></tr><tr><td>(1,0)</td><td>Transmit high priority and low priority at 5:1 ratio.</td></tr><tr><td>(1,1)</td><td>Transmit high priority and low priority at 2:1 ratio.</td></tr></table></td></tr>
<tr><td>93</td><td>PRSEL0</td><td>Ipd</td></tr>
<tr><td>94</td><td>MDC</td><td>Ipu</td><td>MII Management interface: clock input</td></tr>
<tr><td>95</td><td>MDIO</td><td>Ipu / O</td><td>MII Management interface: data input/output</td></tr>
<tr><td>96</td><td>SPIQ</td><td>Opu</td><td>SPI slave mode: serial data output<br><br>See description in pin# (100, 101)</td></tr>
<tr><td>97</td><td>SCL</td><td>Ipu / O</td><td>SPI slave mode / I2C slave mode: clock input<br>I2C master mode: clock output<br><br>See description in pin# (100, 101)</td></tr>
<tr><td>98</td><td>SDA</td><td>Ipu / O</td><td>SPI slave mode: serial data input<br>I2C master/slave mode: serial data input/output<br><br>See description in pin# (100, 101)</td></tr>
<tr><td>99</td><td>SPIS_N</td><td>Ipu</td><td>SPI slave mode: chip select (active low)<br><br>When SPIS_N is high, the KS8993M is deselected and SPIQ is held in high impedance state.<br><br>A high-to-low transition is used to initiate SPI data transfer.<br><br>see description in pin# (100, 101)</td></tr>
</table>

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>100</td><td>PS1</td><td>Ipd</td><td rowspan="2">Serial bus configuration pins to select mode of access to KS8993M internal registers.<br><br>[PS1, PS0] = [0, 0] --- I2C master (EEPROM) mode<br>(If EEPROM is not detected, the power up default values of the KS8993M internal registers will be used)<br><table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>O</td><td>I2C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I2C data I/O</td></tr><tr><td>SPIS_N</td><td>Ipu</td><td>Not used</td></tr></table><br>[PS1, PS0] = [0, 1] --- I2C slave mode<br>The external I2C master will drive the SCL clock.<br>The KS8993M device addresses are:<br>1011_1111 <read><br>1011_1110 <write><br><table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>Not used (tri-stated)</td></tr><tr><td>SCL</td><td>I</td><td>I2C clock</td></tr><tr><td>SDA</td><td>I/O</td><td>I2C data I/O</td></tr><tr><td>SPIS_N</td><td>Ipu</td><td>Not used</td></tr></table><br>[PS1, PS0] = [1, 0] --- SPI slave mode<br><table><tr><th>Interface Signals</th><th>Type</th><th>Description</th></tr><tr><td>SPIQ</td><td>O</td><td>SPI Data Out</td></tr><tr><td>SCL</td><td>I</td><td>SPI clock</td></tr><tr><td>SDA</td><td>I</td><td>SPI Data In</td></tr><tr><td>SPIS_N</td><td>Ipu</td><td>SPI chip select</td></tr></table><br>[PS1, PS0] = [1, 1] --- SMI mode<br>In this mode, the KS8993M provides access to all its internal 8 bit registers thru its MDC and MDIO pins.<br><br><u>Note</u><br>When (PS1, PS0) ≠ (1,1), the KS8993M provides access to its 16 bit MIIM registers thru its MDC and MDIO pins.</td></tr>
<tr><td>101</td><td>PS0</td><td>Ipd</td></tr>
<tr><td>102</td><td>PV31</td><td>Ipu</td><td rowspan="2">Port 3 port-based VLAN mask bits - use to select which ports may transmit packets received on port 3<br><br>PV31 = 1, port 1 may transmit packets received on port 3<br>PV31 = 0, port 1 will not transmit any packets received on port 3<br><br>PV32 = 1, port 2 may transmit packets received on port 3<br>PV32 = 0, port 2 will not transmit any packets received on port 3</td></tr>
<tr><td>103</td><td>PV32</td><td>Ipu</td></tr>
<tr><td>104</td><td>PV21</td><td>Ipu</td><td rowspan="2">Port 2 port-based VLAN mask bits - use to select which ports may transmit packets received on port 2<br><br>PV21 = 1, port 1 may transmit packets received on port 2<br>PV21 = 0, port 1 will not transmit any packets received on port 2<br><br>PV23 = 1, port 3 may transmit packets received on port 2<br>PV23 = 0, port 3 will not transmit any packets received on port 2</td></tr>
<tr><td>105</td><td>PV23</td><td>Ipu</td></tr>
<tr><td>106</td><td>DGND</td><td>Gnd</td><td>Digital ground</td></tr>
<tr><td>107</td><td>VDDIO</td><td>Pwr</td><td>3.3V or 2.5V digital VDD</td></tr>
</table>

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 108 | PV12 | Ipu | **Port 1 port-based VLAN mask bits** - use to select which ports may transmit packets received on port 1<br><br>PV12 = 1, port 2 may transmit packets received on port 1<br>PV12 = 0, port 2 will not transmit any packets received on port 1<br><br>PV13 = 1, port 3 may transmit packets received on port 1<br>PV13 = 0, port 3 will not transmit any packets received on port 1 |
| 109 | PV13 | Ipu | |
| 110 | P3_1PEN | Ipd | **Enable 802.1p priority classification on port 3 ingress**<br>1 = enable<br>0 = disable<br>Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P3_PP pin. |
| 111 | P2_1PEN | Ipd | **Enable 802.1p priority classification on port 2 ingress**<br>1 = enable<br>0 = disable<br>Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P2_PP pin. |
| 112 | P1_1PEN | Ipd | **Enable 802.1p priority classification on port 1 ingress**<br>1 = enable<br>0 = disable<br>Enable is from the receive perspective. If 802.1p processing is disabled or there is no tag, priority is determined by the P1_PP pin. |
| 113 | P3_TXQ2 | Ipd | **Select transmit queue split on port 3**<br>1 = split<br>0 = no split<br>The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 3 is set by P3_TXQ2. |
| 114 | P2_TXQ2 | Ipd | **Select transmit queue split on port 2**<br>1 = split<br>0 = no split<br>The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 2 is set by P2_TXQ2. |
| 115 | P1_TXQ2 | Ipd | **Select transmit queue split on port 1**<br>1 = split<br>0 = no split<br>The split sets up high and low priority queues. Packet priority classification is done on ingress ports, via port-based, 802.1p or TOS based scheme. The priority enabled queuing on port 1 is set by P1_TXQ2. |
| 116 | P3_PP | Ipd | **Select port-based priority on port 3 ingress**<br>1 = high<br>0 = low <default><br>802.1p and Diffserv, if applicable, will take precedence. |

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 117 | P2_PP | Ipd | **Select port-based priority on port 2 ingress**<br>1 = high<br>0 = low <default><br>802.1p and Diffserv, if applicable, will take precedence. |
| 118 | P1_PP | Ipd | **Select port-based priority on port 1 ingress**<br>1 = high<br>0 = low <default><br>802.1p and Diffserv, if applicable, will take precedence. |
| 119 | P3_TAGINS | Ipd | **Enable tag insertion on port 3 egress**<br>1 = enable<br>0 = disable<br>All packets transmitted from port 3 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag. |
| 120 | P2_TAGINS | Ipd | **Enable tag insertion on port 2 egress**<br>1 = enable<br>0 = disable<br>All packets transmitted from port 2 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag. |
| 121 | P1_TAGINS | Ipd | **Enable tag insertion on port 1 egress**<br>1 = enable<br>0 = disable<br>All packets transmitted from port 1 will have 802.1Q tag. Packets received with tag will be sent out intact. Packets received without tag will be tagged with ingress port's default tag. |
| 122 | DGND | Gnd | Digital ground |
| 123 | VDDC | Pwr | 1.8V digital VDD |
| 124 | P3_TAGRM | Ipd | **Enable tag removal on port 3 egress**<br>1 = enable<br>0 = disable<br>All packets transmitted from port 3 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact. |
| 125 | P2_TAGRM | Ipd | **Enable tag removal on port 2 egress**<br>1 = enable<br>0 = disable<br>All packets transmitted from port 2 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact. |
| 126 | P1_TAGRM | Ipd | **Enable tag removal on port 1 egress**<br>1 = enable<br>0 = disable<br>All packets transmitted from port 1 will not have 802.1Q tag. Packets received with tag will be modified by removing 802.1Q tag. Packets received without tag will be sent out intact. |

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 127 | TESTEN | Ipd | Scan Test Enable<br>For normal operation, pull down this pin to ground |
| 128 | SCANEN | Ipd | Scan Test Scan Mux Enable<br>For normal operation, pull down this pin to ground |

## Notes:

Pwr = power supply;
Gnd = ground;
I = input;
O = output;
I / O = bi-directional;
Ipu = input w/ internal pull-up;
Ipd = input w/ internal pull-down;
Ipd / O = input w/ internal pull-down during reset, output pin otherwise;
Ipu / O = input w/ internal pull-up during reset, output pin otherwise;
Opu = Output with internal pull-up;
Opd = Output with internal pull-down;
PU = strap-in pin pull-up;
PD = strap-in pin pull-down;
1 = strap-in pin pull-up;
0 = strap-in pin pull-down;
NC = No Connect

# 2.0 Functional Overview

The KS8993M contains two 10/100 physical layer transceivers and three MAC (Media Access Control) units with an integrated layer 2 managed switch.

The KS8993M has the flexibility to reside in either a managed or unmanaged design. In a managed design, the host processor has complete control of the KS8993M via the SMI interface, MIIM interface, SPI bus, or I2C bus. An unmanaged design is achieved through I/O strapping and/or EEPROM programming at system reset time.

On the media side, the KS8993M supports IEEE 802.3 10BaseT and 100BaseTX on both PHY ports, and 100BaseFX on PHY port 1. The KS8993M can be used as a media converter.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

# 3.0 Functional Overview: Physical Layer Transceiver

## 3.1 100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 3.01 KΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BaseT output is also incorporated into the 100BaseTX transmitter.

## 3.2 100BaseTX Receive

The 100BaseTX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial to parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation

based on comparisons of incoming signal strength against some known cable characteristics, then it tunes itself for optimization. This is an ongoing process and can self adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

### 3.3 PLL Clock Synthesizer

The KS8993M generates 125 MHz, 31.25 MHz, 25 MHz and 10 MHz clocks for system timing. Internal clocks are generated from an external 25 MHz crystal or oscillator.

### 3.4 Scrambler/De-scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

### 3.5 100BaseFX operation

100BaseFX operation is very similar to 100BaseTX operation with the differences being that the scrambler / de-scrambler and MLT3 encoder / decoder are bypassed on transmission and reception. In 100BaseFX mode, the auto negotiation feature is bypassed since there is no standard that supports fiber auto negotiation. The auto-MDI/MDI-X feature is also disabled.

### 3.6 100BaseFX Signal Detection

In Fiber operation, the KS8993M's FXSD1 (fiber signal detect) input pin is usually connected to the fiber transceiver's SD (signal detect) output pin. 100BaseFX mode is activated when the FXSD1 input pin is greater than 1V. When FXSD1 is between 1V and 1.8V, no fiber signal is detected and a Far End Fault is generated. When FXSD1 is over 2.2V, the fiber signal is detected.

Alternatively, the designer may choose not to implement the Far End Fault feature. In this case, the FXSD1 input pin is tied high to force 100BaseFX mode.

100BaseFX signal detection is summarized in the following table:

**Table 1: FX & TX Mode Selection**

| FXSD1 (input pin) | Mode |
|---|---|
| Less than 0.2V | TX mode |
| Greater than 1V, but less than 1.8V | FX mode<br>No signal detected;<br>Far End Fault generated |
| Greater than 2.2V | FX mode<br>Signal detected |

To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver's SD output voltage swing to match the KS8993M's FXSD1 input voltage threshold.

### 3.7 100BaseFX Far End Fault (FEF)

A Far End fault (FEF) occurs when the signal detection is logically false on the receive side of the fiber transceiver. The KS8993M detects a FEF when its FXSD1 input is between 1.0V and 1.8V. When a FEF occurs, the transmission side signals the other end of the link by sending 84 1's followed by a zero in the idle period between frames.

Upon receiving a FEF, the LINK will go down (even when the fiber signal is detected) to indicate a fault condition. The transmitting side is not affected when a FEF is received, and will continue to send out its normal transmit pattern from the MAC.

By default, FEF is disabled. The FEF feature can be enabled through register setting.

### 3.8 10BaseT Transmit

The output 10BaseT driver is incorporated into the 100BaseT driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

### 3.9 10BaseT Receive

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8993M decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

### 3.10 Power Management

The KS8993M features a per-port power down mode. To save power, the user can power down ports that are not in use by setting the port control registers, or MII control registers. In addition, there is a full chip power down mode. When activated, the entire chip will be shut down.

### 3.11 MDI / MDI-X auto crossover

The KS8993M supports MDI / MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the KS8993M device. This feature can be extremely useful when end users are unaware of cable types and can also save on an additional uplink configuration connection. The auto crossover feature can be disabled through the port control registers.

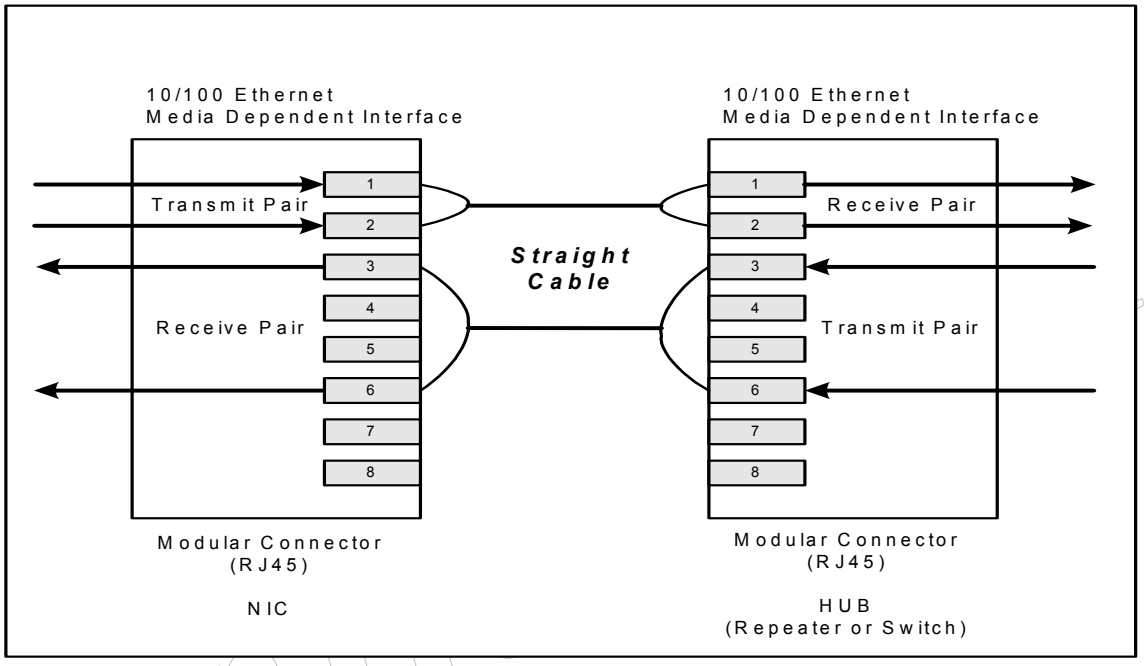
Based on the IEEE 802.3 standard, the MDI and MDI-X definitions are as follows:

**Table 2: MDI / MDI-X Pin Definition**

| MDI | | MDI-X | |
|---|---|---|---|
| **RJ45 pins** | **Signals** | **RJ45 pins** | **Signals** |
| 1 | TD+ | 1 | RD+ |
| 2 | TD- | 2 | RD- |
| 3 | RD+ | 3 | TD+ |
| 6 | RD- | 6 | TD- |

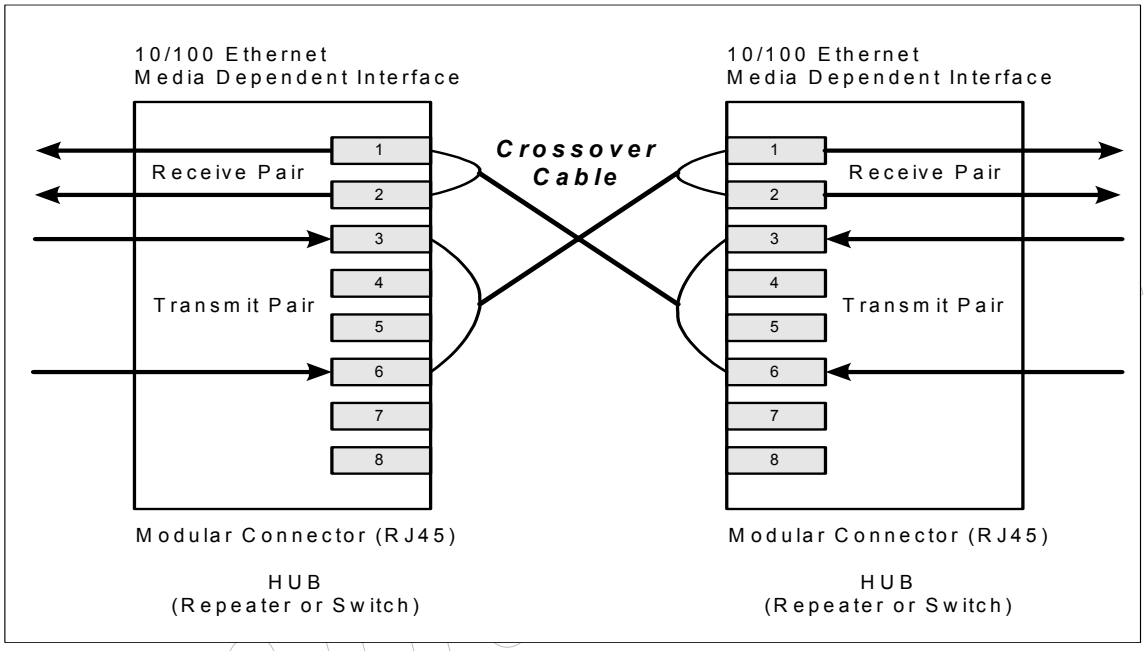
A “Straight Cable” connects a MDI device to a MDI-X device, or a MDI-X device to a MDI device. The following diagram depicts a typical “Straight Cable” connection between a NIC card (MDI) and a switch, or hub (MDI-X).

**Figure 1: Typical Straight Cable Connection**



A “Crossover Cable” connects a MDI device to another MDI device, or a MDI-X device to another MDI-X device. The following diagram depicts a typical “Crossover Cable” connection between two switches, or hubs (two MDI-X devices).

**Figure 2: Typical Crossover Cable Connection**




## 3.12 Auto Negotiation

The KS8993M conforms to the auto negotiation protocol as described by the 802.3 committee. Auto negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KS8993M is forced to bypass auto negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link set up is depicted in the following flow diagram.

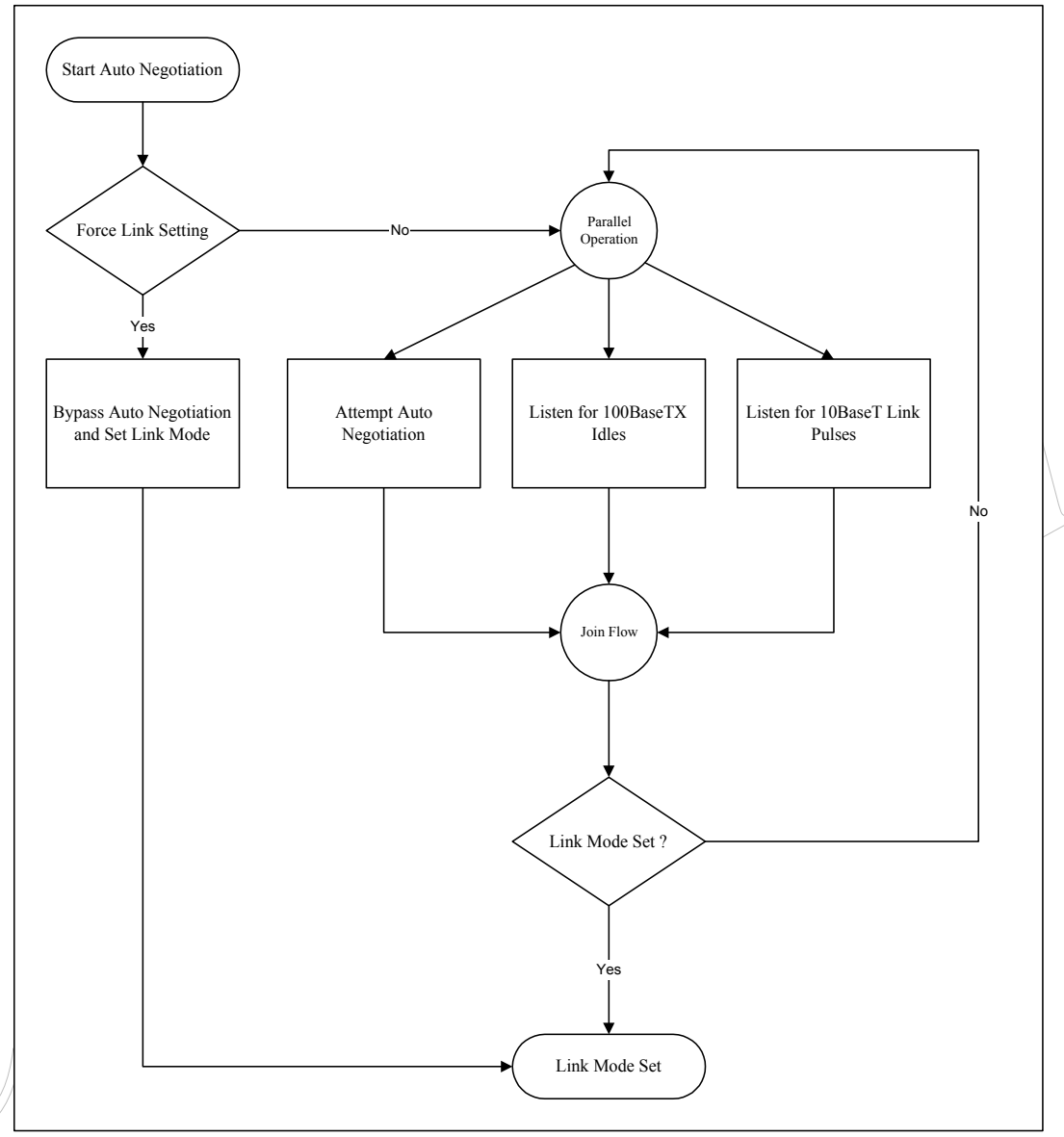



**Figure 3: Auto Negotiation and Parallel Operation**

# 4.0 Functional Overview: MAC and Switch

## 4.1 Address Look Up

The internal look up table stores MAC addresses and their associated information. It contains a 1K uni-cast address table plus switching information. The KS8993M is guaranteed to learn 1K addresses and distinguishes itself from hash-based look up

tables, which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

### 4.2 Learning

The internal look up engine will update its table with a new entry if the following conditions are met:

(1). The received packet's Source Address does not exist in the look up table.
(2). The received packet is good; the packet has no receiving errors, and is of legal length.

The look up engine will insert the qualified Source Address into the table, along with the port number and time stamp. If the table is full, the last entry of the table will be deleted to make room for the new entry.

### 4.3 Migration

The internal look up engine also monitors whether a station has moved. If so, it will update the table accordingly. Migration happens when the following conditions are met:

(1). The received packet's Source Address is in the table but the associated source port information is different.
(2). The received packet is good; the packet has no receiving errors, and is of legal length.

The look up engine will update the existing record in the table with the new source port information.

### 4.4 Aging

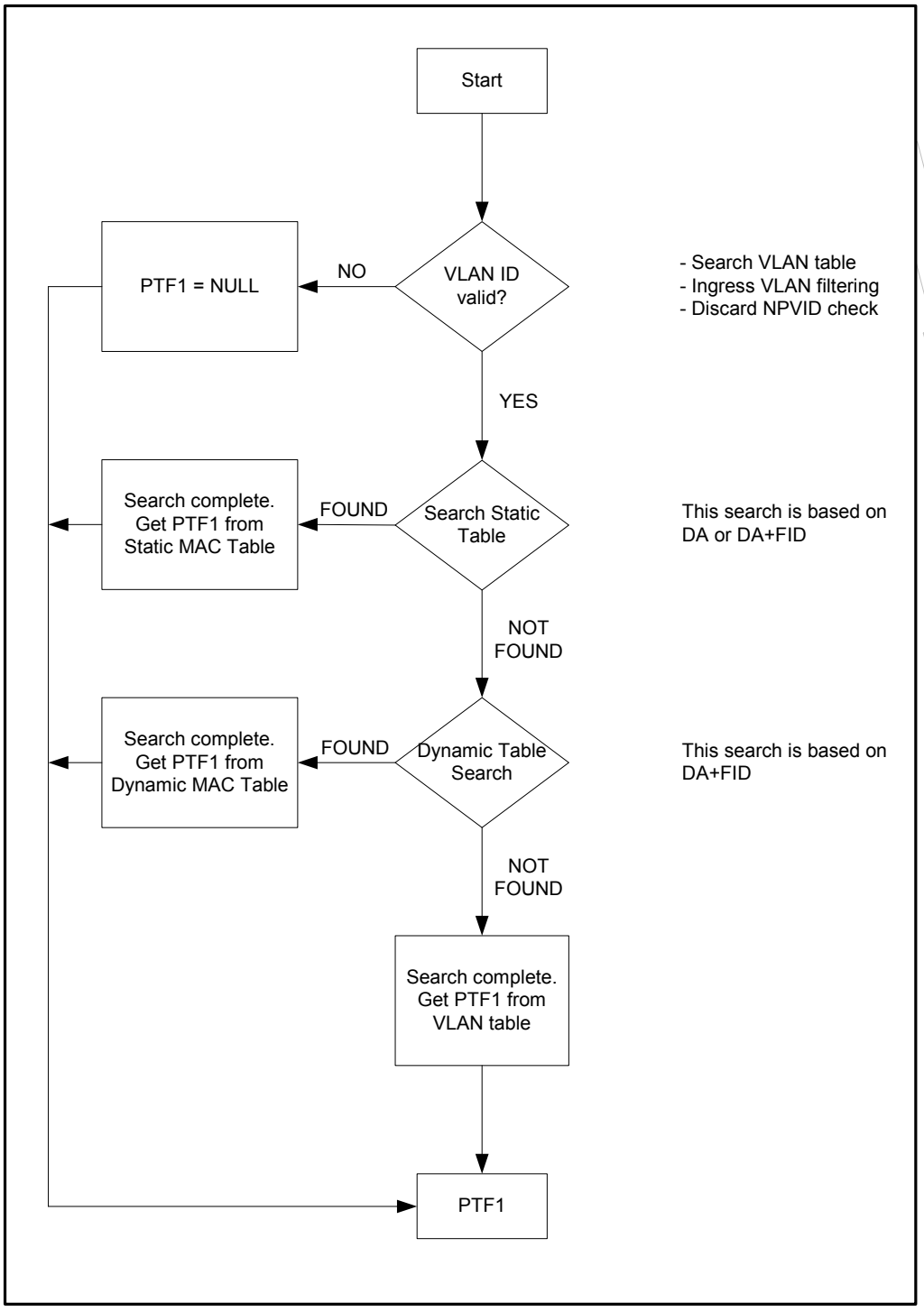
The look up engine will update the time stamp information of a record whenever the corresponding Source Address appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look up engine will remove the record from the table. The look up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 $\pm$ 75 seconds. This feature can be enabled or disabled through Global Register 3 (0x03).

### 4.5 Forwarding

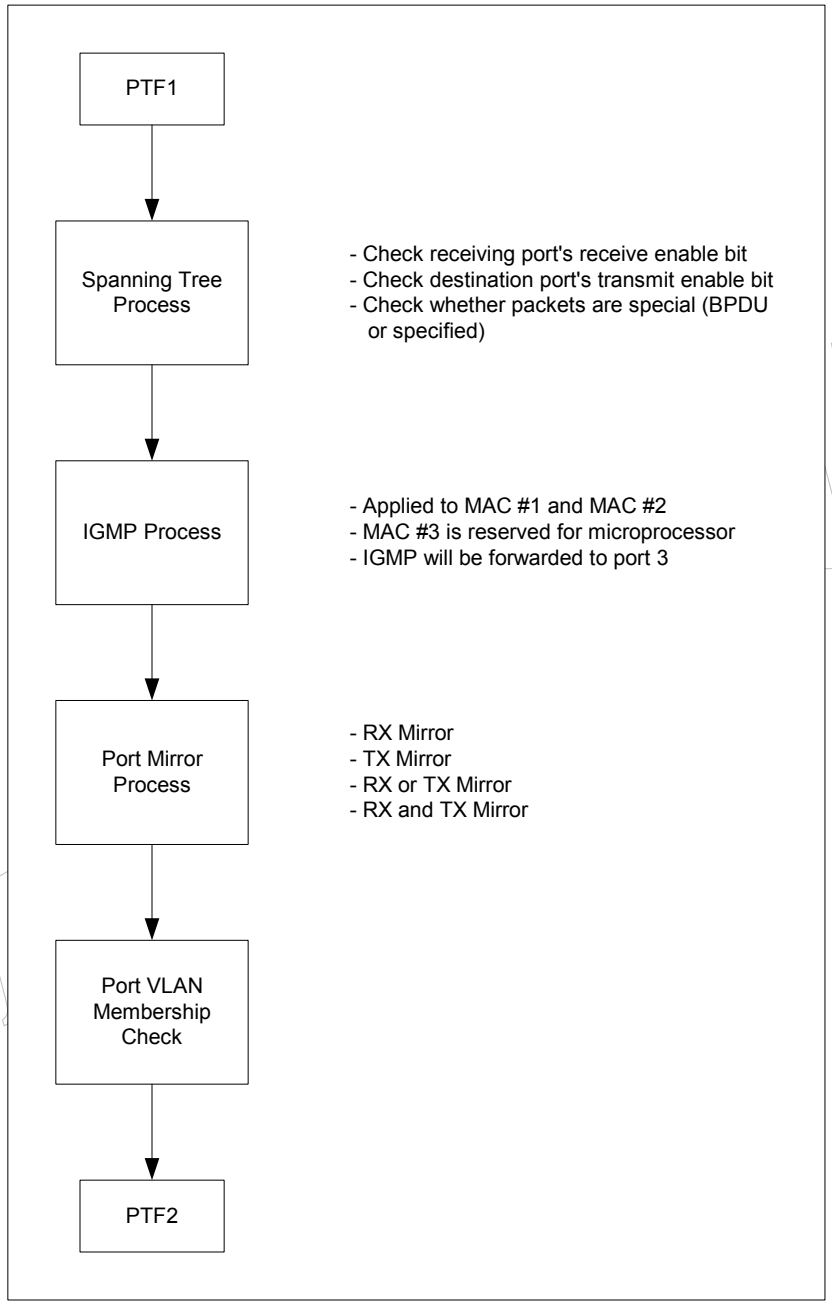
The KS8993M will forward packets using the algorithm that is depicted in the following flowcharts. Figure 4 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by Spanning Tree, IGMP Snooping, Port Mirroring and Port VLAN

processes to come up with “port to forward 2” (PTF2) as shown in Figure 5. PTF2 is where the packet will be sent.

**Figure 4: Destination Address look up flowchart, stage 1**



## Figure 5: Destination Address resolution flowchart, stage 2



**The KS8993M will not forward the following packets:**

(1). Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
(2). 802.3x pause frames. The KS8993M will intercept these packets and perform the appropriate actions.
(3). "Local" packets. Based on destination address (DA) look up. If the destination port from the look up table matches the port where the packet was from, the packet is defined as "local".

## 4.6 Switching Engine

The KS8993M features a high performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8993M has a 32kB internal frame buffer. This resource is shared between all three ports. The buffer sharing mode can be programmed through Global Register 2 (0x02). In one mode, ports are allowed to use any free buffers in the buffer pool. In the second mode, each port is only allowed to use 1/3 of the total buffer pool. There are a total of 250 buffers available. Each buffer is sized at 128B.

## 4.7 MAC operation

The KS8993M strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96 bits time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96 bits time IPG is measured from MCRS and the next MTXEN.

### *4.7.1 Back-off Algorithm*

The KS8993M implements the IEEE Standard 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back-off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration in Global Register 4 (0x04)

### *4.7.2 Late Collision*

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet will be dropped.

### *4.7.3 Illegal Frames*

The KS8993M discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Global Register 4 (0x04). For special applications, the KS8993M can also be programmed to accept frames up to 1916 bytes in the same global register. Since the KS8993M supports VLAN tags, the maximum sizing is adjusted when these tags are present. See the EEPROM section for programming options.

### *4.7.4 Flow Control*

The KS8993M supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8993M receives a pause control frame, the KS8993M will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KS8993M will be transmitted.

On the transmit side, the KS8993M has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KS8993M will flow control a port, which just received a packet, if the destination port resource is being used up. The KS8993M will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8993M will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being activated and deactivated too many times.

The KS8993M will flow control all ports if the receive queue becomes full.

### *4.7.5 Half Duplex Back Pressure*

A half duplex back pressure option (Note: not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full duplex mode. If back pressure is required, the KS8993M will send preambles to defer the other stations' transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other

stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type back pressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

To ensure no packet loss in 10 Base-T or 100 Base-TX half duplex modes, the user must enable the following:

1. Aggressive backoff (Global Register 3 (0x03), bit 0 or external strap-in pin SMAC = high)
2. No excessive collision drop (Global Register 4 (0x04), bit 3 or external strap-in pin SMAC = high)

These bits are not set as defaults because this is not the IEEE standard.

### *4.7.6 Broadcast Storm Protection*

The KS8993M has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus use too many switch resources (bandwidth and available space in transmit queues). The KS8993M has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis. The rate is based on a 50ms interval for 100BT and a 500 ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Global Register 6 (0x06) and 7 (0x07). The default setting for registers 6 and 7 is 0x4A, which is 74 decimal. This is equal to a rate of 1 %, calculated as follows:

148,800 frames/sec * 50 ms/interval * 1% = 74 frames/interval (approx.) = 0x4A

## 4.8 MII Interface Operation

The MII (Media Independent Interface) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The MII Interface provided by the KS8993M is connected to the device’s third MAC. The interface contains two distinct groups of signals: one for transmission and the other for reception. The following table describes the signals used in the MII interface.

## Table 3: MII Signals

| KS8993M PHY Mode Connections | | | KS8993M MAC Mode Connections | |
|---|---|---|---|---|
| **External MAC Controller Signals** | **KS8993M PHY Signals** | **Pin Descriptions** | **External PHY Signals** | **KS8993M MAC Signals** |
| MTXEN | SMTXEN | Transmit enable | MTXEN | SMRXDV |
| MTXER | SMTXER | Transmit error | MTXER | (not used) |
| MTXD3 | SMTXD[3] | Transmit data bit 3 | MTXD3 | SMRXD[3] |
| MTXD2 | SMTXD[2] | Transmit data bit 2 | MTXD2 | SMRXD[2] |
| MTXD1 | SMTXD[1] | Transmit data bit 1 | MTXD1 | SMRXD[1] |
| MTXD0 | SMTXD[0] | Transmit data bit 0 | MTXD0 | SMRXD[0] |
| MTXC | SMTXC | Transmit clock | MTXC | SMRXC |
| MCOL | SCOL | Collision detection | MCOL | SCOL |
| MCRS | SCRS | Carrier sense | MCRS | SCRS |
| MRXDV | SMRXDV | Receive data valid | MRXDV | SMTXEN |
| MRXER | (not used) | Receive error | MRXER | SMTXER |
| MRXD3 | SMRXD[3] | Receive data bit 3 | MRXD3 | SMTXD[3] |
| MRXD2 | SMRXD[2] | Receive data bit 2 | MRXD2 | SMTXD[2] |
| MRXD1 | SMRXD[1] | Receive data bit 1 | MRXD1 | SMTXD[1] |
| MRXD0 | SMRXD[0] | Receive data bit 0 | MRXD0 | SMTXD[0] |
| MRXC | SMRXC | Receive clock | MRXC | SMTXC |

The MII interface operates in either PHY mode or MAC mode. The interface is a nibble wide data interfaces and therefore run at ¼ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors. For half duplex operation there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the interface for PHY mode operation and the signal MTXER is not provided on the interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation, if the device interfacing with the KS8993M has an MRXER pin, it should be tied low. For MAC mode operation, if the device interfacing with the KS8993M has an MTXER pin, it should be tied low.

## 4.9 SNI (7-wire) Interface Operation

The SNI (Serial Network Interface) or 7-wire is compatible with some controllers used for network layer protocol processing. In SNI mode, the KS8993M acts like a PHY and the external controller functions as the MAC. The KS8993M can interface directly with external controllers using the 7-wire interface. These signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in the table below.

**Table 4: SNI Signals**

| Pin Descriptions | External MAC Controller Signals | KS8993M PHY Signals |
|---|---|---|
| Transmit enable | TXEN | SMTXEN |
| Serial transmit data | TXD | SMTXD[0] |
| Transmit clock | TXC | SMTXC |
| Collision detection | COL | SCOL |
| Carrier sense | CRS | SMRXDV |
| Serial receive data | RXD | SMRXD[0] |
| Receive clock | RXC | SMRXC |

The SNI interface is a bit wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Similarly, the receive side has an indicator that conveys when the data is valid.

For half duplex operation, the KS8993M's SCOL signal is used to indicate that a collision has occurred during transmission.

## 4.10 MII Management Interface (MIIM)

The KS8993M supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KS8993M. An external device with MDC/MDIO capability can be used to read the PHY status or configure the PHY settings. Further details on the MIIM interface can be found in section 22.2.4.5 of the IEEE 802.3 specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KS8993M device.
- Access to a set of six 16-bits registers, consisting of standard MIIM registers [0:5].

The following table depicts the MII Management Interface frame format.

**Table 5: MII Management Interface frame format**

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | xx0AA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| **Write** | 32 1's | 01 | 01 | xx0AA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

For the KS8993M, MIIM register access is selected when bit 2 of the PHY address is set to '0'. PHY address bits [4:3] are not defined for MIIM register access, and hence can be set to either 0's or 1's in read/write operation.

## 4.11 Serial Management Interface (SMI)

The Serial Management Interface is the KS8993M non-standard MIIM interface that provides access to all KS8993M configuration registers. This interface allows an external device to completely monitor and control the states of the KS8993M.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KS8993M device.
- Access to all KS8993M configuration registers. Registers access includes the Global, Port and Advanced Control Registers 0-127 (0x00 – 0x7F), and indirect access to the standard MIIM registers [0:5].

The following table depicts the Serial Management Interface frame format.

**Table 6: Serial Management Interface (SMI) frame format**

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | RR1xx | RRRRR | Z0 | 0000_0000_DDDD_DDDD | Z |
| **Write** | 32 1's | 01 | 01 | RR1xx | RRRRR | 10 | xxxx_xxxx_DDDD_DDDD | Z |

For the KS8993M, SMI register access is selected when bit 2 of the PHY address is set to '1'. PHY address bits [1:0] are not defined for SMI register access, and hence can be set to either 0's or 1's in read/write operation.

To access the KS8993M registers 0-127 (0x00 – 0x7F), the following applies:

- PHYAD[4:3] and REGAD[4:0] are concatenated to form the 7-bits address. i.e., {PHYAD[4:3], REGAD[4:0]} = bits [6:0] of the 7-bits address.
- Registers are 8 data bits wide. For read operation, data bits [15:8] are read back as 0's. For write operation, data bits [15:8] are not defined, and hence can be set to either 0's or 1's.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

# 5.0 Advanced Switch Functions

## 5.1 Spanning Tree Support

To support spanning tree, port 3 is the designated port for the processor.

The other ports (port 1 and port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable" and "learning disable" register settings in registers 18 and 34 for ports 1 and 2, respectively. The following description shows the port setting and software actions taken for each of the five spanning tree states.

**Disable state:** The port should not forward or receive any packets. Learning is disabled.

**Port setting:**

"transmit enable = 0, receive enable = 0, learning disable =1"

**Software action:**

The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the "static MAC table" with "overriding bit" set) and the processor should discard those packets. Note: processor is connected to port 3 via MII interface. Address learning is disabled on the port in this state.

**Blocking state:** Only packets to the processor are forwarded. Learning is disabled.

**Port setting:**

"transmit enable = 0, receive enable = 0, learning disable =1"

**Software action:**

The processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.

**Listening state:** Only packets to and from the processor are forwarded. Learning is disabled.

**Port setting:**

"transmit enable = 0, receive enable = 0, learning disable =1"

**Software action:**

The processor should program the "Static MAC table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "Special Tagging Mode" (section 5.2) for details. Address learning is disabled on the port in this state.

**Learning state:** Only packets to and from the processor are forwarded. Learning is enabled.

**Port setting:**

"transmit enable = 0, receive enable = 0, learning disable = 0"

**Software action:**

The processor should program the "Static MAC table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "Special Tagging Mode" (section 5.2) for details. Address learning is enabled on the port in this state.

**Forwarding state:** Packets are forwarded and received normally. Learning is enabled.

**Port setting:**

"transmit enable = 1, receive enable = 1, learning disable = 0"

**Software action:**

The processor should program the "Static MAC table" with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see "Special Tagging Mode" (section 5.2) for details. Address learning is enabled on the port in this state.

## 5.2 Upstream Special Tagging Mode

Upstream Special Tagging Mode is designed for Spanning Tree protocol IGMP snooping and is flexible for use in other applications. The Upstream Special Tagging Mode, similar to 802.1Q, requires software to change network drivers to modify/strip/interpret the special tag. This mode is enabled by setting both register 11 bit 0 and register 48 bit 2 to "1".

**Table 7: Upstream Special Tagging Mode Format**

| 802.1Q Tag Format | Special Tag Format |
|---|---|
| TPID (tag protocol identifier, 0x8100) + TCI. | STPID (special tag identifier, 0x810 + 4 bit for "port mask") + TCI |

The STPID is only seen and used by the port 3 interface, which should be connected to a processor.

The KS8993M uses a non-zero "port mask" to bypass the look up result and override any port setting, regardless of port states (disable, blocking, listening, learning).

For packets from regular ports (port 1 & port 2) to port 3, the port mask is used to tell the processor which port the packets were received on, defined as follows:

"0001" from port 1,
"0010" from port 2,

No port mask values, other than the previous two defined ones, should be received in Upstream Special Tagging Mode. The egress rules are defined as follows:

**Table 8: STPID Egress Rules (Switch Port 3 to Processor)**

| Ingress Packets | Egress Action to Tag Field |
|---|---|
| Tagged with 0x8100 + TCI | - Modify TPID to 0x810 + "port mask", which indicates source port.<br>- No change to TCI if VID is not null<br>- Replace null VID with ingress port VID<br>- Recalculate CRC |
| Not tagged. | - Insert TPID to 0x810 + "port mask", which indicates source port<br>– Insert TCI with ingress port VID<br>- Recalculate CRC |

## 5.3 IGMP Support

For IGMP support in layer 2, the KS8993M provides two components:

*"IGMP" Snooping* The KS8993M will trap IGMP packets and forward them only to the processor (port 3). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

*"multicast address insertion" in the Static MAC Table* Once the multicast address is programmed in the Static MAC Table, the multicast session will be trimmed to the subscribed ports, instead of broadcasting to all ports.

To enable IGMP support, set register 5 bit 6 to "1". Also, "Special Tagging Mode" needs to be enabled, so that the processor knows which port the IGMP packet was received on. This is achieved by setting both register 11 bit 0 and register 48 bit 2 to "1".

## 5.4 Port Mirroring Support

KS8993M supports “Port Mirroring” comprehensively as:

**1) “receive only” mirror on a port** All the packets received on the port will be mirrored on the sniffer port. For example, port 1 is programmed to be “receive sniff” and port 3 is programmed to be the “sniffer port”. A packet, received on port 1, is destined to port 2 after the internal look up. The KS8993M will forward the packet to both port 2 and port 3. The KS8993M can optionally forward even “bad” received packets to the “sniffer port”.

**2) “transmit only” mirror on a port** All the packets transmitted on the port will be mirrored on the sniffer port. For example, port 1 is programmed to be “transmit sniff” and port 3 is programmed to be the “sniffer port”. A packet, received on any of the ports, is destined to port 1 after the internal look up. The KS8993M will forward the packet to both port 1 and port 3.

**3) “receive and transmit” mirror on two ports** All the packets received on port A and transmitted on port B will be mirrored on the sniffer port. To turn on the “AND” feature, set register 5 bit 0 to “1”. For example, port 1 is programmed to be “receive sniff”, port 2 is programmed to be “transmit sniff” and port 3 is programmed to be the “sniffer port”. A packet, received on port 1, is destined to port 2 after the internal look up. The KS8993M will forward the packet to both port 2 and port 3.

Multiple ports can be selected to be “receive sniff” or “transmit sniff”. And any port can be selected to be the “sniffer port”. All these per port features can be selected through registers 17, 33 and 49 for ports 1, 2 and 3, respectively.

## 5.5 IEEE 802.1Q VLAN support

The KS8993M supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KS8993M provides a 16-entries VLAN Table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address look up. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for look up. In VLAN mode, the look up process starts with VLAN Table look up to determine whether the VID is valid. If the VID is not valid, the packet will be dropped and its address will not be learned. If the VID is valid, the FID is retrieved for further look up. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning.

**Table 9: FID+DA look up in VLAN mode**

| DA found in Static MAC Table? | Use FID flag? | FID match? | DA+FID found in Dynamic MAC Table? | Action |
|---|---|---|---|---|
| No | Don't care | Don't care | No | Broadcast to the membership ports defined in the VLAN Table bits [18:16] |
| No | Don't care | Don't care | Yes | Send to the destination port defined in the Dynamic MAC Address Table bits [53:52] |
| Yes | 0 | Don't care | Don't care | Send to the destination port(s) defined in the Static MAC Address Table bits [50:48] |
| Yes | 1 | No | No | Broadcast to the membership ports defined in the VLAN Table bits [18:16] |
| Yes | 1 | No | Yes | Send to the destination port defined in the Dynamic MAC Address Table bits [53:52] |
| Yes | 1 | Yes | Don't care | Send to the destination port(s) defined in the Static MAC Address Table bits [50:48] |

**Table 10: FID+SA look up in VLAN mode**

| FID+SA found in Dynamic MAC Table? | Action |
|---|---|
| No | Learn and add FID+SA to the Dynamic MAC Address Table |
| Yes | Update time stamp |

Advanced VLAN features, such as “Ingress VLAN filtering” and “Discard Non PVID packets” are also supported by the KS8993M. These features can be set on a per port basis, and are defined in register 18, bit 6 and bit 5, respectively for port 1.

## 5.6 QoS Priority Support

This feature provides Quality of Service (QoS) for applications, such as VoIP and video conferencing. The KS8993M per port transmit queue could be split into two priority queues: a high priority queue and a low priority queue. Bit 0 of registers 16, 32 and 48 is used to enable split transmit queues for ports 1, 2 and 3, respectively. Optionally, the Px_TXQ2 strap-in pins can be used to enable this feature. With split transmit queues, high priority packets will be placed in the high priority queue and low priority packets will be placed in the low priority queue.

For split transmit queues, the KS8993M provides four priority schemes:

(1) “Transmit all high priority packets before low priority packets”, i.e. a low priority packet could be transmitted only when the high priority queue is empty;
(2) “Transmit high priority packets and low priority packets at 10:1 ratio”, i.e. transmit a low priority packet after every 10 high priority packets are transmitted, if both queues are busy;
(3) “Transmit high priority packets and low priority packets at 5:1 ratio”;
(4) “Transmit high priority packets and low priority packets at 2:1 ratio”.

If a port's transmit queue is not split, both high priority packets and low priority packets have equal priority in the transmit queue. Register 5 bits [3:2] are used to select the desired priority scheme. Optionally, the PRSEL1 and PRSEL0 strap-in pins can be used.

### Port based Priority

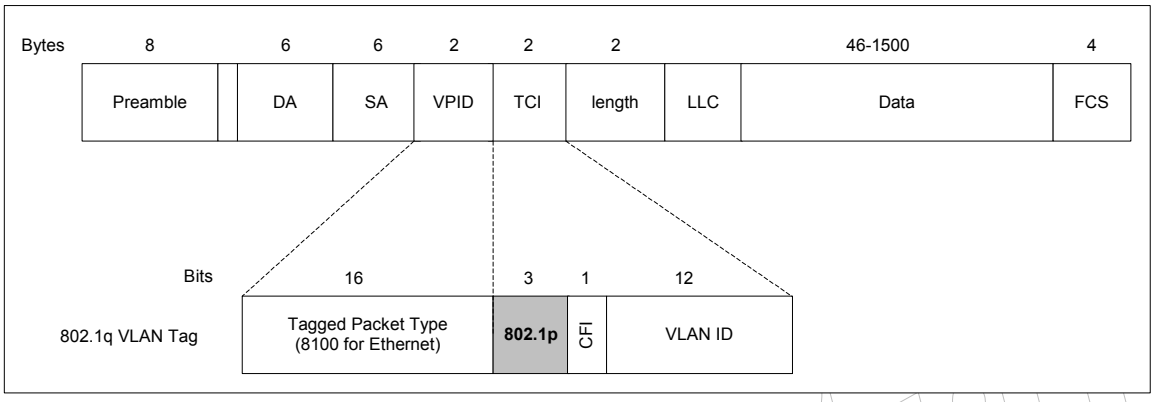
With port based priority, each ingress port can be individually classified as a high priority receiving port. All packets received at the high priority receiving port are marked as high priority, and will be sent to the high priority transmit queue if the corresponding transmit queue is split. Bit 4 of registers 16, 32 and 48 is used to enable port based priority for ports 1, 2 and 3, respectively. Optionally, the Px_PP strap-in pins can be used to enable this feature.

### 802.1p based Priority

For 802.1p based priority, the KS8993M will examine the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bits priority field in the VLAN tag is retrieved and compared against the “priority base” value, specified by register 2 bits [6:4]. The “priority base” value is programmable; its default value is 0x4.

The following figure illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

**Figure 6: 802.1p Priority Field Format**




If an ingress packet has an equal or higher priority value than the "priority base" value, the packet will be placed in the high priority transmit queue if the corresponding transmit queue is split. 802.1p based priority is enabled by bit 5 of registers 16, 32 and 48 for ports 1, 2 and 3, respectively. Optionally, the Px_1PEN strap-in pins can be used to enable this feature.

The KS8993M provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN Protocol ID (VPID) and the 2 bytes Tag Control Information field (TCI), is also refer to as the 802.1Q VLAN Tag.

**Tag insertion** is enabled by bit 2 of registers 16, 32 and 48 for ports 1, 2 and 3, respectively. Optionally, the Px_TAGINS strap-in pins can be used to enable this feature. At the egress port, untagged packets are tagged with the ingress port's default tag. The default tags are programmed in register sets {19,20}, {35,36} and {51,52} for ports 1, 2 and 3, respectively. The KS8993M will not add tags to already tagged packets.

**Tag removal** is enabled by bit 1 of registers 16, 32 and 48 for ports 1, 2 and 3, respectively. Optionally, the Px_TAGRM strap-in pins can be used to enable this feature. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KS8993M will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

**802.1p priority field re-mapping** is a QoS feature that allows the KS8993M to set the "User Priority Ceiling" at any ingress port. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the

packet's priority field is replaced with the default tag's priority field. The "User Priority Ceiling" is enabled by bit 3 of registers 16, 32 and 48 for ports 1, 2 and 3, respectively.

**DiffServ based Priority**

DiffServ based priority uses registers 96 to 103. More details are provided at the beginning of the **Advanced Control Registers** section.

## 5.7 Rate Limiting Support

The KS8993M supports hardware rate limiting independently on the "receive side" and on the "transmit side" on a per port basis. Rate limiting is supported in both priority and non-priority environment. The rate limit starts from 0 kbps and goes up to the line rate in steps of 32 kbps. The KS8993M uses "one second" as the rate limiting interval. At the beginning of each interval, the counter is cleared to zero, and the rate limit mechanism starts to count the number of bytes during the interval.

On the "receive side", if the number of bytes exceeds the programmed limit, the switch will stop receiving packets on the port until the "one second" interval expires. Flow control can be enabled to prevent packet loss. If the rate limit is programmed greater than or equal to 128 kbps and the byte counter is 8 Kbytes below the limit, flow control will be triggered. If the rate limit is programmed lower than 128 kbps and the byte counter is 2 Kbytes below the limit, flow control will also be triggered.

On the "transmit side", if the number of bytes exceeds the programmed limit, the switch will stop transmitting packets on the port until the "one second" interval expires.

If priority is enabled, the KS8993M can be programmed to support different rate limits for high priority packets and low priority packets.

## 5.8 Configuration Interface

The KS8993M can operate as both a managed switch and an unmanaged switch.

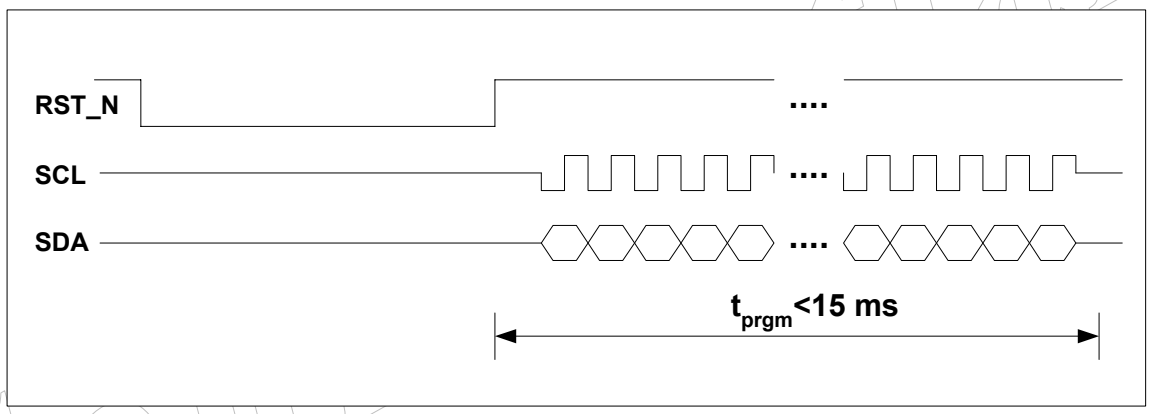
In unmanaged mode, the KS8993M is typically programmed using an EEPROM. If no EEPROM is present, the KS8993M is configured using its default register settings. Some defaults settings are configured via strap-in pin options. The strap-in pins are indicated in the "KS8993M Pin Description and I/O Assignment" table in section 1.2.

### 5.8.1 I2C Master Serial Bus Configuration

With an additional I2C ("2-wire") EEPROM, the KS8993M can perform more advanced switch features like "broadcast storm protection" and "rate control" without the need of an external processor.

For KS8993M I2C Master configuration, the EEPROM stores the configuration data for register 0 to register 109 (as defined in the KS8993M register map) with the exception of the "Read Only" status registers. After the de-assertion of reset, the KS8993M will sequentially read in the configuration data for all 110 registers, starting from register 0. The configuration access time ($t_{prgm}$) is less than 15 ms, as depicted in the following figure.

**Figure 7: KS8993M EEPROM Configuration Timing Diagram**




The following is a sample procedure for programming the KS8993M with a pre-configured EEPROM:

1. Connect the KS8993M to the EEPROM by joining the SCL and SDA signals of the respective devices. For the KS8993M, SCL is pin 97 and SDA is pin 98.

2. Enable I2C master mode by setting the KS8993M strap-in pins, PS[1:0] (pins 100 and 101, respectively) to "00".

3. Check to ensure that the KS8993M reset signal input, RST_N (pin 67), is properly connected to the external reset source at the board level.

4. Program the desired configuration data into the EEPROM.

5. Place the EEPROM on the board and power up the board.

6. Assert an active-low reset to the RST_N pin of the KS8993M. After reset is de-asserted, the KS8993M will begin reading the configuration data from the EEPROM. The KS8993M will check that the first byte read from the EEPROM is “93”. If this value is correct, EEPROM configuration will continue. If not, EEPROM configuration access is denied and all other data sent from the EEPROM will be ignored by the KS8993M. The configuration access time ($t_{prgm}$) is less than 15 ms.

**Note:** For proper operation, check to ensure that the KS8993M PWRDN input signal (pin 36) is not asserted during the reset operation. The PWRDN input is active low.

### 5.8.2 I2C Slave Serial Bus Configuration

In managed mode, the KS8993M can be configured as an I2C slave device. In this mode, an I2C master device (external controller/CPU) has complete programming access to the KS8993M’s 128 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the “Static MAC Table”, “VLAN Table”, “Dynamic MAC Table” and “MIB Counters”. The tables and counters are indirectly accessed via registers 110 thru 120.

In I2C slave mode, the KS8993M operates like other I2C slave devices. Addressing the KS8993M’s 8 bit registers is similar to addressing Atmel’s AT24C02 EEPROM’s memory locations. Details of I2C read/write operations and related timing information can be found in the AT24C02 Datasheet.

Two fixed 8 bits device addresses are used to address the KS8993M in I2C slave mode. One is for read; the other is for write. The addresses are as follow:

1011_1111 <read>
1011_1110 <write>

The following is a sample procedure for programming the KS8993M using the I2C slave serial bus:

1. Enable I2C slave mode by setting the KS8993M strap-in pins PS[1:0] (pins 100 and 101 respectively) to “01”.

2. Power up the board and assert reset to the KS8993M. After reset, the “Start Switch” bit (register 1 bit 0) will be set to ‘0’.

3. Configure the desired register settings in the KS8993M, using the I2C write operation.

4. Read back and verify the register settings in the KS8993M, using the I2C read operation.

5. Write a '1' to the "Start Switch" bit to start the KS8993M with the programmed settings.

   **Note:** The "Start Switch" bit cannot be set to '0' to stop the switch after an '1' is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the "Start Switch" bit is set to '1'.

   Some of the configuration settings, such as "Aging enable", "Auto Negotiation Enable", "Force Speed" and "Power down" can be programmed after the switch has been started.

### 5.8.3 SPI Slave Serial Bus Configuration

In managed mode, the KS8993M can be configured as a SPI slave device. In this mode, a SPI master device (external controller/CPU) has complete programming access to the KS8993M's 128 registers. Programming access includes the Global Registers, Port Registers, Advanced Control Registers and indirect access to the "Static MAC Table", "VLAN Table", "Dynamic MAC Table" and "MIB Counters". The tables and counters are indirectly accessed via registers 110 thru 120.

The KS8993M supports two standard SPI commands: '0000_0011' for data read and '0000_0010' for data write. SPI multiple read and multiple write are also supported by the KS8993M to expedite register read back and register configuration, respectively.

SPI multiple read is initiated when the master device continues to drive the KS8993M SPIS_N input pin (SPI Slave Select signal) low after a byte (a register) is read. The KS8993M internal address counter will increment automatically to the next byte (next register) after the read. The next byte at the next register address will be shifted out onto the KS8993M SPIQ output pin. SPI multiple read will continue until the SPI master device terminates it by de-asserting the SPIS_N signal to the KS8993M.

Similarly, SPI multiple write is initiated when the master device continues to drive the KS8993M SPIS_N input pin low after a byte (a register) is written. The KS8993M internal address counter will increment automatically to the next byte (next register) after the write. The next byte that is sent from the master device to the KS8993M SDA input pin will be written to the next register address. SPI multiple write will continue until the SPI master device terminates it by de-asserting the SPIS_N signal to the KS8993M.

For both SPI multiple read and multiple write, the KS8993M internal address counter will wrap back to register address zero once the highest register address is reached.

This feature allows all 128 KS8993M registers to be read, or written with a single SPI command and any initial register address.

The KS8993M is capable of supporting a 5 MHz SPI bus.

The following is a sample procedure for programming the KS8993M using the SPI bus:

1. At the board level, connect the KS8993M pins as follows:

**Table 11: KS8993M SPI Connections**

| KS8993M Pin # | KS8993M Signal Name | External Processor Signal Description |
|---|---|---|
| 99 | SPIS_N | SPI Slave Select |
| 97 | SCL (SPIC) | SPI Clock |
| 98 | SDA (SPID) | SPI Data (Master output; Slave input) |
| 96 | SPIQ | SPI Data (Master input; Slave output) |

2. Enable SPI slave mode by setting the KS8993M strap-in pins PS[1:0] (pins 100 and 101 respectively) to “10”.

3. Power up the board and assert reset to the KS8993M. After reset, the “Start Switch” bit (register 1 bit 0) will be set to ‘0’.

4. Configure the desired register settings in the KS8993M, using the SPI write or multiple write command.

5. Read back and verify the register settings in the KS8993M, using the SPI read or multiple read command.

6. Write a ‘1’ to the “Start Switch” bit to start the KS8993M with the programmed settings.

   **Note:** The “Start Switch” bit cannot be set to ‘0’ to stop the switch after an ‘1’ is written to this bit. Thus, it is recommended that all switch configuration settings are programmed before the “Start Switch” bit is set to ‘1’.

Some of the configuration settings, such as “Aging enable”, “Auto Negotiation Enable”, “Force Speed” and “Power down” can be programmed after the switch has been started.

The following four figures illustrate the SPI data cycles for “Write”, “Read”, “Multiple Write” and “Multiple Read”. The read data is registered out of SPIQ on the falling edge of SPIC, and the data input on SPID is registered on the rising edge of SPIC.

**Figure 8: SPI Write Data Cycle**

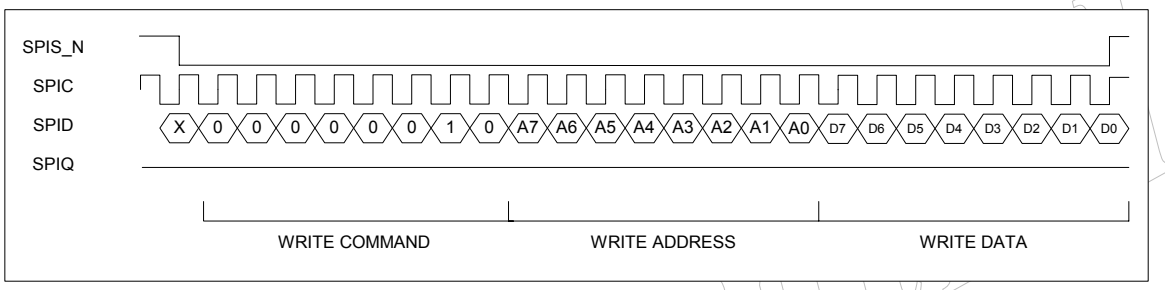



**Figure 9: SPI Read Data Cycle**

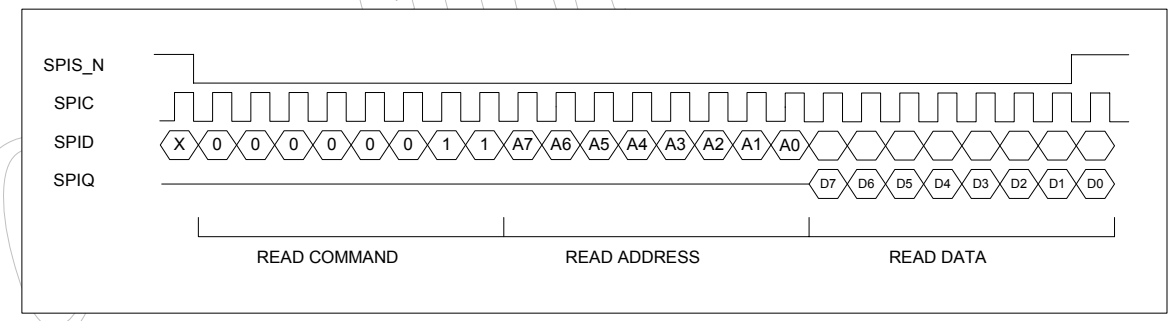


**Figure 10: SPI Multiple Write**

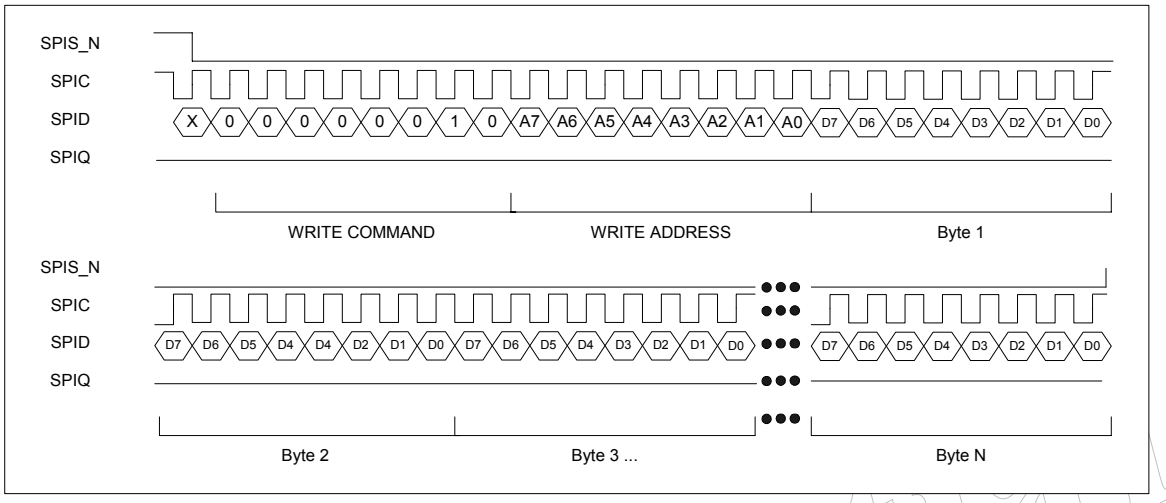
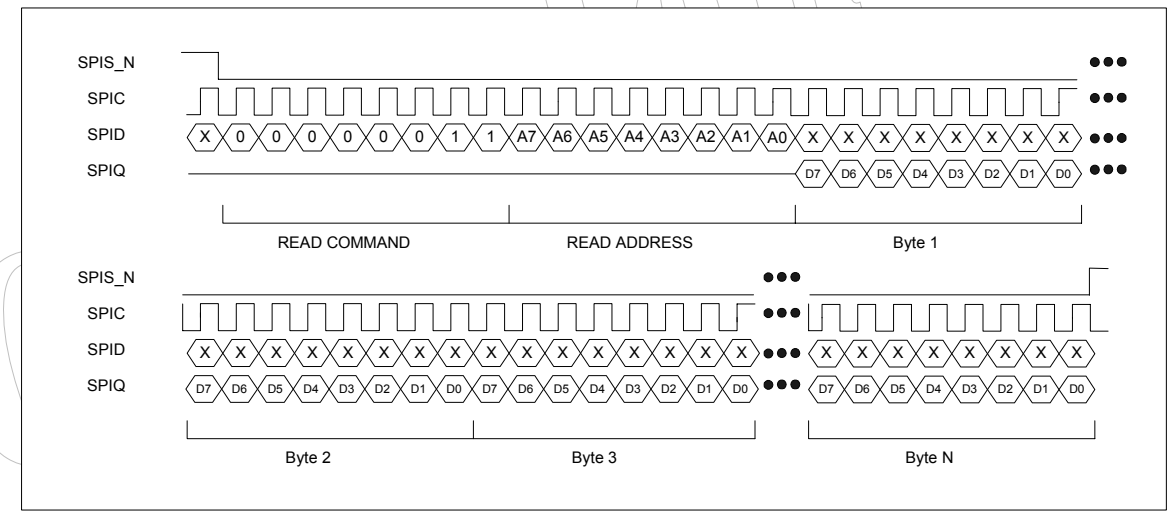



**Figure 11: SPI Multiple Read**



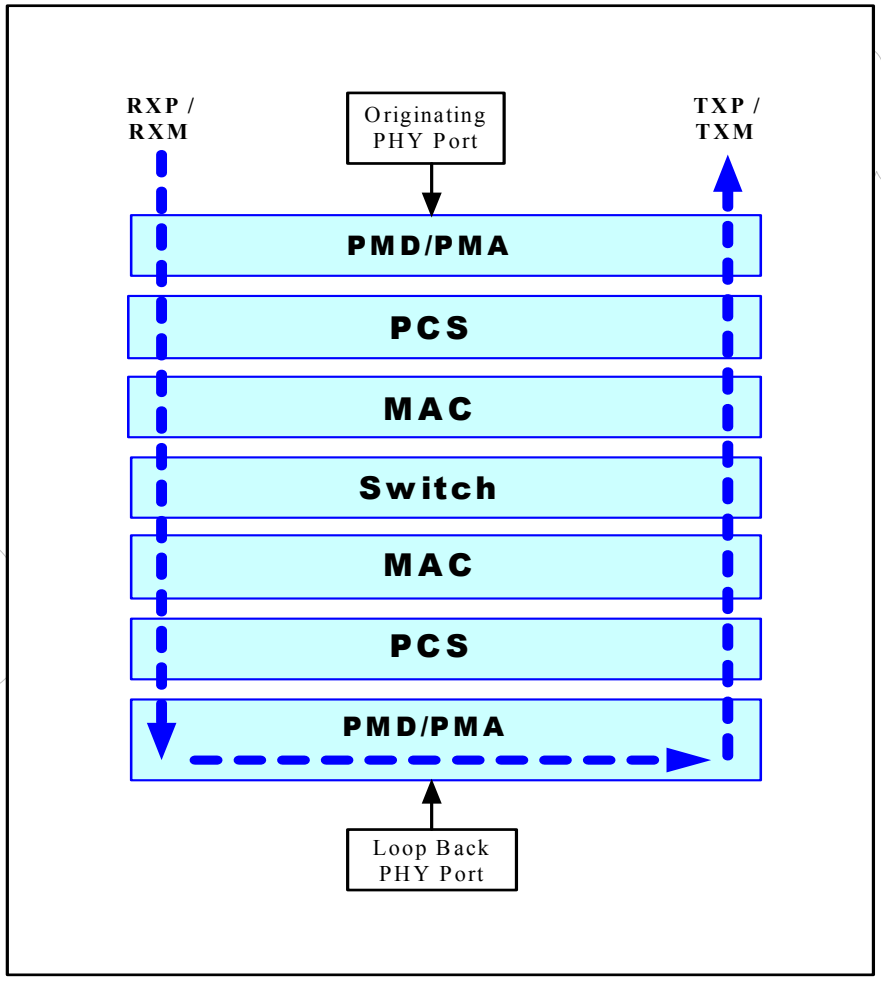

## 5.9 Loop Back Support

The KS8993M provides loop back support for remote diagnostic of failure. In loop back mode, the speed at both PHY ports needs to be set to 100BaseTX, and the “Priority Buffer reserve” bit needs to be set to 48 pre-allocated buffers per output queue. The latter is required to prevent loop back packet drops and is achieved by setting register 4 bit 0 to ‘1’.

Bit 0 of registers 29 and 45 is used to enable loop back for ports 1 and 2, respectively. Alternatively, the MII Management register 0, bit 14 can be used to enable loop back.

Loop back is conducted between the KS8993M's two PHY ports. The loop back path starts at the "Originating" PHY port's receive inputs (RXP/RXM), wraps around at the "Loop Back" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM). The KS8993M loop back path is illustrated in the following figure.

**Figure 12: Loop Back Path**



# 6.0 MII Management (MIIM) Registers

The MIIM interface is used to access the MII PHY registers defined in this section. The SPI, I2C and SMI interfaces can also be used to access these registers. The latter three interfaces use a different mapping mechanism than the MIIM interface.

As defined in the IEEE 802.3 specification, the "PHYAD" are assigned as "0x1" for PHY port 1 and "0x2" for PHY port 2. The "REGAD" supported are 0,1,2,3,4 and 5.

| Register Number | Description |
|---|---|
| 0x0 | Basic Control Register |
| 0x1 | Basic Status Register |
| 0x2 | Physical Identifier I |
| 0x3 | Physical Identifier II |
| 0x4 | Auto-Negotiation Advertisement Register |
| 0x5 | Auto-Negotiation Link Partner Ability Register |
| 0x6 – 0x1F | Not supported |

### *6.1.1 Register 0: MII Basic Control*

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Soft reset | RO | NOT SUPPORTED | 0 | |
| 14 | Loop back | R/W | =1, Loop back mode<br>=0, Normal operation | 0 | Reg. 29, bit 0<br>Reg. 45, bit 0 |
| 13 | Force 100 | R/W | =1, 100 Mbps<br>=0, 10 Mbps | 0 | Reg. 28, bit 6<br>Reg. 44, bit 6 |
| 12 | AN enable | R/W | =1, Auto-negotiation enabled<br>=0, Auto-negotiation disabled | 1 | |
| 11 | Power down | R/W | =1, Power down<br>=0, Normal operation | 0 | Reg. 29, bit 3<br>Reg. 45, bit 3 |
| 10 | Isolate | RO | NOT SUPPORTED | 0 | |
| 9 | Restart AN | R/W | =1, Restart auto-negotiation<br>=0, Normal operation | 0 | Reg. 29, bit 5<br>Reg. 45, bit 5 |
| 8 | Force full duplex | R/W | =1, Full duplex<br>=0, Half duplex | 0 | Reg. 28, bit 5<br>Reg. 44, bit 5 |
| 7 | Collision test | RO | NOT SUPPORTED | 0 | |
| 6 | Reserved | RO | | 0 | |
| 5 | Reserved | RO | | 0 | |
| 4 | Force MDIX | R/W | =1, Force MDIX<br>=0, Normal operation | 0 | Reg. 29, bit 1<br>Reg. 45, bit 1 |
| 3 | Disable MDIX | R/W | =1, Disable auto MDIX<br>=0, Normal operation | 0 | Reg. 29, bit 2<br>Reg. 45, bit 2 |
| 2 | Disable far end fault | R/W | =1, Disable far end fault detection<br>=0, Normal operation | 0 | Reg. 29, bit 4<br>Reg. 45, bit 4 |
| 1 | Disable transmit | R/W | =1, Disable transmit<br>=0, Normal operation | 0 | Reg. 29, bit 6<br>Reg. 45, bit 6 |
| 0 | Disable LED | R/W | =1, Disable LED<br>=0, Normal operation | 0 | Reg. 29, bit 7<br>Reg. 45, bit 7 |

### 6.1.2 Register 1: MII Basic Status

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | T4 capable | RO | =0, Not 100 BaseT4 capable | 0 | |
| 14 | 100 Full capable | RO | =1, 100BaseTX full duplex capable<br>=0, Not capable of 100BaseTX full duplex | 1 | Always 1 |
| 13 | 100 Half capable | RO | =1, 100BaseTX half duplex capable<br>=0, Not 100BaseTX half duplex capable | 1 | Always 1 |
| 12 | 10 Full capable | RO | =1, 10BaseT full duplex capable<br>=0, Not 10BaseT full duplex capable | 1 | Always 1 |
| 11 | 10 Half capable | RO | =1, 10BaseT half duplex capable<br>=0, Not 10BaseT half duplex capable | 1 | Always 1 |
| 10-7 | Reserved | RO | | 0 | |
| 6 | Preamble suppressed | RO | NOT SUPPORTED | 0 | |
| 5 | AN complete | RO | =1, Auto-negotiation complete<br>=0, Auto-negotiation not completed | 0 | Reg. 30, bit 6<br>Reg. 46, bit 6 |
| 4 | Far end fault | RO | =1, Far end fault detected<br>=0, No far end fault detected | 0 | Reg. 31, bit 0 |
| 3 | AN capable | RO | =1, Auto-negotiation capable<br>=0, Not auto-negotiation capable | 1 | Reg. 28, bit 7<br>Reg. 44, bit 7 |
| 2 | Link status | RO | =1, Link is up<br>=0, Link is down | 0 | Reg. 30, bit 5<br>Reg. 46, bit 5 |
| 1 | Jabber test | RO | NOT SUPPORTED | 0 | |
| 0 | Extended capable | RO | =0, Not extended register capable | 0 | |

### 6.1.3 Register 2: PHYID HIGH

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15-0 | PHYID high | RO | High order PHYID bits | 0x0022 |

### 6.1.4 Register 3: PHYID LOW

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15-0 | PHYID low | RO | Low order PHYID bits | 0x1430 |

### 6.1.5 Register 4: Auto-Negotiation Advertisement Ability

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Next page | RO | NOT SUPPORTED | 0 | |
| 14 | Reserved | RO | | 0 | |
| 13 | Remote fault | RO | NOT SUPPORTED | 0 | |
| 12-11 | Reserved | RO | | 0 | |
| 10 | Pause | R/W | =1, Advertise pause ability<br>=0, Do not advertise pause ability | 1 | Reg. 28, bit 4<br>Reg. 44, bit 4 |
| 9 | Reserved | R/W | | 0 | |
| 8 | Adv 100 Full | R/W | =1, Advertise 100 full duplex ability<br>=0, Do not advertise 100 full duplex ability | 1 | Reg. 28, bit 3<br>Reg. 44, bit 3 |
| 7 | Adv 100 Half | R/W | =1, Advertise 100 half duplex ability<br>=0, Do not advertise 100 half duplex ability | 1 | Reg. 28, bit 2<br>Reg. 44, bit 2 |
| 6 | Adv 10 Full | R/W | =1, Advertise 10 full duplex ability<br>=0, Do not advertise 10 full duplex ability | 1 | Reg. 28, bit 1<br>Reg. 44, bit 1 |
| 5 | Adv 10 Half | R/W | =1, Advertise 10 half duplex ability<br>=0, Do not advertise 10 half duplex ability | 1 | Reg. 28, bit 0<br>Reg. 44, bit 0 |
| 4-0 | Selector field | RO | 802.3 | 00001 | |

### 6.1.6 Register 5: Auto-Negotiation Link Partner Ability

| Bit | Name | R/W | Description | Default | Reference |
|---|---|---|---|---|---|
| 15 | Next page | RO | NOT SUPPORTED | 0 | |
| 14 | LP ACK | RO | NOT SUPPORTED | 0 | |
| 13 | Remote fault | RO | NOT SUPPORTED | 0 | |
| 12-11 | Reserved | RO | | 0 | |
| 10 | Pause | RO | Link partner pause capability | 0 | Reg. 30, bit 4<br>Reg. 46, bit 4 |
| 9 | Reserved | RO | | 0 | |
| 8 | Adv 100 Full | RO | Link partner 100 full capability | 0 | Reg. 30, bit 3<br>Reg. 46, bit 3 |
| 7 | Adv 100 Half | RO | Link partner 100 half capability | 0 | Reg. 30, bit 2<br>Reg. 46, bit 2 |
| 6 | Adv 10 Full | RO | Link partner 10 full capability | 0 | Reg. 30, bit 1<br>Reg. 46, bit 1 |
| 5 | Adv 10 Half | RO | Link partner 10 half capability | 0 | Reg. 30, bit 0<br>Reg. 46, bit 0 |
| 4-0 | Reserved | RO | | 00000 | |

# 7.0 Register Map: Switch & PHY (8 bits registers)

### *Global Registers*

| Register (Decimal) | Register (Hex) | Description |
|---|---|---|
| 0-1 | 0x00-0x01 | Chip ID Registers |
| 2-11 | 0x02-0x0B | Global Control Registers |
| 12 | 0x0C | Reserved Register |
| 13-15 | 0x0D-0x0F | User Defined Registers |

### *Port Registers*

| Register (Decimal) | Register (Hex) | Description |
|---|---|---|
| 16-29 | 0x10-0x1D | Port 1 Control Registers, including MII PHY Registers |
| 30-31 | 0x1E-0x1F | Port 1 Status Registers, including MII PHY Registers |
| 32-45 | 0x20-0x2D | Port 2 Control Registers, including MII PHY Registers |
| 46-47 | 0x2E-0x2F | Port 2 Status Registers, including MII PHY Registers |
| 48-61 | 0x30-0x3D | Port 3 Control Registers, including MII PHY Registers |
| 62-63 | 0x3E-0x3F | Port 3 Status Registers, including MII PHY Registers |
| 64-95 | 0x40-0x5F | Reserved |

### *Advanced Control Registers*

| Register (Decimal) | Register (Hex) | Description |
|---|---|---|
| 96-103 | 0x60-0x67 | TOS Priority Control Registers |
| 104-109 | 0x68-0x6D | Switch Engine's MAC Address Registers |
| 110-111 | 0x6E-0x6F | Indirect Access Control Registers |
| 112-120 | 0x70-0x78 | Indirect Data Registers |
| 121-122 | 0x79-0x7A | Digital Testing Status Registers |
| 123-124 | 0x7B-0x7C | Digital Testing Control Registers |
| 125-126 | 0x7D-0x7E | Analog Testing Control Registers |
| 127 | 0x7F | Analog Testing Status Register |

## 7.1 Global Registers

### *7.1.1 Register 0 (0x00): Chip ID0*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Family ID | RO | Chip family | 0x93 |

### 7.1.2 Register 1 (0x01): Chip ID1 / Start Switch

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-4 | Chip ID | RO | 0x0 is assigned to M series. (93M) | 0x0 |
| 3-1 | Revision ID | RO | Revision ID | - |
| 0 | Start Switch | RW | = 1, start the chip when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1).<br><br>**Note:** In (PS1, PS0) = (0, 0) mode, the chip will start automatically after trying to read the external EEPROM. If EEPROM does not exist, the chip will use pin strapping and default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x93, (2) Register 1 bits [7:4] = 0x0. If this check is OK, the contents in the EEPROM will override chip registers' default values.<br><br>= 0, chip will not start when external pins (PS1, PS0) = (0,1) or (1,0) or (1,1). | - |

### 7.1.3 Register 2 (0x02): Global Control 0

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | New Back-off Enable | R/W | New back-off algorithm designed for UNH<br>1 = Enable<br>0 = Disable | 0x0 |
| 6-4 | 802.1p base priority | R/W | Used to classify priority for incoming 802.1Q packets. "user priority" is compared against this value.<br>>= : classified as high priority<br>< : classified as low priority | 0x4 |
| 3 | Pass flow control packet | R/W | = 1, switch will not filter 802.1x "flow control" packets | 0x0 |
| 2 | Buffer share mode | R/W | = 1, buffer pool is shared by all ports. A port can use more buffers when other ports are not busy.<br>= 0, a port is only allowed to use 1/3 of the buffer pool. | 0x1 |
| 1 | Reserved | R/W | Reserved | 0 |
| 0 | Link change age | R/W | = 1, link change from "link" to "no link" will cause fast aging (<800us) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 ± 75 seconds).<br><br>**Note:** If any port is unplugged, all addresses will be automatically aged out. | 0 |

### 7.1.4 Register 3 (0x03): Global Control 1

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Pass all frames | R/W | = 1, switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with Sniffer mode only. | 0 |
| 6 | Repeater mode | R/W | 0 = normal mode<br>1 = repeater mode (half duplex Hub mode) | 0 |
| 5 | IEEE 802.3x Transmit direction flow control enable | R/W | = 1, will enable transmit direction flow control feature.<br>= 0, will not enable transmit direction flow control feature. | 1 |
| 4 | IEEE 802.3x Receive direction flow control enable | R/W | = 1, will enable receive direction flow control feature.<br>= 0, will not enable receive direction flow control feature. | 1 |
| 3 | Frame Length field check | R/W | 1 = will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500). | 0 |
| 2 | Aging enable | R/W | 1 = enable age function in the chip<br>0 = disable age function in the chip | 1 |
| 1 | Fast age enable | R/W | 1 = turn on fast age (800us) | 0 |
| 0 | Aggressive back off enable | R/W | 1 = enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard. | SMAC (pin 69) value during reset |

### 7.1.5 Register 4 (0x04): Global Control 2

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Unicast port-VLAN mismatch discard | R/W | This feature is used for port-VLAN (described in reg. 17, reg. 33, ...)<br><br>= 1, all packets can not cross VLAN boundary<br>= 0, unicast packets (excluding unkown/multicast/broadcast) can cross VLAN boundary | 1 |
| 6 | Multicast storm protection disable | R/W | = 1, “Broadcast Storm Protection” does not include multicast packets. Only DA = FFFFFFFFFFFF packets will be regulated.<br>= 0, “Broadcast Storm Protection” includes DA = FFFFFFFFFFFF and DA[40] = 1 packets. | 1 |

| | | | | |
|---|---|---|---|---|
| 5 | Back pressure mode | R/W | = 1, carrier sense based backpressure is selected<br>= 0, collision based backpressure is selected | 1 |
| 4 | Flow control and back pressure fair mode | R/W | = 1, fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time.<br>= 0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be "fair" to the flow control port. | 1 |
| 3 | No excessive collision drop | R/W | = 1, the switch will not drop packets when 16 or more collisions occur.<br>= 0, the switch will drop packets when 16 or more collisions occur. | SMAC (pin 69) value during reset |
| 2 | Huge packet support | R/W | = 1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register.<br>= 0, the max packet size will be determined by bit 1 of this register. | 0 |
| 1 | Legal Maximum Packet size check enable | R/W | = 0, will accept packet sizes up to 1536 bytes (inclusive).<br>= 1, 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped. | SMRXD0 (pin 85) value during reset |
| 0 | Priority Buffer reserve | R/W | = 1, each output queue is pre-allocated 48 buffers, used exclusively for high priority packets. It is recommended to enable this when priority queue feature is turned on.<br>= 0, no reserved buffers for high priority packets. | 1 |

### *7.1.6 Register 5 (0x05): Global Control 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | 802.1Q VLAN enable | R/W | = 1, 802.1Q VLAN mode is turned on. VLAN table needs to set up before the operation.<br>= 0, 802.1Q VLAN is disabled. | 0 |
| 6 | IGMP snoop enable on Switch MII interface | R/W | =1, IGMP snoop is enabled. All the IGMP packets will be forwarded to the Switch MII port.<br>=0, IGMP snoop is disabled. | 0 |
| 5 | Reserved | R/W | | 0 |
| 4 | Reserved | R/W | | 0 |

| | | | | |
|---|---|---|---|---|
| 3-2 | Priority Scheme select | R/W | 00 = always deliver high priority packets first<br>01 = deliver high/low packets at ratio 10/1<br>10 = deliver high/low packets at ratio 5/1<br>11 = deliver high/low packets at ratio 2/1 | 00 |
| 1 | Reserved | R/W | | 0 |
| 0 | Sniff mode select | R./W | = 1, will do rx AND tx sniff (both source port and destination port need to match)<br>= 0, will do rx OR tx sniff (Either source port or destination port needs to match). This is the mode used to implement rx only sniff. | 0 |

### *7.1.7 Register 6 (0x06): Global Control 4*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | | 0 |
| 6 | Switch MII half duplex mode | R/W | = 1, enable MII interface half duplex mode.<br>= 0, enable MII interface full duplex mode. | Pin SMRXD2 strap option.<br>Pull down(0): Full duplex mode<br>Pull up(1): Half duplex mode<br>Note: SMRXD2 has internal pull down |
| 5 | Switch MII flow control enable | R/W | = 1, enable full duplex flow control on Switch MII interface.<br>= 0, disable full duplex flow control on Switch MII interface. | Pin SMRXD3 strap option.<br>Pull down(0): Disable flow control<br>Pull up(1): Enable flow control<br>Note: SMRXD3 has internal pull down |
| 4 | Switch MII 10BT | R/W | = 1, the switch interface is in 10Mbps mode<br>= 0, the switch interface is in 100Mbps mode | Pin SMRXD1 strap option.<br>Pull down(0): Enable 100Mbps<br>Pull up(1): Enable 10Mpbs<br>Note: SMRXD1 has internal pull down |
| 3 | Null VID replacement | R/W | = 1, will replace NULL VID with port VID(12 bits)<br>= 0, no replacement for NULL VID | 0 |

| | | | | |
|---|---|---|---|---|
| 2-0 | Broadcast storm protection rate Bit [10:8] | R/W | This register along with the next register determines how many “64 byte blocks” of packet data allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%. | 000 |

### 7.1.8 Register 7 (0x07): Global Control 5

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Broadcast storm protection rate Bit [7:0] | R/W | This register along with the previous register determines how many “64 byte blocks” of packet data are allowed on an input port in a preset period. The period is 67ms for 100BT or 500ms for 10BT. The default is 1%. | 0x63 |

***Rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx.) = 0x63***

### 7.1.9 Register 8 (0x08): Global Control 6

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved | 0x4E |

### 7.1.10 Register 9 (0x09): Global Control 7

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved | 0x24 |

### 7.1.11 Register 10 (0x0A): Global Control 8

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved | 0x24 |

### 7.1.12 Register 11 (0x0B): Global Control 9

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | | Reserved | 0 |
| 6 | PHY power save | R/W | = 1, enable PHY power save mode<br>= 0, disable PHY power save mode | 0 |
| 5 | Reserved | R/W | Reserved | 0 |
| 4 | Reserved | RW | Testing mode, must be 0 | 0 |
| 3 | Reserved | R/W | Reserved | 1 |
| 2 | Reserved | R/W | Reserved | 0 |

<table>
<tr>
<td>1</td>
<td>LED mode</td>
<td>R/W</td>
<td>This register bit sets the LEDSEL0 selection only. LEDSEL1 is set via strap-in pin.<br><br>Port x LED Indicators, defined as below:<br><br>
<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[0, 0]</th><th>[0, 1]</th></tr>
<tr><td>PxLED3</td><td>------</td><td>------</td></tr>
<tr><td>PxLED2</td><td>LINK/ACT</td><td>100LINK/ACT</td></tr>
<tr><td>PxLED1</td><td>FULL_DPX/COL</td><td>10LINK/ACT</td></tr>
<tr><td>PxLED0</td><td>SPEED</td><td>FULL_DPX</td></tr>
</table>
<br>
<table>
<tr><th></th><th colspan="2">[LEDSEL1, LEDSEL0]</th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>PxLED3</td><td>ACT</td><td>------</td></tr>
<tr><td>PxLED2</td><td>LINK</td><td>------</td></tr>
<tr><td>PxLED1</td><td>FULL_DPX/COL</td><td>------</td></tr>
<tr><td>PxLED0</td><td>SPEED</td><td>------</td></tr>
</table>
<br>Notes:<br>LEDSEL0 is external strap-in pin #70.<br>LEDSEL1 is external strap-in pin #23.</td>
<td>LEDSEL0 pin value during reset</td>
</tr>
<tr>
<td>0</td>
<td>Special TPID mode</td>
<td>R/W</td>
<td>Used for direct mode forwarding from port 3. See description in “spanning tree” functional description.<br><br>0 = disable<br>1 = enable</td>
<td>0</td>
</tr>
</table>

### *7.1.13 Register 12 (0x0C): Reserved Register*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Reserved | | Reserved | 0x00 |

### *7.1.14 Register 13 (0x0D): User Defined Register 1*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | UDR1 | R/W | | 0x00 |

### *7.1.15 Register 14 (0x0E): User Defined Register 2*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | UDR2 | R/W | | 0x00 |

### *7.1.16 Register 15 (0x0F): User Defined Register 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | UDR3 | R/W | | 0x00 |

## 7.2 Port Registers

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

### *7.2.1 Register 16 (0x10): Port 1 Control 0*
### *Register 32 (0x20): Port 2 Control 0*
### *Register 48 (0x30): Port 3 Control 0*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Broadcast storm protection enable | R/W | = 1, enable broadcast storm protection for ingress packets on the port<br>= 0, disable broadcast storm protection | 0 |
| 6 | Diffserv priority classification enable | R/W | = 1, enable diffserv priority classification for ingress packets on port<br>= 0, disable diffserv function | 0 |
| 5 | 802.1p priority classification enable | R/W | = 1, enable 802.1p priority classification for ingress packets on port<br>= 0, disable 802.1p | Pin value during reset:<br>**P1_1PEN (port 1), P2_1PEN (port 2), P3_1PEN (port 3)** |
| 4 | Port based priority classification enable | R/W | = 1, ingress packets on the port will be classified as high priority if "Diffserv" or "802.1p" classification is not enabled or fails to classify.<br>= 0, ingress packets on port will be classified as low priority if "Diffserv" or "802.1p" classification is not enabled or fails to classify.<br><br>**Note:** "Diffserv", "802.1p" and port priority can be enabled at the same time. The OR'ed result of 802.1p and DSCP overwrites the port priority. | Pin value during reset:<br>**P1_PP (port 1), P2_PP (port 2), P3_PP (port 3)** |
| 3 | User Priority Ceiling | R/W | = 1, if the packet's "user priority field" is greater than the "user priority field" in the port default tag register, replace the packet's "user priority field" with the "user priority field" in the port default tag register.<br>= 0, do no compare and replace the packet's 'user priority field" | 0 |
| 2 | Tag insertion | R/W | = 1, when packets are output on the port, the switch will add 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port's "port VID".<br>= 0, disable tag insertion | Pin value during reset:<br>**P1_TAGINS (port 1), P2_TAGINS (port 2), P3_TAGINS (port 3)** |

| | | | | |
|---|---|---|---|---|
| 1 | Tag removal | R/W | = 1, when packets are output on the port, the switch will remove 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags.<br>= 0, disable tag removal | Pin value during reset:<br>**P1_TAGRM (port 1), P2_TAGRM (port 2), P3_TAGRM (port 3)** |
| 0 | Priority Enable | R/W | = 1, the port output queue is split into high and low priority queues.<br>= 0, single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority. | Pin value during reset:<br>**P1_TXQ2 (port 1), P2_TXQ2 (port 2), P3_TXQ2 (port 3)** |

### *7.2.2 Register 17 (0x11): Port 1 Control 1*
### *Register 33 (0x21): Port 2 Control 1*
### *Register 49 (0x31): Port 3 Control 1*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Sniffer port | R/W | = 1, Port is designated as sniffer port and will transmit packets that are monitored.<br>= 0, Port is a normal port | 0 |
| 6 | Receive sniff | R/W | = 1, All the packets received on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port"<br>= 0, no receive monitoring | 0 |
| 5 | Transmit sniff | R/W | = 1, All the packets transmitted on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port"<br>= 0, no transmit monitoring | 0 |
| 4 | Double tag | R/W | = 1, all packets will be tagged with port default tag of ingress port regardless of the original packets are tagged or not<br>= 0, do not double tagged on all packets | 0x0 |
| 3 | Reserved | R/W | | 0x0 |
| 2-0 | Port VLAN membership | R/W | Define the port's " egress port VLAN membership. Bit 2 stands for port 3, bit 1 for port 2… bit 0 for port 1. The Port can only communicate within the membership. A '1' includes a port in the membership, a '0' excludes a port from membership. | Pin value during reset:<br>For port 1,<br>**(PV13, PV12, 1)**<br>For port 2,<br>**(PV23, 1, PV21)**<br>For port 3,<br>**(1, PV32, PV31)** |

### *7.2.3 Register 18 (0x12): Port 1 Control 2*
### *Register 34 (0x22): Port 2 Control 2*
### *Register 50 (0x32): Port 3 Control 2*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | | Reserved | 0 |

| | | | | |
|---|---|---|---|---|
| 6 | Ingress VLAN filtering | R/W | = 1, the switch will discard packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port.<br>= 0, no ingress VLAN filtering. | 0 |
| 5 | Discard Non PVID packets | R/W | = 1, the switch will discard packets whose VID does not match ingress port default VID.<br>= 0, no packets will be discarded | 0 |
| 4 | Force flow control | R/W | = 1, will always enable flow control on the port, regardless of AN result.<br><br>= 0, the flow control is enabled based on AN result. | Pin value during reset:<br><br>For port 1,<br>**P1FFC pin**<br><br>For port 2,<br>**P2FFC pin**<br><br>For port 3, this bit has no meaning. Flow control is controlled by<br>**Reg. 6, bit 5** |
| 3 | Back pressure enable | R/W | = 1, enable port's half duplex back pressure<br>= 0, disable port's half duplex back pressure. | Pin value during reset:<br><br>**BPEN pin** |
| 2 | Transmit enable | R/W | = 1, enable packet transmission on the port<br>= 0, disable packet transmission on the port | 1 |
| 1 | Receive enable | R/W | = 1, enable packet reception on the port<br>= 0, disable packet reception on the port | 1 |
| 0 | Learning disable | R/W | = 1, disable switch address learning capability<br>= 0, enable switch address learning | 0 |

**(Note: Bits [2:0] are used for Spanning Tree support. See section 5.1)**

### *7.2.4 Register 19 (0x13): Port 1 Control 3*
### *Register 35 (0x23): Port 2 Control 3*
### *Register 51 (0x33): Port 3 Control 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Default tag [15:8] | R/W | Port's default tag, containing<br>7-5 : User Priority bits<br>4 : CFI bit<br>3-0 : VID[11:8] | 0x00 |

### *7.2.5 Register 20 (0x14): Port 1 Control 4*
### *Register 36 (0x24): Port 2 Control 4*
### *Register 52 (0x34): Port 3 Control 4*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Default tag [7:0] | R/W | Port's default tag, containing<br>7-0: VID[7:0] | 0x01 |

**Note: Registers 19 and 20 (and those corresponding to other ports) serve two purposes:**
**(1) Associated with the ingress untagged packets, and used for egress tagging.**

**(2) Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.**

### *7.2.6 Register 21 (0x15): Port 1 Control 5*
### *Register 37 (0x25): Port 2 Control 5*
### *Register 53 (0x35): Port 3 Control 5*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Transmit high priority rate control [7:0] | R/W | This register along with port control 7, bits [3:0] form a 12-bits field to determine how many “32Kbps” high priority blocks can be transmitted. (in a unit of 4K bytes in a one second period) | 0x00 |

### *7.2.7 Register 22 (0x16): Port 1 Control 6*
### *Register 38 (0x26): Port 2 Control 6*
### *Register 54 (0x36): Port 3 Control 6*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Transmit low priority rate control [7:0] | R/W | This register along with port control 7, bits [7:4] form a 12-bits field to determine how many “32Kbps” low priority blocks can be transmitted. (in a unit of 4K bytes in a one second period) | 0x00 |

### *7.2.8 Register 23 (0x17): Port 1 Control 7*
### *Register 39 (0x27): Port 2 Control 7*
### *Register 55 (0x37): Port 3 Control 7*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-4 | Transmit low priority rate control [11:8] | R/W | These bits along with port control 6, bits [7:0] form a 12-bits field to determine how many “32Kbps” low priority blocks can be transmitted. (in a unit of 4K bytes in a one second period) | 0x0 |
| 3-0 | Transmit high priority rate control [11:8] | R/W | These bits along with port control 5, bits [7:0] form a 12-bits field to determine how many “32Kbps” high priority blocks can be transmitted. (in a unit of 4K bytes in a one second period) | 0x0 |

### *7.2.9 Register 24 (0x18): Port 1 Control 8*
### *Register 40 (0x28): Port 2 Control 8*
### *Register 56 (0x38): Port 3 Control 8*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Receive high priority rate control [7:0] | R/W | This register along with port control 10, bits [3:0] form a 12-bits field to determine how many “32Kbps” high priority blocks can be received. (in a unit of 4K bytes in a one second period) | 0x00 |

### 7.2.10 Register 25 (0x19): Port 1 Control 9
### Register 41 (0x29): Port 2 Control 9
### Register 57 (0x39): Port 3 Control 9

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Receive low priority rate control [7:0] | R/W | This register along with port control 10, bits [7:4] form a 12-bits field to determine how many "32Kbps" low priority blocks can be received. (in a unit of 4K bytes in a one second period) | 0x00 |

### 7.2.11 Register 26 (0x1A): Port 1 Control 10
### Register 42 (0x2A): Port 2 Control 10
### Register 58 (0x3A): Port 3 Control 10

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-4 | Receive low priority rate control [11:8] | R/W | These bits along with port control 9, bits [7:0] form a 12-bits field to determine how many "32Kbps" low priority blocks can be received. (in a unit of 4K bytes in a one second period) | 0x0 |
| 3-0 | Receive high priority rate control [11:8] | R/W | These bits along with port control 8, bits [7:0] form a 12-bits field to determine how many "32Kbps" high priority blocks can be received. (in a unit of 4K bytes in a one second period) | 0x0 |

### 7.2.12 Register 27 (0x1B): Port 1 Control 11
### Register 43 (0x2B): Port 2 Control 11
### Register 59 (0x3B): Port 3 Control 11

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Receive differential priority rate control | R/W | = 1, If bit 6 is also '1' this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also '1', this will enable receive rate control on high priority packets at the high priority rate.<br>= 0, receive rate control will be based on the low priority rate for all packets on this port. | 0 |
| 6 | Low priority receive rate control enable | R/W | = 1, enable port's low priority receive rate control feature<br>= 0, disable port's low priority receive rate control. | 0 |
| 5 | High priority receive rate control enable | R/W | = 1, If bit 7 is also '1' this will enable the port's high priority receive rate control feature. If bit 7 is a '0' and bit 6 is a '1', all receive packets on this port will be rate controlled at the low priority rate.<br>= 0, disable port's high priority receive rate control feature | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | Low priority receive rate flow control enable | R/W | = 1, flow control may be asserted if the port's low priority receive rate is exceeded.<br>= 0, flow control is not asserted if the port's low priority receive rate is exceeded. | 0 |
| 3 | High priority receive rate flow control enable | R/W | = 1, flow control may be asserted if the port's high priority receive rate is exceeded.<br>(to use this, differential receive rate control must be on)<br>= 0, flow control is not asserted if the port's high priority receive rate is exceeded. | 0 |
| 2 | Transmit differential priority rate control | R/W | = 1, will do transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets respectively.<br>= 0, will do transmit rate control on any packets. The rate counters defined in low priority will be used. | 0 |
| 1 | Low priority transmit rate control enable | R/W | = 1, enable the port's low priority transmit rate control feature<br>= 0, disable the port's low priority transmit rate control feature | 0 |
| 0 | High priority transmit rate control enable | R/W | = 1, enable the port's high priority transmit rate control feature<br>= 0, disable the port's high priority transmit rate control feature | 0 |

**NOTE: Port Control 12 and 13, and Port Status 0 contents can also be accessed with the MIIM (MDC/MDIO) interface via the standard MIIM registers.**

### *7.2.13 Register 28 (0x1C): Port 1 Control 12*
### *Register 44 (0x2C): Port 2 Control 12*
### *Register 60 (0x3C): Reserved, not applied to port 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Auto Negotiation Enable | R/W | = 0, disable auto negotiation, speed and duplex are decided by bit 6 and 5 of the same register.<br>= 1, auto negotiation is on | For port 1, P1ANEN pin value during reset<br><br>For port 2, P2ANEN pin value during reset |

| | | | | |
|---|---|---|---|---|
| 6 | Force Speed | R/W | =1, forced 100BT if AN is disabled (bit 7)<br>=0, forced 10BT if AN is disabled (bit 7) | For port 1, P1SPD pin value during reset.<br><br>For port 2, P2SPD pin value during reset |
| 5 | Force duplex | R/W | = 1, forced full duplex if (1) AN is disabled or (2) AN is enabled but failed.<br>= 0, forced half duplex if (1) AN is disabled or (2) AN is enabled but failed. | For port 1, P1DPX pin value during reset.<br><br>For port 2, P2DPX pin value during reset |
| 4 | Advertised flow control capability | R/W | = 1, advertise flow control (pause) capability<br>= 0, suppress flow control (pause) capability from transmission to link partner | ADVFC pin value during reset |
| 3 | Advertised 100BT Full duplex capability | R/W | = 1, advertise 100BT Full duplex capability<br>= 0, suppress 100BT Full duplex capability from transmission to link partner | 1 |
| 2 | Advertised 100BT half duplex capability | R/W | = 1, advertise 100BT half duplex capability<br>= 0, suppress 100BT half duplex capability from transmission to link partner | 1 |
| 1 | Advertised 10BT Full duplex capability | R/W | = 1, advertise 10BT Full duplex capability<br>= 0, suppress 10BT Full duplex capability from transmission to link partner | 1 |
| 0 | Advertised 10BT half duplex capability | R/W | = 1, advertise 10BT half duplex capability<br>= 0, suppress 10BT half duplex capability from transmission to link partner | 1 |

### *7.2.14 Register 29 (0x1D): Port 1 Control 13*
### *Register 45 (0x2D): Port 2 Control 13*
### *Register 61 (0x3D): Reserved, not applied to port 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | LED off | R/W | = 1, Turn off all port's LEDs (LEDx_3, LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one.<br>= 0, normal operation | 0 |
| 6 | Txids | R/W | = 1, disable port's transmitter<br>= 0, normal operation | 0 |
| 5 | Restart AN | R/W | = 1, restart auto-negotiation<br>= 0, normal operation | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | Disable Far end fault | R/W | = 1, disable far end fault detection & pattern transmission.<br>= 0, enable far end fault detection & pattern transmission | 0 |
| 3 | Power down | R/W | = 1, power down<br>= 0, normal operation | 0 |
| 2 | Disable auto MDI/MDIX | R/W | = 1, disable auto MDI/MDIX function<br>= 0, enable auto MDI/MDIX function | 0 |
| 1 | Force MDIX | R/W | = 1, If auto MDI/MDIX is disabled, force PHY into MDIX mode<br>= 0, Do not force PHY into MDIX mode | 0 |
| 0 | Loop back | R/W | = 1, perform loop back, as indicated:<br><br>**Port 1 Loop back (reg. 29, bit 0 = '1')**<br>Start: RXP2/RXM2 (port 2)<br>Loop back: PMD/PMA of port 1's PHY<br>End: TXP2/TXM2 (port 2)<br><br>**Port 2 Loop back (reg. 45, bit 0 = '1')**<br>Start: RXP1/RXM1 (port 1)<br>Loop back: PMD/PMA of port 2's PHY<br>End: TXP1/TXM1 (port 1)<br><br>= 0, normal operation | 0 |

### *7.2.15 Register 30 (0x1E): Port 1 Status 0*
### *Register 46 (0x2E): Port 2 Status 0*
### *Register 62 (0x3E): Reserved, not applied to port 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | MDIX status | RO | = 1, MDI-X<br>= 0, MDI | 0 |
| 6 | AN done | RO | = 1, AN done<br>= 0, AN not done | 0 |
| 5 | Link good | RO | = 1, Link good<br>= 0, Link not good | 0 |
| 4 | Partner flow control capability | RO | = 1, link partner flow control (pause) capable<br>= 0, link partner not flow control (pause) capable | 0 |
| 3 | Partner 100BT full duplex capability | RO | = 1, link partner 100BT full duplex capable<br>= 0, link partner not 100BT full duplex capable | 0 |
| 2 | Partner 100BT half duplex capability | RO | = 1, link partner 100BT half duplex capable<br>= 0, link partner not 100BT half duplex capable | 0 |
| 1 | Partner 10BT full duplex capability | RO | = 1, link partner 10BT full duplex capable<br>= 0, link partner not 10BT full duplex capable | 0 |
| 0 | Partner 10BT half duplex capability | RO | = 1, link partner 10BT half duplex capable<br>= 0, link partner not 10BT half duplex capable | 0 |

### *7.2.16 Register 31 (0x1F): Port 1 Status 1*
### *Register 47 (0x2F): Port 2 Status 1*
### *Register 63 (0x3F): Port 3 Status 1*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | | 0 |
| 6-5 | Reserved | RO | | 00 |
| 4 | Receive flow control enable | RO | 1 = Receive flow control feature is active<br>0 = Receive flow control feature is inactive | 0 |
| 3 | Transmit flow control enable | RO | 1 = transmit flow control feature is active<br>0 = transmit flow control feature is inactive | 0 |
| 2 | Operation Speed | RO | 1 = link speed is 100Mbps<br>0 = link speed is 10Mbps | 0 |
| 1 | Operation duplex | RO | 1 = link duplex is full<br>0 = link duplex is half | 0 |
| 0 | Far end fault | RO | = 1, Far end fault status detected.<br>= 0, no far end fault status detected. | 0<br>Note: only port 1 supports fiber, this bit is applicable to port 1 only |

## 7.3 Advanced Control Registers

The IPv4 TOS priority control registers implement a fully decoded 64 bit DSCP (Differentiated Services Code Point) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.

### *7.3.1 Register 96 (0x60): TOS priority control register 0*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[63:56] | R/W | | 0000_0000 |

### *7.3.2 Register 97 (0x61): TOS priority control register 1*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[55:48] | R/W | | 0000_0000 |

### *7.3.3 Register 98 (0x62): TOS priority control register 2*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[47:40] | R/W | | 0000_0000 |

### *7.3.4 Register 99 (0x63): TOS priority control register 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[39:32] | R/W | | 0000_0000 |

### 7.3.5 Register 100 (0x64): TOS priority control register 4

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[31:24] | R/W | | 0000_0000 |

### 7.3.6 Register 101 (0x65): TOS priority control register 5

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[23:16] | R/W | | 0000_0000 |

### 7.3.7 Register 102 (0x66): TOS priority control register 6

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[15:8] | R/W | | 0000_0000 |

### 7.3.8 Register 103 (0x67): TOS priority control register 7

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | DSCP[7:0] | R/W | | 0000_0000 |

**Registers 104 to 109 define the switching engine's MAC address. This 48-bit address is used as the source address in MAC pause control frames.**

### 7.3.9 Register 104 (0x68): MAC address register 0

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[47:40] | R/W | | 0x00 |

### 7.3.10 Register 105 (0x69): MAC address register 1

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[39:32] | R/W | | 0x10 |

### 7.3.11 Register 106 (0x6A): MAC address register 2

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[31:24] | R/W | | 0xA1 |

### 7.3.12 Register 107 (0x6B): MAC address register 3

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[23:16] | R/W | | 0xFF |

### 7.3.13 Register 108 (0x6C): MAC address register 4

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[15:8] | R/W | | 0xFF |

### 7.3.14 Register 109 (0X6D): MAC address register 5

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | MACA[7:0] | R/W | | 0xFF |

**Use registers 110 and 111 to read or write data to the static MAC address table, VLAN table, dynamic address table, or the MIB counters.**

### *7.3.15 Register 110 (0x6E): Indirect Access Control 0*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-5 | Reserved | R/W | Reserved | 000 |
| 4 | Read High Write Low | R/W | = 1, read cycle<br>= 0, write cycle | 0 |
| 3-2 | Table select | R/W | 00 = static MAC address table selected<br>01 = VLAN table selected<br>10 = dynamic address table selected<br>11 = MIB counter selected | 00 |
| 1-0 | Indirect address high | R/W | Bit 9-8 of indirect address | 00 |

### *7.3.16 Register 111 (0x6F): Indirect Access Control 1*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect address low | R/W | Bit 7-0 of indirect address | 0000_0000 |

**Note: (1) write to register 111 will actually trigger a command.**
**Read or write access is determined by Register 110 bit 4.**

### *7.3.17 Register 112 (0x70): Indirect Data register 8*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 68-64 | Indirect data | R/W | Bit 68-64 of indirect data | 0_0000 |

### *7.3.18 Register 113 (0x71): Indirect Data register 7*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 63-56 | Indirect data | R/W | Bit 63-56 of indirect data | 0000_0000 |

### *7.3.19 Register 114 (0x72): Indirect Data register 6*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 55-48 | Indirect data | R/W | Bit 55-48 of indirect data | 0000_0000 |

### *7.3.20 Register 115 (0x73): Indirect Data register 5*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47-40 | Indirect data | R/W | Bit 47-40 of indirect data | 0000_0000 |

### *7.3.21 Register 116 (0x74): Indirect Data register 4*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 39-32 | Indirect data | R/W | Bit 39-32 of indirect data | 0000_0000 |

### *7.3.22 Register 117 (0x75): Indirect Data register 3*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31-24 | Indirect data | R/W | Bit of 31-24 of indirect data | 0000_0000 |

### 7.3.23 Register 118 (0x76): Indirect Data register 2

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 23-16 | Indirect data | R/W | Bit 23-16 of indirect data | 0000_0000 |

### 7.3.24 Register 119 (0x77): Indirect Data register 1

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15-8 | Indirect data | R/W | Bit 15-8 of indirect data | 0000_0000 |

### 7.3.25 Register 120 (0x78): Indirect Data register 0

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Indirect data | R/W | Bit 7-0 of indirect data | 0000_0000 |

**DO NOT READ/WRITE TO/FROM REGISTERS 121 TO 127.**
**DOING SO MAY PREVENT PROPER OPERATION.**
**MICREL INTERNAL TESTING ONLY**

### 7.3.26 Register 121 (0x79): Digital Testing Status 0

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | RO | Reserved<br>Qm_split status | 0x00 |

### 7.3.27 Register 122 (0x7A): Digital Testing Status 1

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | RO | Reserved<br>Dbg[7:0] | 0x00 |

### 7.3.28 Register 123 (0x7B): Digital Testing Control 0

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved<br>Dbg[12:8] | 0x00 |

### 7.3.29 Register 124 (0x7C): Digital Testing Control 1

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved | 0x00 |

### 7.3.30 Register 125 (0x7D): Analog Testing Control 0

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved | 0x00 |

### 7.3.31 Register 126 (0x7E): Analog Testing Control 1

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | R/W | Reserved | 0x00 |

### 7.3.32 Register 127 (0x7F): Analog Testing Status

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7-0 | Factory testing | RO | Reserved | 0x00 |

### 7.3.33 Static MAC Address Table

The KS8993M has both a static and a dynamic MAC address table. When a Destination Address (DA) look up is requested, both tables are searched to make a packet forwarding decision. When a Source Address (SA) look up is requested, only the dynamic table is searched for aging, migration and learning purposes. The static DA look up result will have precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table will be used. The static table can be accessed and controlled by an external processor via the SMI, SPI and I2C interfaces. The external processor performs all addition, modification and deletion of static table entries. These entries in the static table will not be aged out by the KS8993M.

### Format of Static MAC Table (8 Entries)

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 57-54 | FID | R/W | Filter VLAN ID, representing one of the 16 active VLANs | 0000 |
| 53 | Use FID | R/W | = 1, use (FID+MAC) to look up in static table<br>= 0, use MAC only to look up in static table | 0 |
| 52 | Override | R/W | = 1, override port setting “transmit enable=0” or “receive enable=0” setting.<br>= 0, no override | 0 |
| 51 | Valid | R/W | = 1, this entry is valid, the look up result will be used<br>= 0, this entry is not valid | 0 |
| 50-48 | Forwarding ports | R/W | These 3 bits control the forwarding port(s):<br>001, forward to port 1<br>010, forward to port 2<br>100, forward to port 3<br>011, forward to port 1 and port 2<br>110, forward to port 2 and port 3<br>101, forward to port 1 and port 3<br>111, broadcasting (excluding the ingress port) | 000 |
| 47-0 | MAC address | R/W | 48 bits MAC Address | 0x0000_0000_0000 |

**Examples:**

**(1) Static Address Table Read (read the 2nd entry)**

Write to reg. 110 with 0x10 (read static table selected)
Write to reg. 111 with 0x01 (trigger the read operation)
Then
Read reg. 113 (57-56)
Read reg. 114 (55-48)
Read reg. 115 (47-40)
Read reg. 116 (39-32)
Read reg. 117 (31-24)

Read reg. 118 (23-16)
Read reg. 119 (15-8)
Read reg. 120 (7-0)

**(2) Static Address Table Write (write the 8th entry)**

Write reg. 113 (57-56)
Write reg. 114 (55-48)
Write reg. 115 (47-40)
Write reg. 116 (39-32)
Write reg. 117 (31-24)
Write reg. 118 (23-16)
Write reg. 119 (15-8)
Write reg. 120 (7-0)
Write to reg. 110 with 0x00 (write static table selected)
Write to reg. 111 with 0x07 (trigger the write operation)

### *7.3.34 VLAN Table*

VLAN table is used to do VLAN table look up. If 802.1Q VLAN mode is enabled (Register 5, Bit 7 = 1), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (filter ID), VID (VLAN ID), and VLAN membership as described below:

***Format of Static VLAN Table (16 Entries)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 19 | Valid | R/W | = 1, the entry is valid<br>= 0, entry is invalid | 1 |
| 18-16 | Membership | R/W | Specify which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. E.g. 101 means port 3 and 1 are in this VLAN. | 111 |
| 15-12 | FID | R/W | Filter ID. KS8993M supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA. | 0x0 |
| 11-0 | VID | R/W | IEEE 802.1Q 12 bits VLAN ID | 0x001 |

If 802.1Q VLAN mode is enabled, KS8993M will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

**Examples:**

**(1) VLAN Table Read (read the 3rd entry)**

Write to reg. 110 with 0x14 (read VLAN table selected)
Write to reg. 111 with 0x02 (trigger the read operation)
Then
Read reg. 118 (VLAN table bits 19-16)
Read reg. 119 (VLAN table bits 15-8)
Read reg. 120 (VLAN table bits 7-0)

**(2) VLAN Table Write (write the 7th entry)**

Write to reg. 118 (VLAN table bits 19-16)
Write to reg. 119 (VLAN table bits 15-8)
Write to reg. 120 (VLAN table bits 7-0)
Write to reg. 110 with 0x04 (write VLAN table selected)
Write to reg. 111 with 0x06 (trigger the write operation)

### *7.3.35 Dynamic MAC Address Table*

**This table is read only. The table contents are maintained by KS8993M only.**

### *Format of Dynamic MAC Address Table (1K Entries)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 71 | Data not ready | RO | = 1, entry is not ready, retry until this bit is set to 0<br>= 0, entry is ready | |
| 70-67 | Reserved | RO | Reserved | |
| 66 | MAC empty | RO | = 1, there is no valid entry in the table<br>= 0, there are valid entries in the table | 1 |
| 65-56 | No of valid entries | RO | Indicates how many valid entries in the table<br>0x3ff means 1 K entries<br>0x001 means 2 entries<br>0x000 and bit 66 = 0 means 1 entry<br>0x000 and bit 66 = 1 means 0 entry | 00_0000_0000 |
| 55-54 | Time Stamp | RO | 2 bits counter for internal aging | |
| 53-52 | Source port | RO | The source port where FID+MAC is learned<br>00, port 1<br>01, port 2<br>10, port 3 | 00 |
| 51-48 | FID | RO | Filter ID | 0x0 |
| 47-0 | MAC Address | RO | 48 bits MAC address | 0x0000_0000_0000 |

**Example:**

**Dynamic MAC Address Table Read (read the 1st entry and retrieve the MAC Table size)**

Write to reg. 110 with 0x18 (read dynamic table selected)
Write to reg. 111 with 0x00 (trigger the read operation)
Then
Read reg. 112 (71-64) // if bit 71 = 1, restart (reread) from this register
Read reg. 113 (63-56)
Read reg. 114 (55-48)
Read reg. 115 (47-40)

Read reg. 116 (39-32)
Read reg. 117 (31-24)
Read reg. 118 (23-16)
Read reg. 119 (15-8)
Read reg. 120 (7-0)

### *7.3.36 MIB (Management Information Base) Counters*

**The KS8993M provides 34 MIB counters per port. These counters are used to monitor the port activity for network management. The MIB counters have two format groups: "Per Port" and "All Port Dropped Packet".**

### *Format of "Per Port" MIB Counters*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31 | Overflow | RO | = 1, Counter overflow<br>= 0, No Counter overflow | 0 |
| 30 | Count Valid | RO | = 1, Counter value is valid<br>= 0, Counter value is not valid | 0 |
| 29-0 | Counter Values | RO | Counter value | 0 |

**"Per Port" MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:**

**Port 1, base is 0x00 and range is (0x00-0x1f)**
**Port 2, base is 0x20 and range is (0x20-0x3f)**
**Port 3, base is 0x40 and range is (0x40-0x5f)**

**Port 1's "Per Port" MIB Counters Indirect Memory Offsets are shown in the following table:**

**Table 12: Port 1's "Per Port" MIB Counters Indirect Memory Offsets**

| Offset | Counter Name | Description |
|---|---|---|
| 0x0 | **RxLoPriorityByte** | Rx lo-priority (default) octet count including bad packets |
| 0x1 | **RxHiPriorityByte** | Rx hi-priority octet count including bad packets |
| 0x2 | **RxUndersizePkt** | Rx undersize packets w/ good CRC |
| 0x3 | **RxFragments** | Rx fragment packets w/ bad CRC, symbol errors or alignment errors |
| 0x4 | **RxOversize** | Rx oversize packets w/ good CRC (max: 1536 or 1522 bytes) |
| 0x5 | **RxJabbers** | Rx packets longer than 1522 bytes w/ either CRC errors, Alignment errors, or symbol errors. (Depends on max packet size setting). |
| 0x6 | **RxSymbolError** | Rx packets w/ invalid data symbol and legal packet size. |

| | | |
|---|---|---|
| 0x7 | **RxCRCError** | Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (Upper limit depends on max packet size setting). |
| 0x8 | **RxAlignmentError** | Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (Upper limit depends on max packet size setting). |
| 0x9 | **RxControl8808Pkts** | The number of MAC control frames received by a port with 88-08h in EtherType field. |
| 0xA | **RxPausePkts** | The number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC |
| 0xB | **RxBroadcast** | Rx good broadcast packets (not including error broadcast packets or valid multicast packets) |
| 0xC | **RxMulticast** | Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets) |
| 0xD | **RxUnicast** | Rx good unicast packets |
| 0xE | **Rx64Octets** | Total Rx packets (bad packets included) that were 64 octets in length |
| 0xF | **Rx65to127Octets** | Total Rx packets (bad packets included) that are between 65 and 127 octets in length |
| 0x10 | **Rx128to255Octets** | Total Rx packets (bad packets included) that are between 128 and 255 octets in length |
| 0x11 | **Rx256to511Octets** | Total Rx packets (bad packets included) that are between 256 and 511 octets in length |
| 0x12 | **Rx512to1023Octets** | Total Rx packets (bad packets included) that are between 512 and 1023 octets in length |
| 0x13 | **Rx1024to1522Octets** | Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (Upper limit depends on max packet size setting). |
| 0x14 | **TxLoPriorityByte** | Tx lo-priority good octet count, including PAUSE packets |
| 0x15 | **TxHiPriorityByte** | Tx hi-priority good octet count, including PAUSE packets |
| 0x16 | **TxLateCollision** | The number of times a collision is detected later than 512 bit-times into the Tx of a packet. |
| 0x17 | **TxPausePkts** | The number of PAUSE frames transmitted by a port |
| 0x18 | **TxBroadcastPkts** | Tx good broadcast packets (not including error broadcast or valid multicast packets) |
| 0x19 | **TxMulticastPkts** | Tx good multicast packets (not including error multicast packets or valid broadcast packets) |

| | | |
|---|---|---|
| 0x1A | **TxUnicastPkts** | Tx good unicast packets |
| 0x1B | **TxDeferred** | Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium |
| 0x1C | **TxTotalCollision** | Tx total collision, half duplex only |
| 0x1D | **TxExcessiveCollision** | A count of frames for which Tx fails due to excessive collisions |
| 0x1E | **TxSingleCollision** | Successfully Tx frames on a port for which Tx is inhibited by exactly one collision |
| 0x1F | **TxMultipleCollision** | Successfully Tx frames on a port for which Tx is inhibited by more than one collision |

### *Format of "All Port Dropped Packet" MIB Counters*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 30-16 | Reserved | N/A | Reserved | N/A |
| 15-0 | Counter values | RO | Counter value | 0 |

**Note: "All Port Dropped Packet" MIB Counters do not indicate overflow or validity; therefore the application must keep track of overflow and valid conditions.**

**"All Port Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in the following table:**

### Table 13: "All Port Dropped Packet" MIB Counters Indirect Memory Offsets

| Offset | Counter Name | Description |
|---|---|---|
| 0x100 | **Port1 TX Drop Packets** | TX packets dropped due to lack of resources |
| 0x101 | **Port2 TX Drop Packets** | TX packets dropped due to lack of resources |
| 0x102 | **Port3 TX Drop Packets** | TX packets dropped due to lack of resources |
| 0x103 | **Port1 RX Drop Packets** | RX packets dropped due to lack of resources |
| 0x104 | **Port2 RX Drop Packets** | RX packets dropped due to lack of resources |
| 0x105 | **Port3 RX Drop Packets** | RX packets dropped due to lack of resources |

**Examples:**

**(1) MIB counter read (read port 1 "Rx64Octets" counter)**

Write to reg. 110 with 0x1c (read MIB counters selected)
Write to reg. 111 with 0x0e (trigger the read operation)
Then
Read reg. 117 (counter value 31-24) // If bit 31 = 1, there was a counter overflow
// If bit 30 = 0, restart (reread) from this register
Read reg. 118 (counter value 23-16)
Read reg. 119 (counter value 15-8)
Read reg. 120 (counter value 7-0)

**(2) MIB counter read (read port 2 "Rx64Octets" counter)**

Write to reg. 110 with 0x1c (read MIB counter selected)
Write to reg. 111 with 0x2e (trigger the read operation)
Then
Read reg. 117 (counter value 31-24) // If bit 31 = 1, there was a counter overflow
// If bit 30 = 0, restart (reread) from this register
Read reg. 118 (counter value 23-16)
Read reg. 119 (counter value 15-8)
Read reg. 120 (counter value 7-0)

**(3) MIB counter read (read "Port1 TX Drop Packets" counter)**

Write to reg. 110 with 0x1d (read MIB counter selected)
Write to reg. 111 with 0x00 (trigger the read operation)
Then
Read reg. 119 (counter value 15-8)
Read reg. 120 (counter value 7-0)

***NOTE:***

To read out all the counters, the best performance over the SPI bus is (160+3)*8*200 = 260 ms, where there are 160 registers, 3 overheads, 8 clocks per access, **at 5 MHz**. In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds.

A high performance SPI master is also recommended to prevent counters overflow.

**Per Port MIB counters** are designed as "read clear". That is, these counters will be cleared after they are read.

**All Port Dropped Packet MIB counters** are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

# 8.0 Electrical Specifications

## 8.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

**Table 14: Absolute Maximum Ratings**

| Description | Pins | Value |
|---|---|---|
| Storage Temperature | N/A | -55°C to 150°C |
| Supply Voltages | VDDA, VDDAP, VDDC | -0.5V to 2.4V |
| | VDDATX, VDDARX, VDDIO | -0.5V to 4.0V |
| Input Voltage | All Inputs | -0.5V to 4.0V |
| Output Voltage | All Outputs | -0.5V to 4.0V |

## 8.2 Recommended Operating Conditions

**Table 15: Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltages | VDDA, VDDAP, VDDC | 1.710 | 1.8 | 1.890 | V |
| | VDDATX, VDDARX, VDDIO | 3.135 or 2.375 | 3.3 or 2.5 | 3.465 or 2.625 | V |
| Ambient Operating Temperature | TA | 0 | | 70 | °C |
| Maximum Junction Temperature | TJ | | | 125 | °C |
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | | 32 | | °C/W |

## 8.3 Electrical Characteristics

### Table 16: Electrical Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Current (including TX output driver current, KS8993M device only)** | | | | | | |
| | **100BaseTX operation (All ports @ 100% Utilization)** | | | | | |
| 100BaseTX (analog core + PLL + digital core) | $I_{ddc}$ | VDDA, VDDAP, VDDC = 1.8V | | 0.10 | | A |
| 100BaseTX (transceiver + digital I/O) | $I_{ddxio}$ | VDDATX, VDDARX, VDDIO = 3.3V | | 0.16 | | A |
| | **10BaseT operation (All ports @ 100% Utilization)** | | | | | |
| 10BaseT (analog core + PLL + digital core) | $I_{ddc}$ | VDDA, VDDAP, VDDC = 1.8V | | 0.07 | | A |
| 10BaseT (transceiver + digital I/O) | $I_{ddxio}$ | VDDATX, VDDARX, VDDIO = 3.3V | | 0.19 | | A |
| **TTL Inputs** | | | | | | |
| Input High Voltage | $V_{ih}$ | | ½ VDDIO + 0.4 V | | | V |
| Input Low Voltage | $V_{il}$ | | | | ½ VDDIO – 0.4 V | V |
| Input Current | $I_{in}$ | $V_{in}$ = GND ~ VDDIO | -10 | | 10 | µA |
| **TTL Outputs** | | | | | | |
| Output High Voltage | $V_{oh}$ | $I_{oh}$ = -8 mA | VDDIO - 0.4 | | | V |
| Output Low Voltage | $V_{ol}$ | $I_{ol}$ = 8 mA | | | 0.4 V | V |
| Output Tri-state Leakage | $\|I_{oz}\|$ | | | | 10 | µA |

| | | | | | | |
|---|---|---|---|---|---|---|
| **100BaseTX Transmit (measured differentially after 1:1 transformer)** | | | | | | |
| Peak Differential Output Voltage | $V_o$ | 100 Ω termination on the differential output. | 0.95 | | 1.05 | V |
| Output Voltage Imbalance | $V_{imb}$ | 100 Ω termination on the differential output | | | 2 | % |
| Rise/Fall time | $T_r/T_f$ | | 3 | | 5 | ns |
| Rise/Fall time Imbalance | | | 0 | | 0.5 | ns |
| **100BaseTX Transmit (measured differentially after 1:1 transformer)** | | | | | | |
| Duty Cycle Distortion | | | | | ± 0.5 | ns |
| Overshoot | | | | | 5 | % |
| Reference Voltage of ISET | $V_{set}$ | | | 0.5 | | V |
| Output Jitters | | Peak to peak | | 0.7 | 1.4 | ns |
| **10BaseT Receive** | | | | | | |
| Squelch Threshold | $V_{sq}$ | 5 MHz square wave | | 400 | | mV |
| **10BaseT Transmit (measured differentially after 1:1 transformer)** VDDATX = 3.3V only | | | | | | |
| Peak Differential Output Voltage | $V_p$ | 100 Ω termination on the differential output. | | 2.3 | | V |
| Jitters Added | | 100 Ω termination on the differential output. | | | ± 3.5 | ns |
| Rise/Fall time | | | | 25 | | ns |

# 9.0 Timing Specifications

## 9.1 EEPROM Timing

**Figure 13: EEPROM Interface Input Timing Diagram**

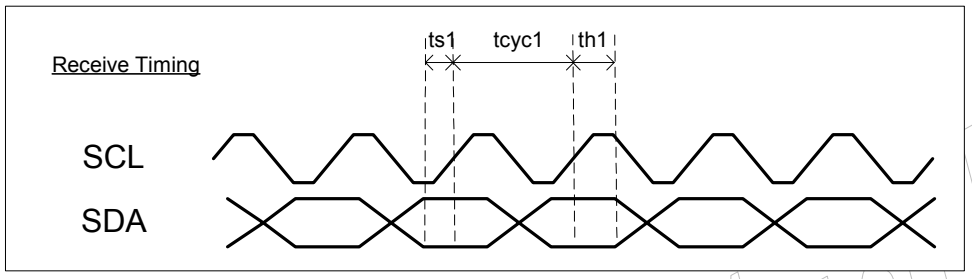



**Figure 14: EEPROM Interface Output Timing Diagram**

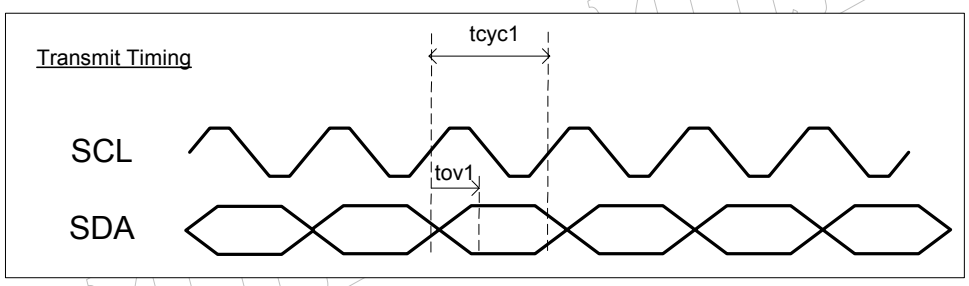





**Table 17: EEPROM Timing Parameters**

| Timing Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tcyc1 | Clock cycle | | 16384 | | ns |
| ts1 | Setup time | 20 | | | ns |
| th1 | Hold time | 20 | | | ns |
| tov1 | Output Valid | 4096 | 4112 | 4128 | ns |

## 9.2 SNI Timing

**Figure 15: SNI Input Timing Diagram**

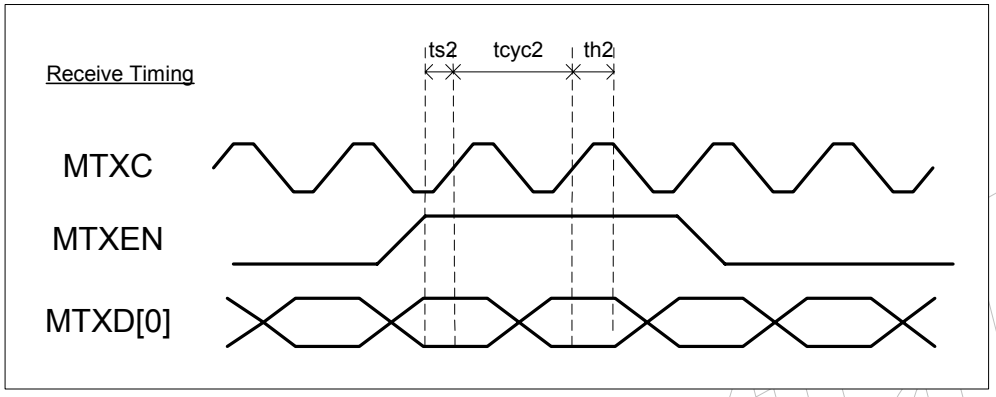



**Figure 16: SNI Output Timing Diagram**

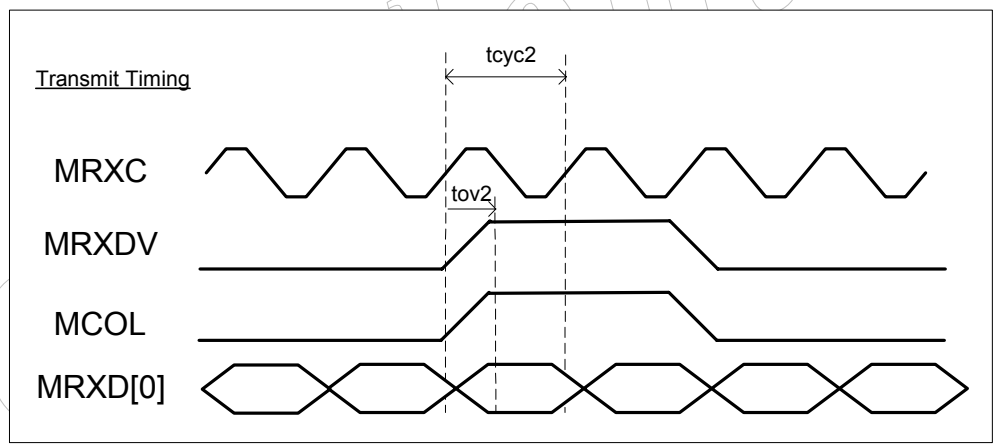



**Table 18: SNI Timing Parameters**

| Timing Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tcyc2 | Clock cycle | | 100 | | ns |
| ts2 | Setup time | 10 | | | ns |
| th2 | Hold time | 0 | | | ns |
| tov2 | Output Valid | 0 | 3 | 6 | ns |

## 9.3 MII Timing

### *9.3.1 MAC Mode MII Timing*

**Figure 17: MAC Mode MII Timing - Data received from MII**

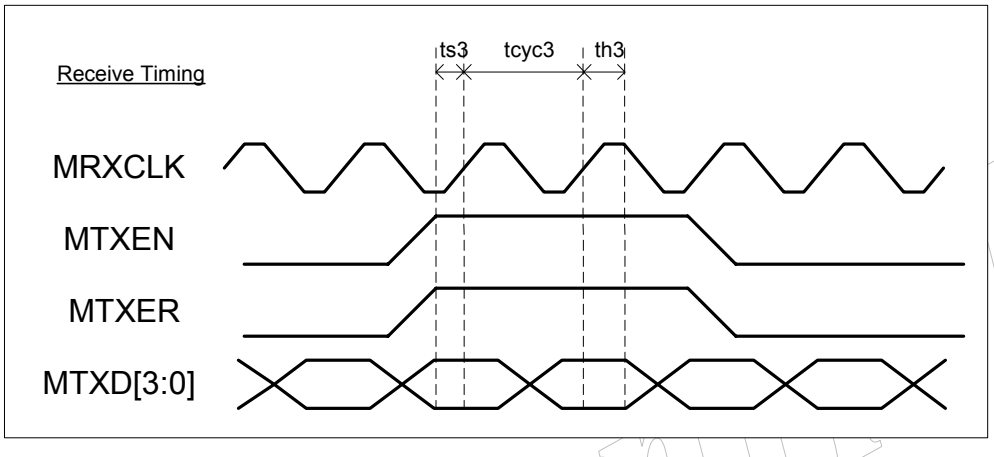



**Figure 18: MAC Mode MII Timing - Data transmitted to MII**

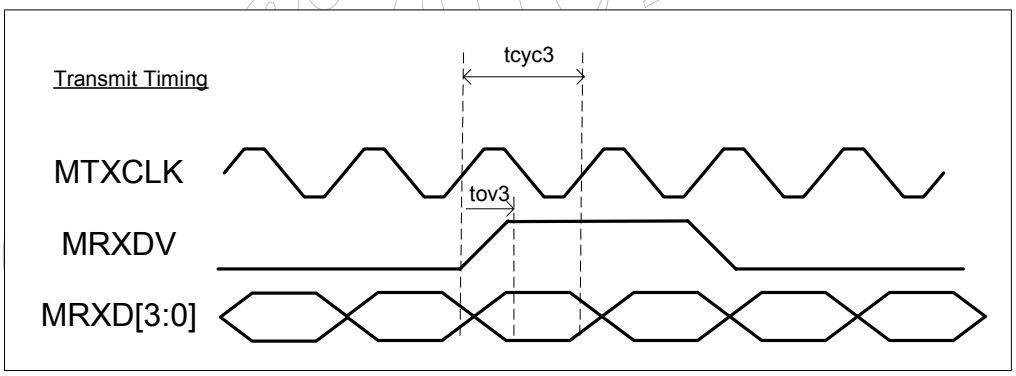



**Table 19: MAC mode MII Timing Parameters**

| Timing Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tcyc3 (100BaseT) | Clock cycle 100BaseT | | 40 | | ns |
| tcyc3 (10BaseT) | Clock cycle 10BaseT | | 400 | | ns |
| ts3 | Setup time | 10 | | | ns |
| th3 | Hold time | 5 | | | ns |
| tov3 | Output Valid | 7 | 11 | 16 | ns |

### *9.3.2 PHY Mode MII Timing*

**Figure 19: PHY Mode MII Timing – Data received from MII**

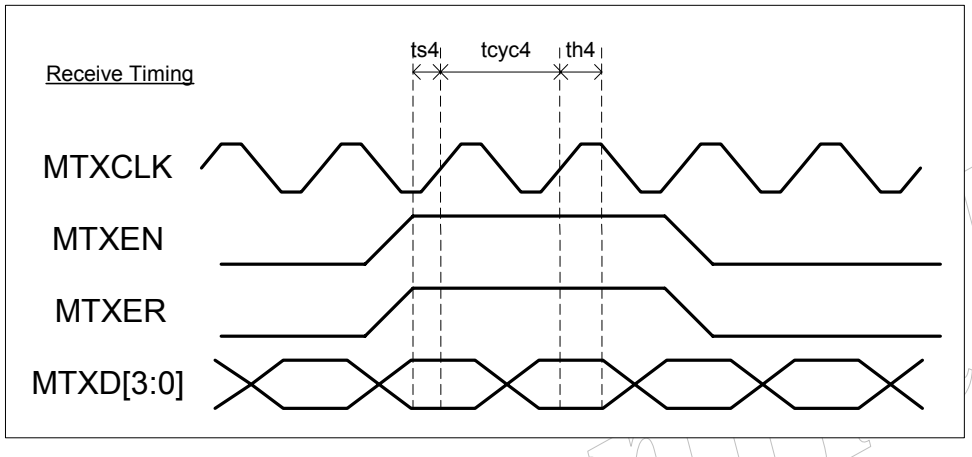



**Figure 20: PHY Mode MII Timing - Data transmitted to MII**

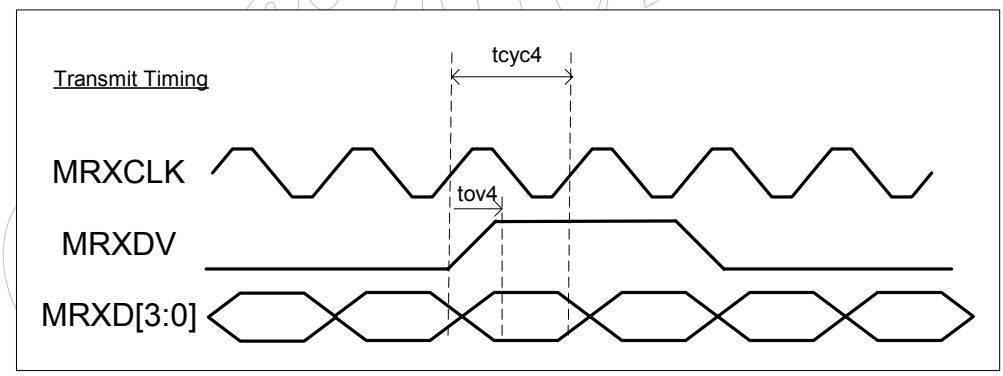



**Table 20: PHY Mode MII Timing Parameters**

| Timing Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tcyc4 (100BaseT) | Clock cycle 100BaseT | | 40 | | ns |
| tcyc4 (10BaseT) | Clock cycle 10BaseT | | 400 | | ns |
| ts4 | Setup time | 10 | | | ns |
| th4 | Hold time | 0 | | | ns |
| tov4 | Output Valid | 18 | 25 | 28 | ns |

## 9.4 SPI Timing

**Figure 21: SPI Input Timing**

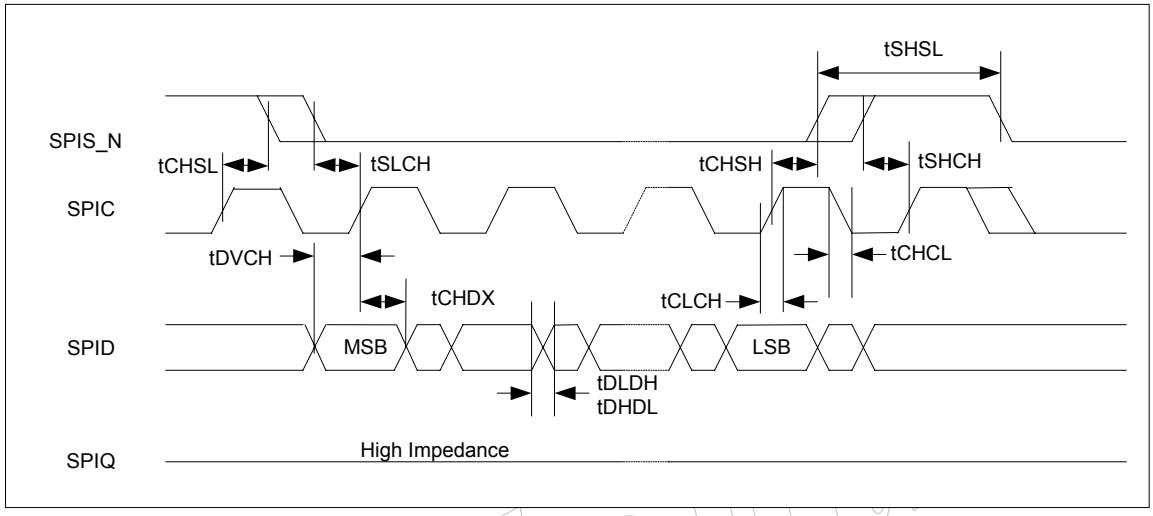
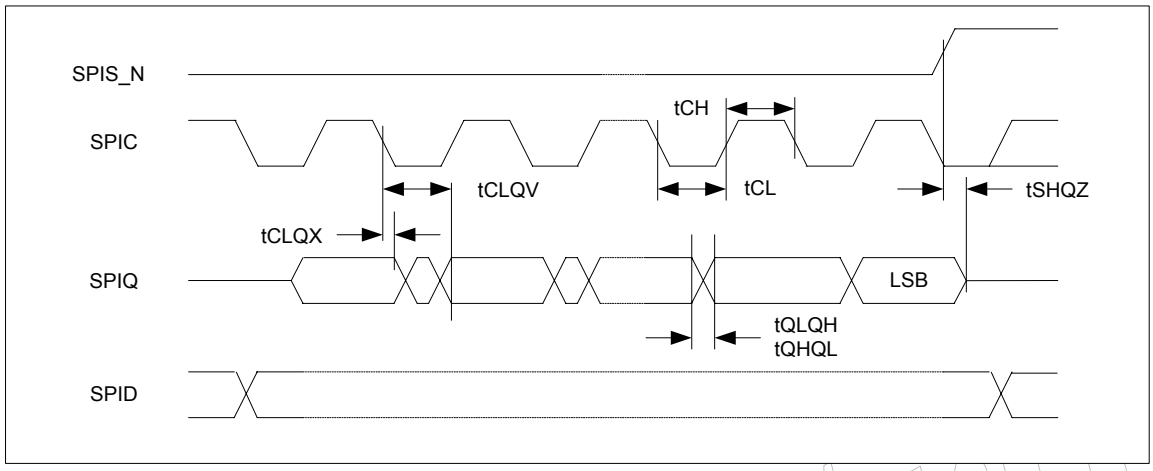



**Table 21: SPI Input Timing Parameters**

| Timing Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| fC | Clock Frequency | | 5 | MHz |
| tCHSL | SPIS_N Inactive Hold Time | 90 | | ns |
| tSLCH | SPIS_N Active Setup Time | 90 | | ns |
| tCHSH | SPIS_N Active Hold Time | 90 | | ns |
| tSHCH | SPIS_N Inactive Setup Time | 90 | | ns |
| tSHSL | SPIS_N Deselect Time | 100 | | ns |
| tDVCH | Data Input Setup Time | 20 | | ns |
| tCHDX | Data Input Hold Time | 30 | | ns |
| tCLCH | Clock Rise Time | | 1 | us |
| tCHCL | Clock Fall Time | | 1 | us |
| tDLDH | Data Input Rise Time | | 1 | us |
| tDHDL | Data Input Fall Time | | 1 | us |

## Figure 22: SPI Output Timing




## Table 22: SPI Output Timing Parameters

| Timing Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| fC | Clock Frequency | | 5 | MHz |
| tCLQX | SPIQ Hold Time | 0 | 0 | ns |
| tCLQV | Clock Low to SPIQ Valid | | 60 | ns |
| tCH | Clock High Time | 90 | | ns |
| tCL | Clock Low Time | 90 | | |
| tQLQH | SPIQ Rise Time | | 50 | ns |
| tQHQL | SPIQ Fall Time | | 50 | ns |
| tSHQZ | SPIQ Disable Time | | 100 | ns |

## 9.5 Reset Timing

As long as the stable supply voltages to reset high timing (minimum of 10 ms) is met, there is no power sequencing requirement for the KS8993M supply voltages (1.8V, 3.3/2.5V).

The reset timing requirement is summarized in the following figure and table.

**Figure 23: Reset Timing**

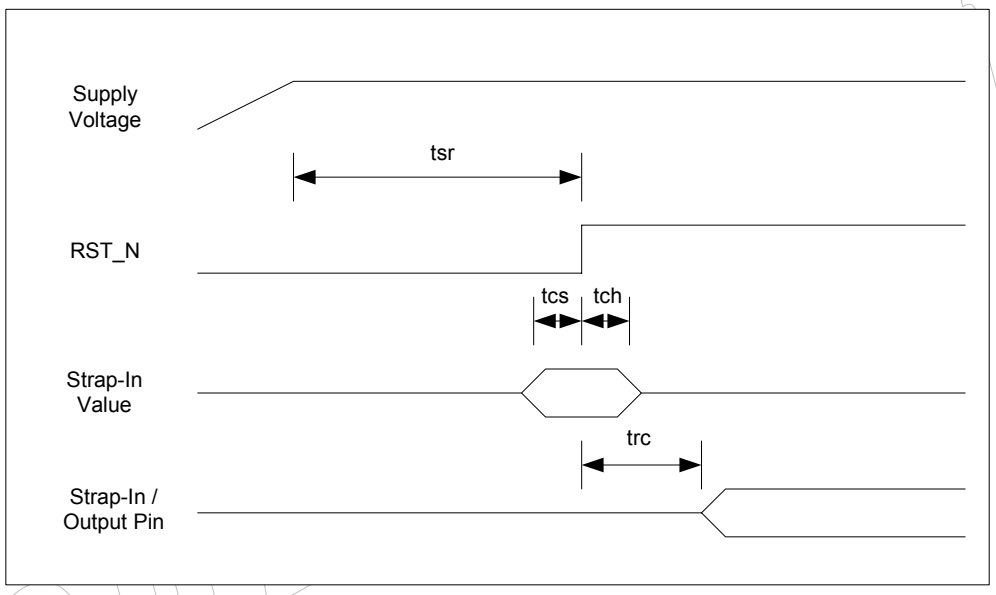



**Table 23: Reset Timing Parameters**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{sr}$ | Stable supply voltages to reset high | 10 | | ms |
| $t_{cs}$ | Configuration setup time | 50 | | ns |
| $t_{ch}$ | Configuration hold time | 50 | | ns |
| $t_{rc}$ | Reset to Strap-In pin output | 50 | | us |

# 10.0 Package Outline and Dimensions

**128 Pin PQFP Package Outline Drawing**

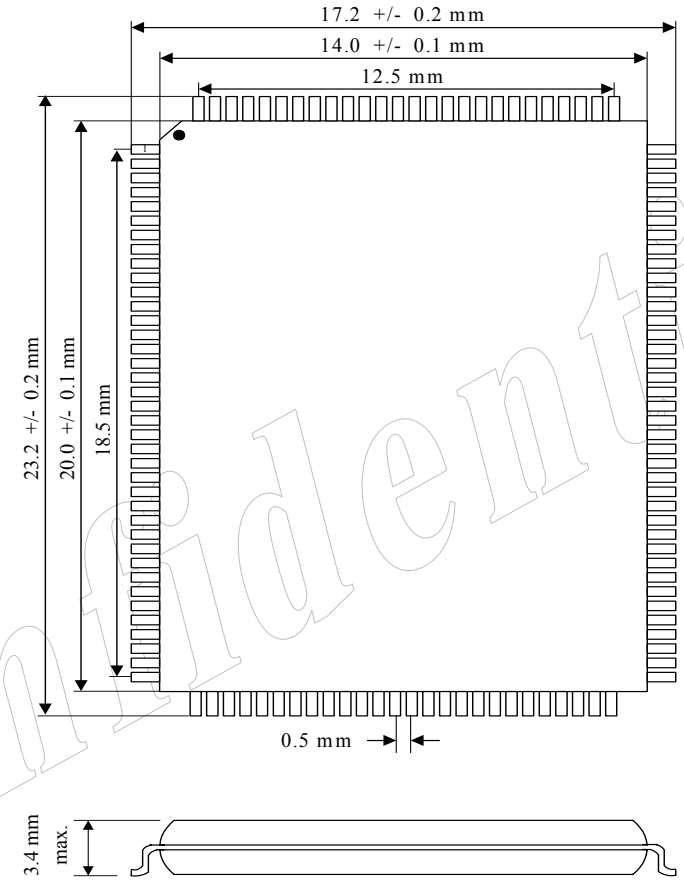





**Figure 24: Package Outline**

## 11.0 Selection of Isolation Transformers

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

**Table 24: Transformer Selection Criteria**

| ***Parameter*** | ***Value*** | ***Test Condition*** |
|---|---|---|
| Turns Ratio | 1 CT : 1 CT | |
| Open-Circuit Inductance (min.) | 350 uH | 100 mV, 100 kHz, 8 mA |
| Leakage Inductance (max.) | 0.4 uH | 1 MHz (min.) |
| Inter-Winding Capacitance (max.) | 12 pF | |
| D.C. Resistance (max.) | 0.9 Ohms | |
| Insertion Loss (max.) | 1.0 dB | 0-65 MHz |
| HIPOT (min.) | 1500 Vrms | |

The following are recommended transformers for the KS8993M.

**Table 25: Qualified Single Port Magnetics**

| ***Magnetic Manufacturer*** | ***Part Number*** | ***Auto MDI-X*** |
|---|---|---|
| Pulse | H1102 | Yes |
| Pulse (low cost) | H1260 | Yes |
| Transpower | HB726 | Yes |
| Bel Fuse | S558-5999-U7 | Yes |
| Delta | LF8505 | Yes |
| LanKom | LF-H41S | Yes |

## 12.0 Part Ordering Information

| *Part Number* | *Package* | *Description* |
|---|---|---|
| KS8993M | 128 pins PQFP | 3-Ports 10/100 Integrated Managed Switch for Commercial Temperature |
| KS8993MI‡ | 128 pins PQFP | 3-Ports 10/100 Integrated Managed Switch for Industrial Temperature |

**Note: ‡ KS8993MI is available from Q1 2004.**



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