SL1935

Single Chip Synthesized Zero IF Tuner

April 2004

Features

- Single chip synthesised tuner solution for quadrature down conversion, L-band to Zero IF.
- DVB compliant, operating dynamic range -70 to -20dBm.
- Compatible with DSS and DVB variable symbol rate applications.
- Selectable baseband path, programmable through I^2C bus.
- Excellent quadrature balance up to 30MHz baseband
- Excellent immunity to spurious second harmonic (RF and LO) mixing effects.
- Low oscillator phase noise and reradiation.
- High output referred linearity for low distortion and multi channel application.
- Integral fast mode compliant I^2C bus controlled PLL frequency synthesiser, designed for high comparison frequencies and low phase noise performance.
- Buffered crystal output for clocking QPSK demodulator.
- ESD protection (Normal ESD handling procedures should be observed).

Applications

- Satellite receiver systems.
- Data communications systems.

Ordering Information

SL1935D/KG/NP1P (Tubes)	36 pin SSOP
SL1935D/KG/NP1Q (Tape and Reel)	36 pin SSOP

Description

The SL1935 is a complete single chip I^2C bus controlled Zero IF tuner and operates from 950 to 2150MHz. It includes an on-board low phase noise PLL frequency synthesiser and low noise LNA/AGC. The SL1935 is intended primarily for application in digital satellite Network Interface Modules and performs the complete tuner function.

The device contains all elements necessary, with the exception of local oscillator tuning network and crystal reference, to produce a high performance I(n-phase) & Q(uadrature) downconversion tuner function. Due to the high signal handling design the device does not require any front end tracking filters.

The SL1935 includes selectable baseband signal paths, allowing application with two externally definable filter bandwidths, facilitating application in variable symbol rate and simulcast systems. The SL1935 is optimised to interface with the VP310 (ADC/QPSK/FEC) Satellite Channel Decoder, available from Zarlink Semiconductor and offers a full front end solution.

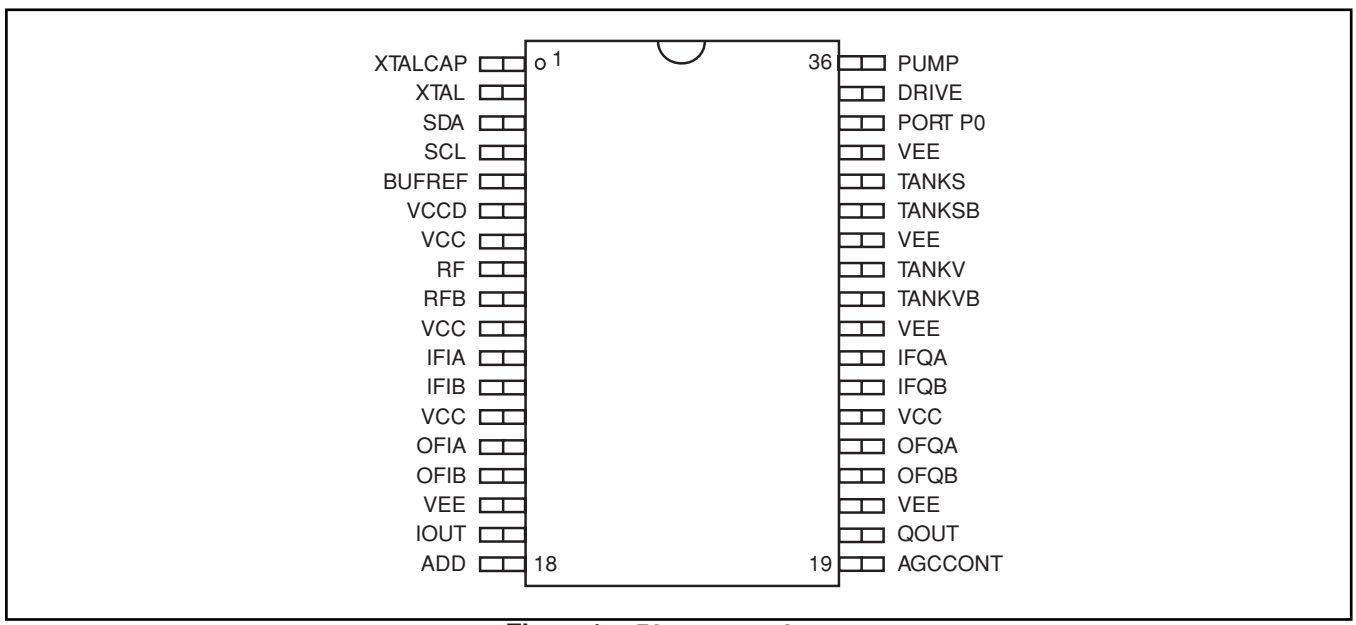


Figure1. Pin connections

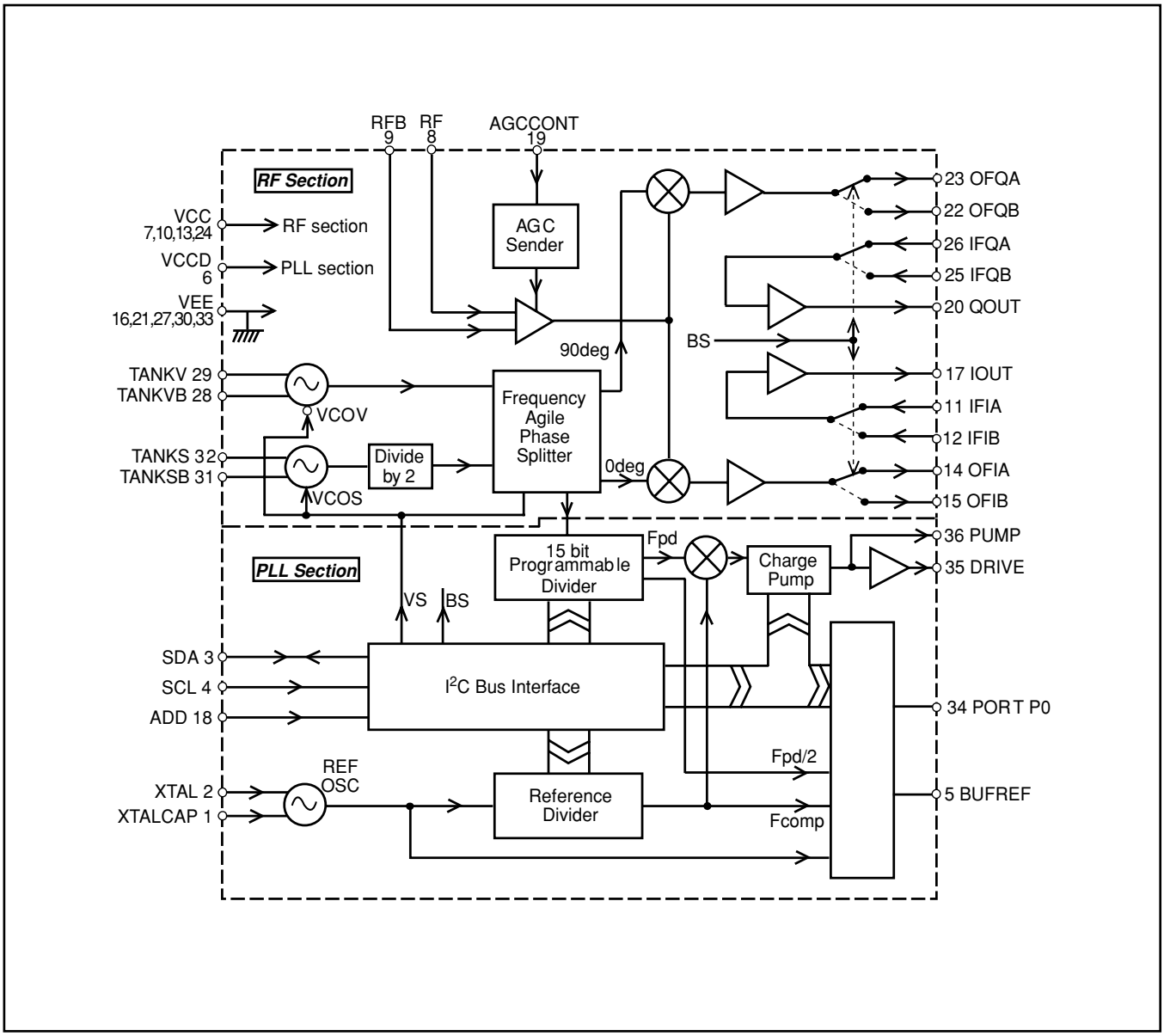


Figure 2. Block diagram

Table 1. Quick Reference Data

Characteristic	Value	Units
Operating range	950 to 2150	MHz
Input dynamic range	-75 to -15	dBm
VSWR with input match	10	dB
Input NF		
@ -70dBm operating sensitivity	10	dB
@ -60dBm operating sensitivity	15	dB
IPIP3 @ -20dBm operating sensitivity	+5	dBm
IPIP2@ -20dBm operating sensitivity	+20	dBm
IPP1dB@ -20dBm operating sensitivity	-5	dBm
Baseband output limit voltage	2.0	V
Gain match up to 22MHz	0.2	dB
Phase match up to 22MHz	0.7	deg
Gain flatness up to 30MHz	1	dB
Local oscillator phase noise		
SSB at 10kHz offset	-80	dBc/Hz
In band LO reradiation from RF input	<-70	dBm
LO second harmonic interference level at input level of -20dBm per carrier	-55	dBc
LNA second harmonic interference level at input level of -25dBm per carrier	-35	dBc
PLL maximum comparison frequency	4	MHz
PLL phase noise at phase detector	-152	dBc/Hz

Note: ∞6dB interstage filter loss assumed in external base band paths.
∞dBm assumes 75Ω characteristic impedance.

Functional Description

General

The SL1935 is a complete wideband direct conversion tuner incorporating an on board frequency synthesiser and LNA/AGC, optimised for application in digital satellite receiver systems. The device offers a highly integrated solution to a satellite tuner function, incorporating an I^2C bus interface controller, a low phase noise PLL frequency synthesiser and all tuner analogue functionality. The analogue blocks include the reference oscillator, consisting of two independent oscillators, a phase splitter, RF preamplifier with AGC facility, channel mixers and baseband amplifiers incorporating two selectable baseband paths, allowing for two externally definable bandwidths. In this application two varactor tuned tanks, a reference crystal and baseband filtering components are required to complete the tuner system.

A buffered crystal frequency output is available to clock the QPSK demodulator and powers up in the active state.

The I^2C bus interface controls the frequency synthesiser, the local oscillator, the baseband path selection, the buffered reference frequency output and an external switching port.

Figure 2 shows the device block diagram and pin allocations are shown in Figure 1.

Quadrature Downconverter Section

In normal application the tuner IF frequency of typically 950 to 2150MHz is fed direct to the SL1935 RF input through an appropriate impedance match (Fig.16) and LNB switching. The input stage is optimised for both NF and signal handling.

The signal handling of the front end is designed to offer immunity to input composite overload without the requirement of a tracking filter. RF input impedance is shown in Fig.3.

The RF input amplifier feeds an AGC stage and provides system gain control. The system AGC gain range will guarantee an operating dynamic range of -70 to -20dBm. The AGC is controlled by the AGC sender and is optimised for S/N and S/I performance across the full dynamic range. Details of the AGC characteristics, variations in IIP3, IIP2, P1dB and NF are illustrated in Figs.4, 5, 6, 7, and 8 respectively.

The required I and Q local oscillator frequencies for quadrature downconversion are generated by the on-board reference oscillators designated 'VCOS' and 'VCOV'. VCOS operates nominally from 1900 to 3000MHz and is then divided by two to provide 950 to 1500MHz. VCOV operates nominally from 1400 to 2200MHz. Only the oscillator selected via bit VS in the I^2C data transmission is powered.

Quadrature Downconverter Section - continued
The oscillators share a common varactor line drive and both require an external varactor tuned resonator optimised for low phase noise performance. The recommended application circuit for the local oscillators is detailed in Fig.9 and the typical phase noise performance is detailed in Fig.10. The local oscillator frequency is coupled internally to the PLL frequency synthesiser programmable divider input.

The mixer outputs are coupled to the baseband buffer amplifiers, providing for one of two selectable baseband outputs in each channel. The required output is selected by bit BS in the I^2C bus transmission (Table 6). These outputs are fed off chip via ports 'OPIA' and 'OPIB' ('OPQA' and 'OPQB'), then back on chip through ports 'IPIA' and 'IPIB' ('IPQA' and 'IPQB'), allowing for the insertion of two independent user definable filter bandwidths. Each output provides a low impedance drive (Fig.11) and each input provides a high impedance load . An example filter for 30MS/s is detailed in Fig.13. Both path gains are nominally equal. NB 6dB insertion loss is assumed in each channel, however a different pot down ratio may be applied.

Each baseband path is then multiplexed to the final baseband amplifier stage, providing further gain and a low impedance output drive. The nominal output load test condition is detailed in Fig.14.

PLL Frequency Synthesiser Section
The PLL frequency synthesiser section contains all the elements necessary, with the exception of a reference frequency source and a loop filter to control the selected oscillator to produce a complete PLL frequency synthesised source. The device, produced using high speed logic, allows for operation with a high comparison frequency and enables the generation of a loop with excellent phase noise performance.

The LO signal from the selected oscillator drives from the phase splitter into an internal preamplifier, providing gain and reverse isolation from the divider signals. The output of the preamplifier interfaces directly with the 15-bit fully programmable divider. The programmable divider has MN+A architecture, the dual modulus prescaler is 16/17, the A counter is 4-bits and the M counter is 11-bits.

The output of the programmable divider is fed to the phase comparator and compared in both phase and frequency domains to the comparison frequency. This frequency is derived from either the on board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider, programmable into 1 of 29 ratios and detailed in Table 3. The typical application for the crystal oscillator is shown in Fig.15.

The output of the phase detector feeds a charge pump and a loop amplifier. When used with an external loop filter and a high voltage transistor it integrates the current pulses into the varactor line voltage used to control the selected oscillator.

The programmable divider output Fpd divided by two and the reference divider output Fcomp are switched to port P0 by programming the device into test mode. Test modes are detailed in Table 4.

The crystal reference frequency can be switched to the BUFREF output by bit RE as detailed in Table 7.

Programming

The SL1935 is controlled by an I^2C data bus and is compatible with both standard and fast mode formats. Data and Clock are fed on the SDA and SCL lines respectively as defined by the I^2C bus format. The device can either accept data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. Tables 9a and 9b detail the format of the data. The SL1935 may be programmed to respond to several addresses and enables the use of more than one device in an I^2C bus system. Table 9c details the how the address is selected by applying a voltage to the 'ADD' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal 'STOP' condition which inhibits further reading.

Write mode
Bytes 2 and 3 contain frequency information bits 2^{14} to 2^0 inclusive (Table 9). Byte 4 controls the synthesiser reference divider ratio (Table 3) and the charge pump setting (Table 5). Byte 5 controls test modes (Table 4), baseband filter path select BS (Table 6), local oscillator select VS (Table 8), buffered crystal reference output select RE (Table 7) and the output port P0.
After reception and acknowledgment of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as byte 2 or 4, a logic '0' indicates byte 2 and a logic '1' indicates byte 4. Having interpreted this byte as either byte 2 or 4, the following byte will be interpreted as byte 3 or 5 respectively. After receiving two complete data bytes, additional data bytes may be entered and byte interpretation follows the same procedure without re-addressing the device. The procedure continues until a 'STOP' condition is received.

The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

Read mode

When the device is in read mode, the status byte read from the device takes the form shown in Table 9b.

Bit 1 (POR) is the power-on reset indicator, and this is set to a logic '1' if the Vccd supply to the device has dropped below 3V (at 25^{o}C),e.g. when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to the power up condition.

Bit 2 (FL) indicates whether the synthesiser is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Table 2. Programmable Features

Programmable features	Function
Synthesiser programmable divider	Function as described above
Reference programmable divider	Function as described above.
Baseband filter path select	Function as described above.
Local oscillator select	Function as described above.
Charge pump current	The charge pump current can be programmed by bits C1 & C0 (Table 5).
Test mode	The test modes are defined by bits T2 - T0 as described in Table 4.
General purpose port, P0	The general purpose port can be programmed by bit P0; Logic '1' = on Logic '0' = off (high impedance)
Buffered crystal reference output, BUFREF	The buffered crystal reference frequency can be switched to the BUFREF output by bit RE as described in Table 7. The BUFREF output defaults to the 'ON' condition at device power up.

The typical key performance data at Vcc = 5V and +25^{o}C ambient are detailed in Table 1.

Table 3. Reference division ratios

R4	R3	R2	R1	R0	Ratio
0	0	0	0	0	2
0	0	0	0	1	4
0	0	0	1	0	8
0	0	0	1	1	16
0	0	1	0	0	32
0	0	1	0	1	64
0	0	1	1	0	128
0	0	1	1	1	256
0	1	0	0	0	Illegal state
0	1	0	0	1	5
0	1	0	1	0	10
0	1	0	1	1	20
0	1	1	0	0	40
0	1	1	0	1	80
0	1	1	1	0	160
0	1	1	1	1	320
1	0	0	0	0	Illegal state
1	0	0	0	1	6
1	0	0	1	0	12
1	0	0	1	1	24
1	0	1	0	0	48
1	0	1	0	1	96
1	0	1	1	0	192
1	0	1	1	1	384
1	1	0	0	0	Illegal state
1	1	0	0	1	7
1	1	0	1	0	14
1	1	0	1	1	28
1	1	1	0	0	56
1	1	1	0	1	112
1	1	1	1	0	224
1	1	1	1	1	448

Table 4. Test modes

T2	T1	T0	Test mode description
0	0	0	Normal operation
0	0	1	Charge pump sink* (status byte FL set to logic '0')
0	1	0	Charge pump source* (status byte FL set to logic '0')
0	1	1	Charge pump disabled* (status byte FL set to logic '1')
1	0	0	Normal operation and port P0 = Fpd/2
1	0	1	Charge pump sink* (status byte FL set to logic '0'. Port P0 = Fcomp)
1	1	0	Charge pump source* (status byte FL set to logic '0'. Port P0 = Fcomp)
1	1	1	Charge pump disabled* (status byte FL set to logic '1'. Port P0 = Fcomp)

Note: * Clocks need to be present on crystal and RF inputs to enable charge pump test modes and to toggle status byte bit FL.

Table 5. Charge pump current

C1	C0	Current in μA		
		min	typ	max
0	0	+-116	+-155	+-194
0	1	+-247	+-330	+-412
1	0	+-517	+-690	+-862
1	1	+-1087	+-1450	+-1812

Table 6. Baseband path select

BS	Path Selected			
	I Channel		Q Channel	
	Filter drive output	Baseband amp input	Filter drive output	Baseband amp input
0	OFIB	IFIB	OFQB	IFQB
1	OFIA	IFIA	OFQA	IFQA

Table 7. Buffered crystal reference output select

RE	BUFREF output
0	Disabled, high impedance
1	Enabled

Table 8. Local oscillator select

VS	Local oscillator selected
0	VCOV
1	VCOS

Table 9a. Write data format (MSB is transmitted first)

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	Byte 1
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
Control data	1	C1	C0	R4	R3	R2	R1	R0	A	Byte 4
Control data	T2	T1	T0	VS	BS	0	RE	P0	A	Byte 5

Table 9b. Read data format (MSB is transmitted first)

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	Byte 1
Status Byte	POR	FL	0	0	0	0	0	0	A	Byte 2

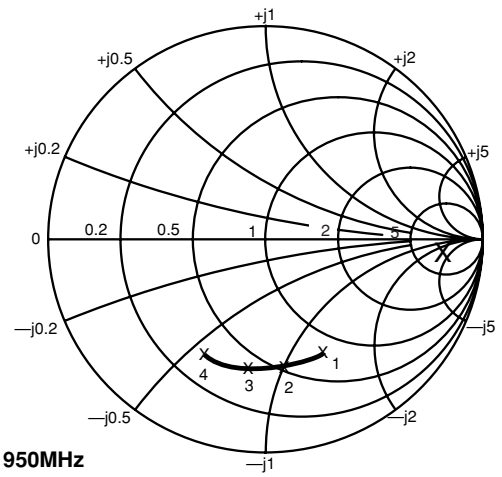
Table 9c. Address selection

MA1	MA0	Address input voltage level
0	0	0 - 0.1 Vcc
0	1	Open circuit
1	0	0.4 Vcc - 0.6 Vcc*
1	1	0.9 Vcc - Vcc

Note: * Programmed by connecting a 30kΩ resistor between pin and Vcc

Key to Tables 9a to 9c

A ..... Acknowledge bit
MA1, MA0 ..... Variable address bits (Table 9c)
2^{14} to 2^{0} ..... Programmable division ratio control bits
C1 to C0 ..... Charge pump current select (Table 5)
R4 to R0 ..... Reference division ratio select (Table 3)
T2 to T0 ..... Test modes control bits (Table 4)
BS ..... Baseband path select (Table 6)
VS ..... Local oscillator select (Table 8)
RE ..... Buffered crystal reference output enable (Table 7)
P0 ..... P0 port output state
POR ..... Power on reset indicator
FL ..... Phase lock flag



Marker	Freq (MHz)	Z real Ω	Z imag Ω
1	950	64	-100
2	1400	40	-75
3	1600	32	-65
4	2150	23	-45

START 950MHz

Normalised to 75Ω

STOP 2150MHz

Figure 3. RF input impedance (typical)

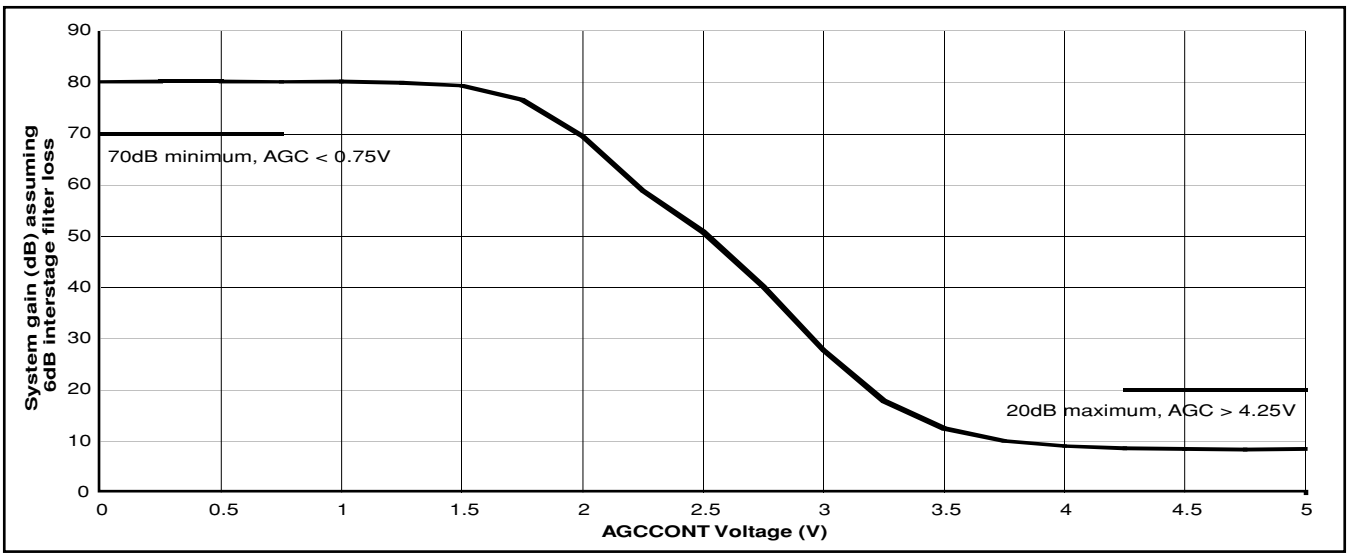


Figure 4. AGC characteristic (typical)

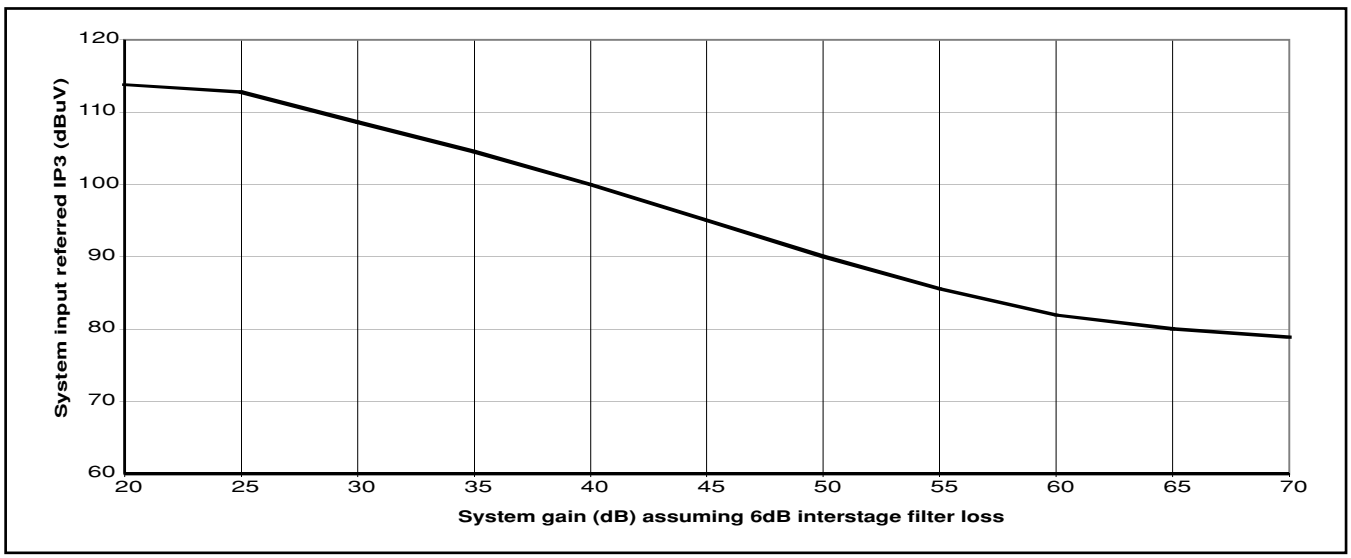


Figure 5. Variation in IIP3 with system gain (typical)

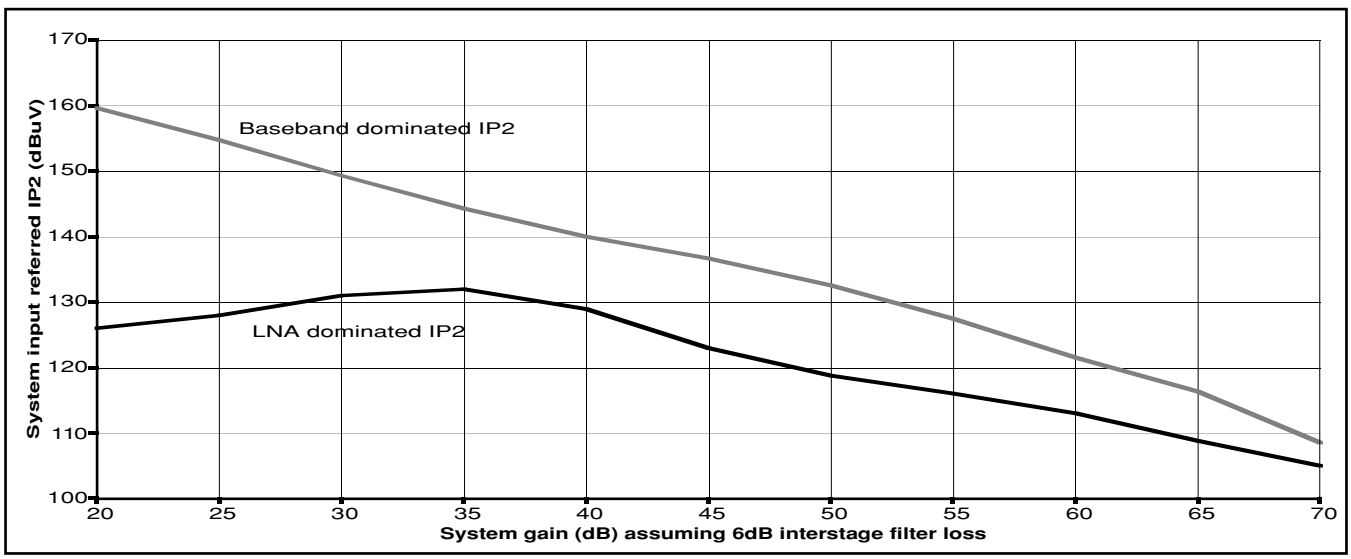


Figure 6. Variation in IIP2 with system gain (typical)

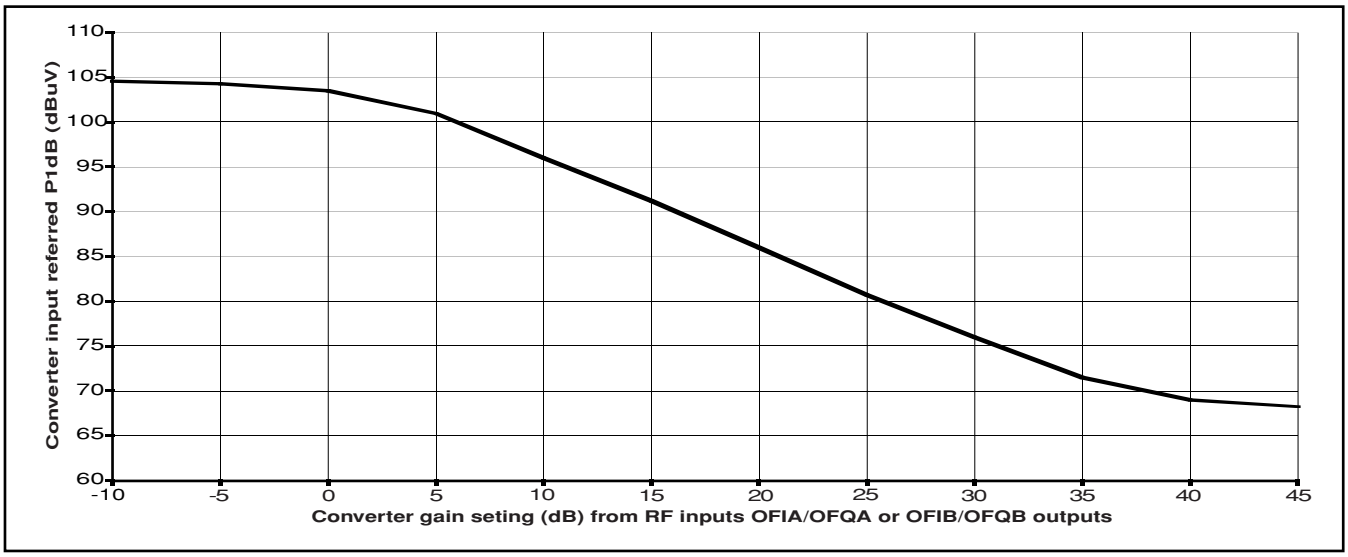


Figure 7. Variation in P1dB with converter gain (typical)

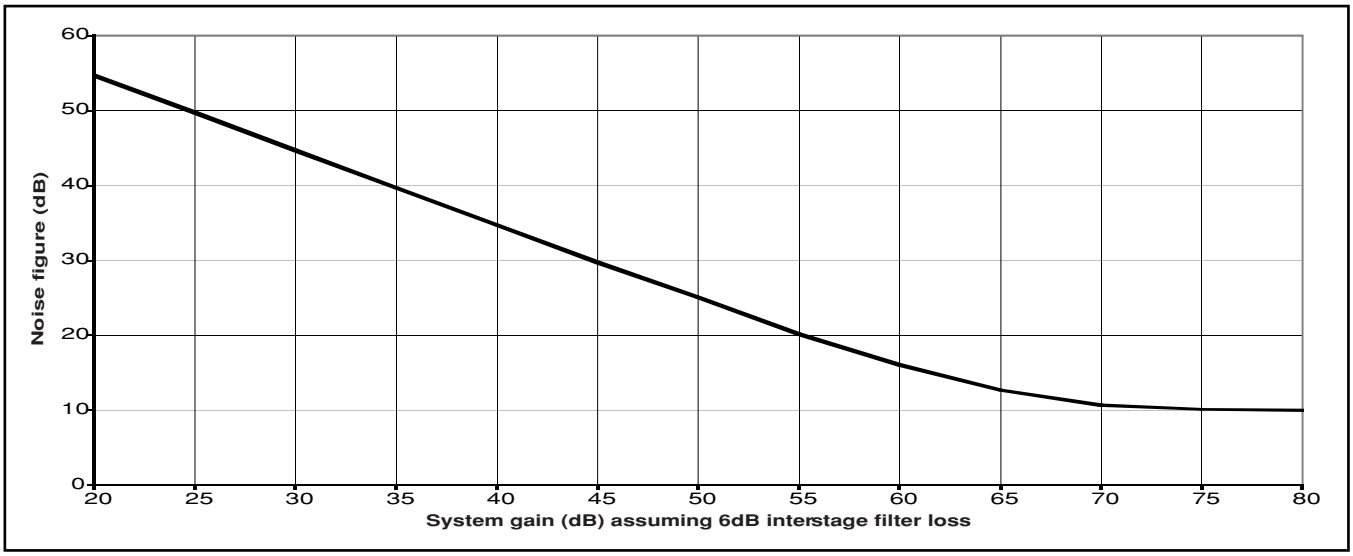


Figure 8. Variation in NF with system gain (typical)

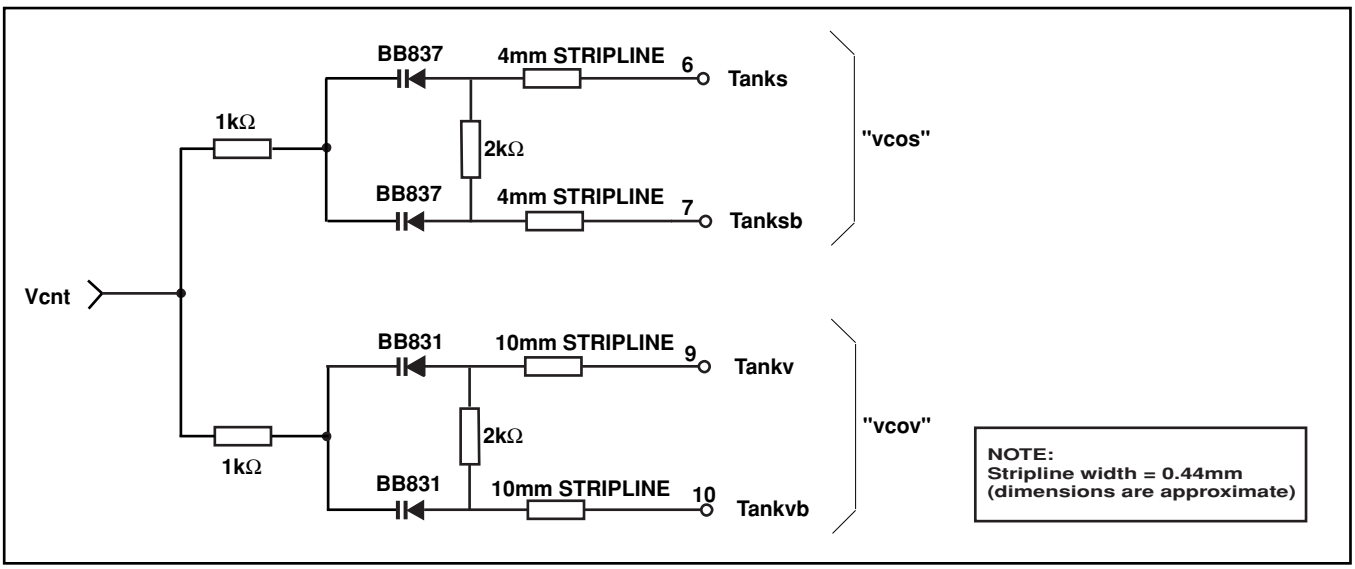


Figure 9. Local oscillator application circuit

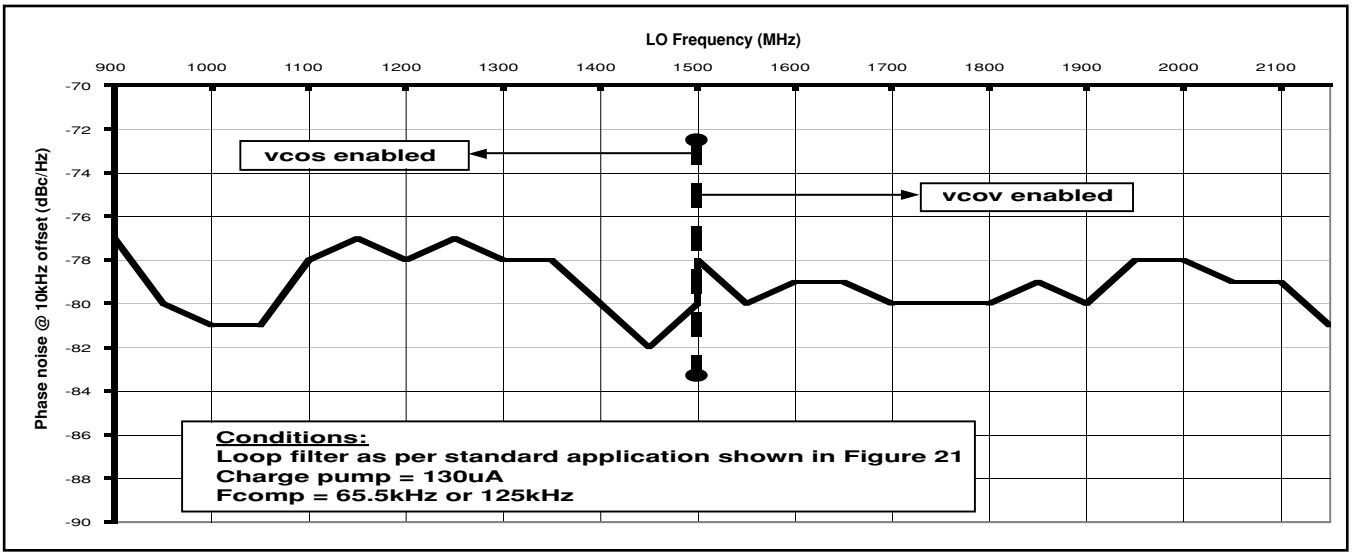
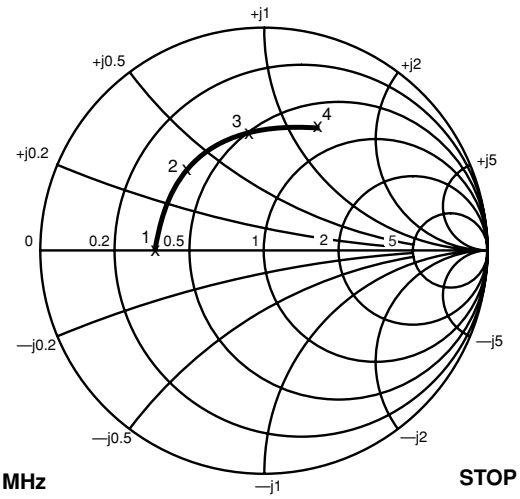


Figure 10. Local oscillator phase noise variation with frequency (typical)

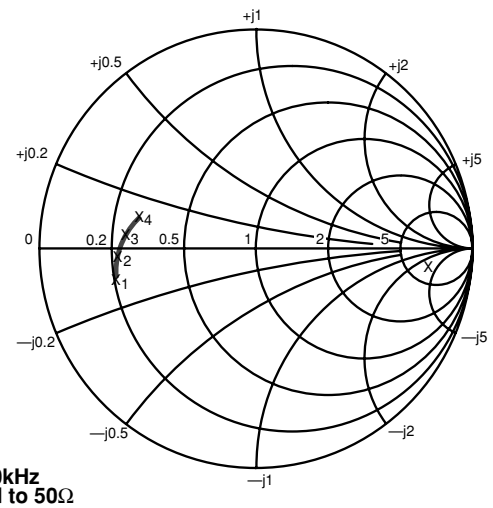


Marker	Freq (MHz)	Z real Ω	Z imag Ω
1	1	17	0
2	10	18	19
3	20	22	38
4	30	33	60

START 1MHz
Normalised to 50Ω

STOP 30MHz

Figure 11. Converter output impedance; OFIA, OFIB, OFQA, OFQB (typical)



Marker	Freq (MHz)	Z real Ω	Z imag Ω
1	0.1	9.5	-2.0
2	10	10.0	1.3
3	20	10.6	3.3
4	30	12.6	5.5

START 100kHz
Normalised to 50Ω

STOP 30MHz

Figure 12. Baseband output impedance; IOUT, QOUT (typical)

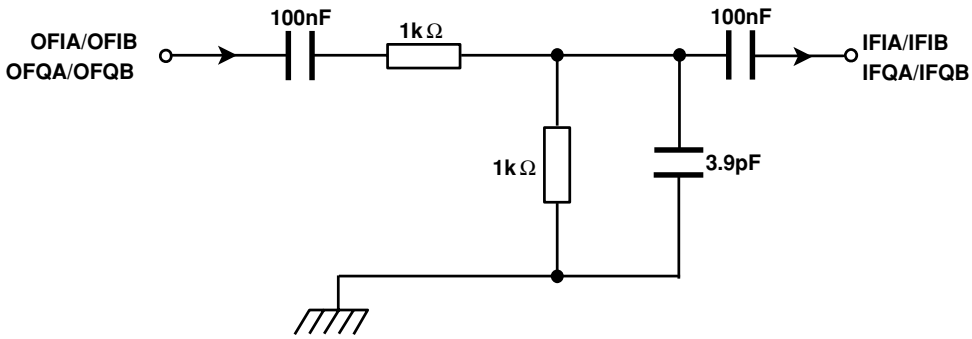


Figure 13. Example baseband interstage filter for 30MS/s

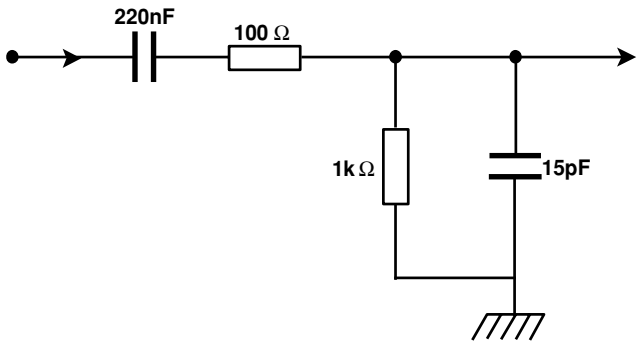


Figure 14. Nominal baseband output load test condition

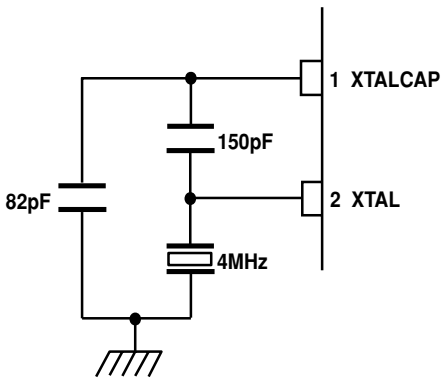


Figure 15. Crystal oscillator application (typical)

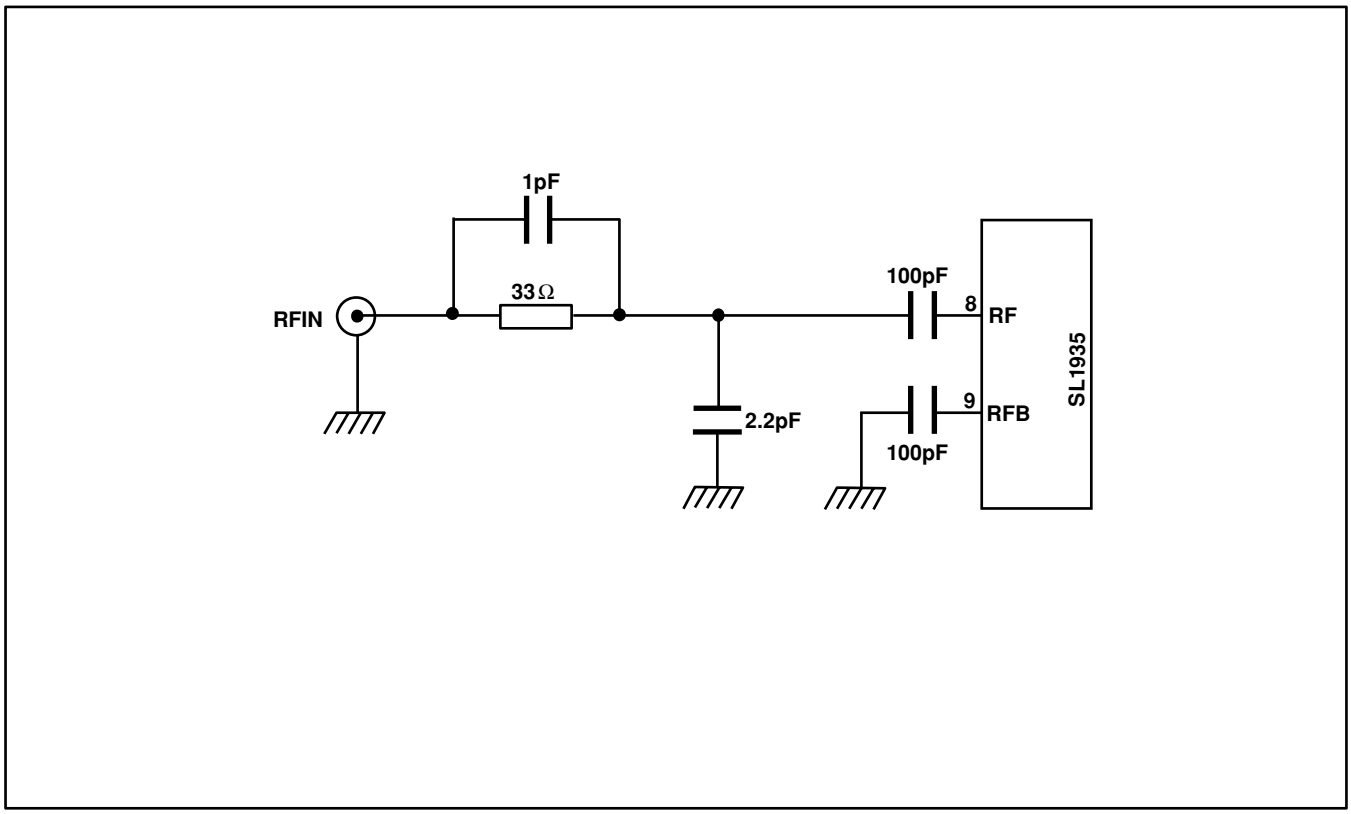


Figure 16. Input matching network

Table 10. Electrical Characteristics

Test conditions (unless otherwise stated); Tamb = -20°to +80°C, Vee= 0V, Vcc =Vccd = 5V+-5%.
These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	6,7,10 13,24		130	175	mA	VCCD (PLL) and VCC
RF input operating frequency	8,9	950		2150	MHz	
SYSTEM						All system specification items should be read in conjunction with Note 2
System noise figure DSB			10	12	dB	At -70dBm operating sensitivity
			15	17	dB	At -60dBm operating sensitivity
Variation in system NF with gain adjust				-1	dB/dB	Above –60dBm operating sensitivity, (Fig.7)
System input referred IP2		121	140		dBµV	At –20dBm operating sensitivity, see Notes 3 and 4
Variation in system input referred IP2 with operating sensitivity						(Fig.6)
System input referred IP3		112			dBµV	At -20dBm operating sensitivity, see Note 5
Variation in system input referred IP3 with operating sensitivity						(Fig.5)

Continued

Table 10. Electrical Characteristics (Continued)

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
System dynamic range						Note 6
		-70			dBm	AGCCONT = 0.75V
				-20	dBm	AGCCONT = 4.25V
System gain roll off			3		dB	Within RF band 950-2150MHz
System gain variation with temperature			2		dB	-20˚C to +80˚C
System I Q gain match	17,20	-1		+1	dB	Interstage filter (Fig.13)
System I Q phase balance	17,20	-3		+3	deg	Interstage filter (Fig.13)
System I and Q channel in band ripple	17,20			1	dB	Interstage filter (Fig.13)
System baseband path gain match		-1		+1	dB	
LO second harmonic interference level			-50		dBc	Note 8.
LNA second harmonic interference level			-35		dBc	Note 9.
Synthesiser and other spurii on I and Q outputs	17,20			76	dBµV	Within 0-100MHz band under all gain settings, RF input set to deliver 108dBµV on output
In band leakage to RF input	8,9		-60		dBm	Within RF band 950-2150MHz. Note 11.
CONVERTER						
Converter input impedance	8,9		75		Ω	
Converter input return loss	8,9	8			dB	With input matching (Fig.16)
System input referred P1dB		102			dBµV	Converter gain =-5dBm (to OFIA/ OPQA, OFIB/OPQB outputs. Fig.7)
Converter output impedance, OFIA, OFIB, OPQA and OPQB.	14,15 22,23		25	50	Ω	0.1 to 30MHz (Fig.11)
Converter output leakage to unselected output, OFIA, OFIB, OPQA and OPQB.			-26		dBc	Relative to selected output
Oscillator VCOS operating range	31,32	1900		3000	MHz	Giving LO = 950 to 1500MHz (Application as in Fig.9)
Oscillator VCOV operating range	28,29	1450		2150	MHz	(Application as in Fig.9)
Local oscillator SSB phase noise			-78		dBc/Hz	@10kHz offset, PLL loop bw < 1kHz Application is measured at baseband output frequency of 10MHz (Fig.10).
AGCONT input current	19	-150		150	µA	
BASEBAND AMPLIFIERS						The baseband inputs must be externally ac coupled
Baseband input impedance, IFIA, IFIB, IFQA And IFQB.	11,12 25,26					0.1- 30MHz bandwidth
Resistance		10			kΩ	
Capacitance				5	pF	
Baseband unselected input leakage to output	17,20			-40	dBc	Relative to selected input.
Baseband amplifier output impedance	17,20			20	Ω	
Baseband output limiting	17,20		2.0		Vp-p	Level at hard clipping (load as Fig.14)
Baseband bandwidth 1dB	17,20	40			MHz	(Load as Fig.14)
Baseband output roll-off		6			dB/oct	Above 3dB point, no load

Continued

Table 10. Electrical Characteristics (Continued)

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
SYNTHESISER						
SDA,SCL	3,4					I²C 'fast mode' compliant
Input high voltage		3		5.5	V	
Input low voltage		0		1.5	V	
Input high current				10	µA	Input voltage = Vcc
Input low current		-10			µA	Input voltage = Vee
Leakage current				10	µA	Vcc = Vee = 0V
Hysterysis			0.4		V	
SDA output voltage	3			0.4	V	Isink = 3mA
				0.6	V	Isink = 6mA
SCL clock rate	4			400	kHz	
Charge pump output current	36					Vpin36 = 2V. (Table 5)
Charge pump output leakage	36		+-3	+-10	nA	Vpin36 = 2V
Charge pump drive output current	35	0.5			mA	Vpin35 = 0.7V
Crystal frequency	1,2	2		20	MHz	(Fig.15 for application)
Recommended crystal series resistance		10		200	Ω	4MHz parallel resonant crystal
External reference input frequency	2	2		20	MHz	Sinewave coupled via 10nF blocking capacitor
External reference drive level	2	0.2		0.5	Vpp	Sinewave coupled via 10nF blocking capacitor
Phase detector comparison frequency				4	MHz	
Equivalent phase noise at phase detector			-152		dBc/Hz	SSB within loop bandwidth, all comparison frequencies
Local oscillator programmable divider division ratio		240		32767		
Reference division ratio						(Table 3)
Output port P0	34					(Note 7)
Sink current		2			mA	Vport = 0.7
Leakage current				10	µA	Vport = Vcc
BUFREF output	5					AC coupled. (Note 10.)
Output amplitude		0.25	0.35	0.45	Vpp	Enabled by bit RE = 1 and default
Output impedance			250		Ω	state on power-up.
Address select	18					(Table 9c)
Input high curent				1	mA	Vin = Vcc
Input low current				-0.5	mA	Vin = Vee

Notes to Table 10

1. All power levels are referred to 75Ω, and 0dBm = 109dBµV.
2. System specifications refer to total cascaded system of converter/AGC stage and baseband amplifier stagewith nominal 6dB pad as interstage filter and load impedance as detailed in Figure 14.
3. Baseband dominated IP2. AGC set for 20dB system gain with two tones for intermodulation test at fc+146and fc+155MHz at 100dBµV generating output intermodulation spur at 9MHz. 30MHz 3dB bandwidthinterstage filter included.
4. LNA dominated IP2. AGC set for 20dB system gain with two tones for intermodulation test at fc+146 and2*fc+155 MHz at 100dBµV generating output intermodulation spur at 9MHz. 30MHz 3dB bandwidthinterstage filter included.
5. AGC set for 20dB system gain with two tones for intermodulation test at fc+110 and fc+211MHz at 100dBµVgenerating output intermodulation spur at 9MHz. 30MHz 3dB bandwidth interstage filter included.
6. Dynamic range assuming termination as detailed in Figure 14, and including 6 dB interstage filter insertion loss, delivering 700mVp-p at baseband outputs (pins 17,20). AGC monotonic from Vee to Vcc (Fig.4).
7. Port powers up in high impedance state.
8. The level of 2.01GHz downconverted to baseband relative to 1.01GHz with the oscillator tuned to 1GHz,measured with no input pre-filtering.
9. The level of second harmonic of 1.01GHz input at –25dBm downconverted to baseband relative to 2.01GHz at–40 dBm with the oscillator tuned to 2GHz, measured with no input pre-filtering.
10. If the BUFREF output is not used it should be left open circuit or connected to Vccd, and disabled by settingRE = '0'.
11. This parameter is very application dependant. With good RF isolation <-60dBm can be achieved.

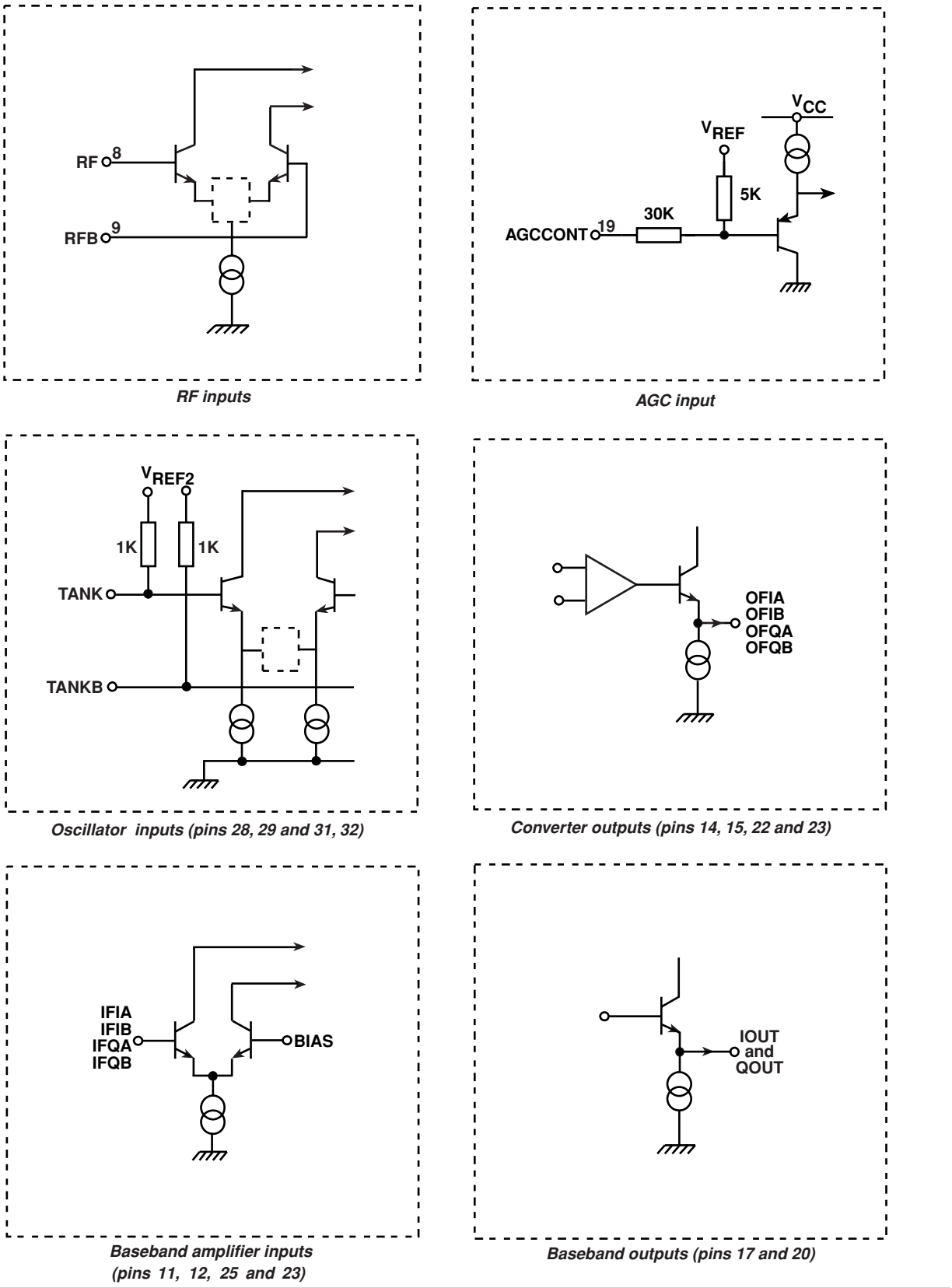


Figure 17. Input and output interface circuits (RF section)

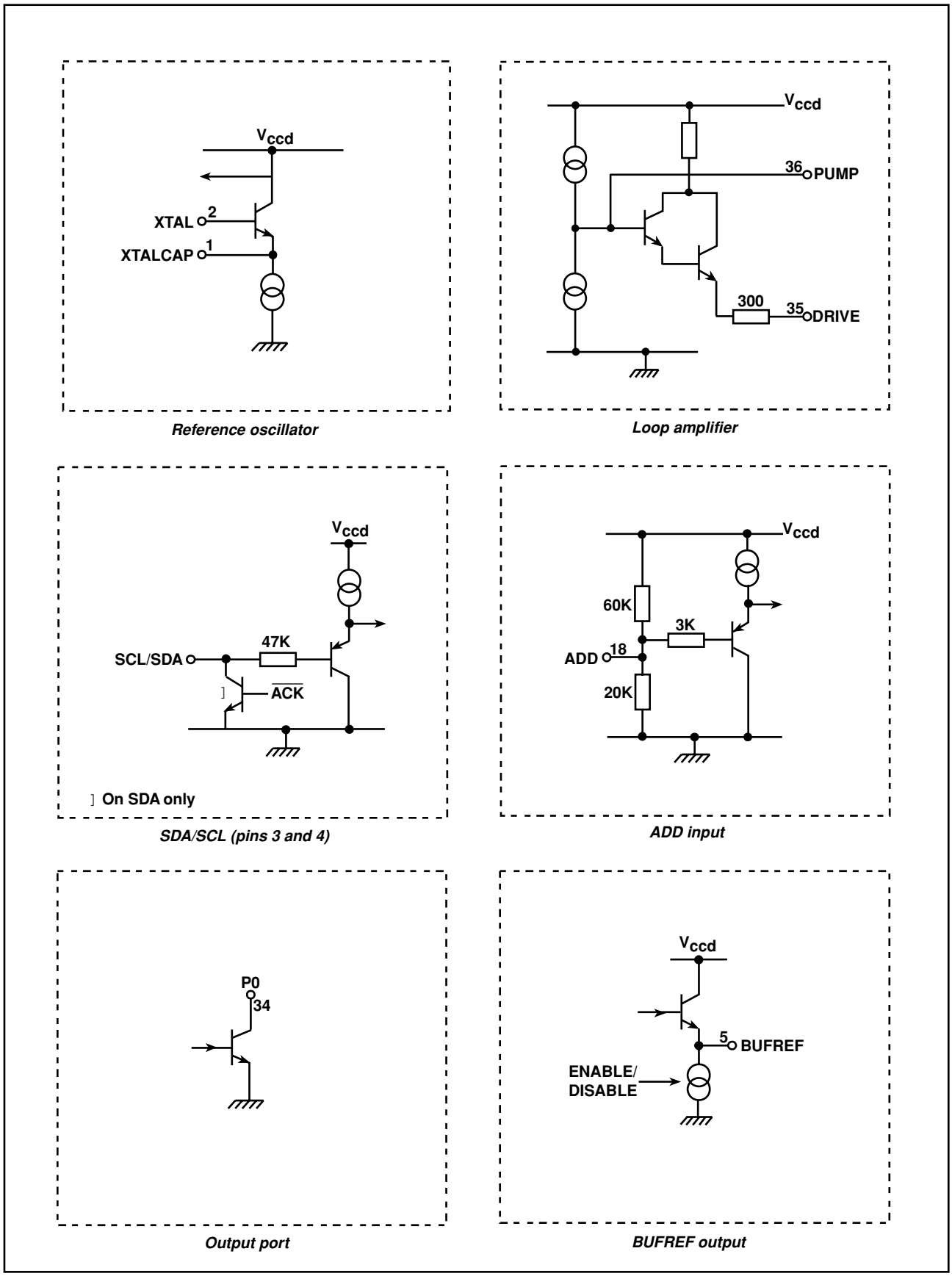


Figure 18. Input and output interface circuits (PLL section)

Table 11. Absolute Maximum Ratings (All voltages referred to Vee at 0V and Vcc = Vccd)

Characteristic	Min	Max	Units	Conditions
Supply voltage	-0.3	7	V	
SDA, SCL DC offsets	-0.3	6	V	Vcc = Vee to 5.25V
All I/O port DC offsets	-0.3	Vcc+0.3	V	
Port P0 current		10	mA	
Storage temperature	-55	150	°C	
Junction temperature		150	°C	
Package thermal resistance, chip to case		20	°C/W	
Package thermal resistance, chip to ambient		77	°C/W	
Power consumption at 5.25V		919	mW	
ESD protection	3.5		kV	Mil-std 883 method 3015 cat1

SL1935 Demo Board

The demo board contains an SL1935 I²C bus controlled Zero IF tuner IC, plus all components necessary to demonstrate operation of the SL1935. The schematic and PCB layout of the board are shown in Figures 19, 20 and 21.

Supplies
The board must be provided with the following supplies:

5V for the synthesiser section (5VD)
5V for the converter and baseband sections (5V)
30V for the varactor line (30V)

The supply connector is a 5 pin 0.1" pin header.
The order of connections is 5V – GND – 30V – GND – 5V.

I²C bus connections
The board is provided with a RJ11 I²C bus connector which feeds directly to the synthesiser. This connects to a standard 4 way cable.

Operating instructions
1. Software.
Use the Zarlink Semiconductor synthesiser software. Pull down the 'Device' menu, then select the 'SL1935'. It is suggested that the charge pump is set to 130uA with a reference divider ratio of 32. These settings give a small loop bandwidth (i.e. 100's Hz), which allows detailed phase noise measurements of the oscillators to be taken if desired.

2. VCO control.
The two VCO's are selected by toggling the oscillator switch below the two oscillators on the main software block diagram. This switch programs bit VS of the I²C data (see Tables 8 and 9a to 9c).

VCOS oscillates at twice the LO frequency (lower band) and is then divided by two to provide the required LO frequency in the range 950MHz to 1500MHz (approximately).

VCOV oscillates at the LO frequency (upper band) in the range 1500MHz to 2150MHz (approximately).

3. Baseband path select.
The SL1935 has two filter paths selected by programming bit BS of the I²C data (see Tables 6 and 9a to 9c). The value of BS is changed by toggling the switch position to the left of 'Filter A' and 'Filter B' on the main software block diagram.

4. AGC control.
The conversion gain of the SL1935 is set by the voltage applied to the AGCCONT input. On the demo board this is controlled by the potential divider labelled 'AGC ADJ' which varies the AGCCONT input from 0V to Vcc.

CAUTION: Care should be taken to ensure the chip is powered ON if the board is modified to accept an external AGC input voltage. Damage to the device may result if this is not complied with as a result of the IC powering itself up via the AGCCONT input ESD protection diode. It is recommended that a low current limit is set on any external AGC voltage source used.

5. Free running the VCO's.
Select the required VCO as detailed in (2) above. Program an LO frequency which is above the maximum capability of the oscillator. 3GHz is suggested. Under this condition the varactor control voltage is pumped to its maximum value, ie to the top of the band. The oscillator frequency can now be manually tuned by varying the 30V supply.

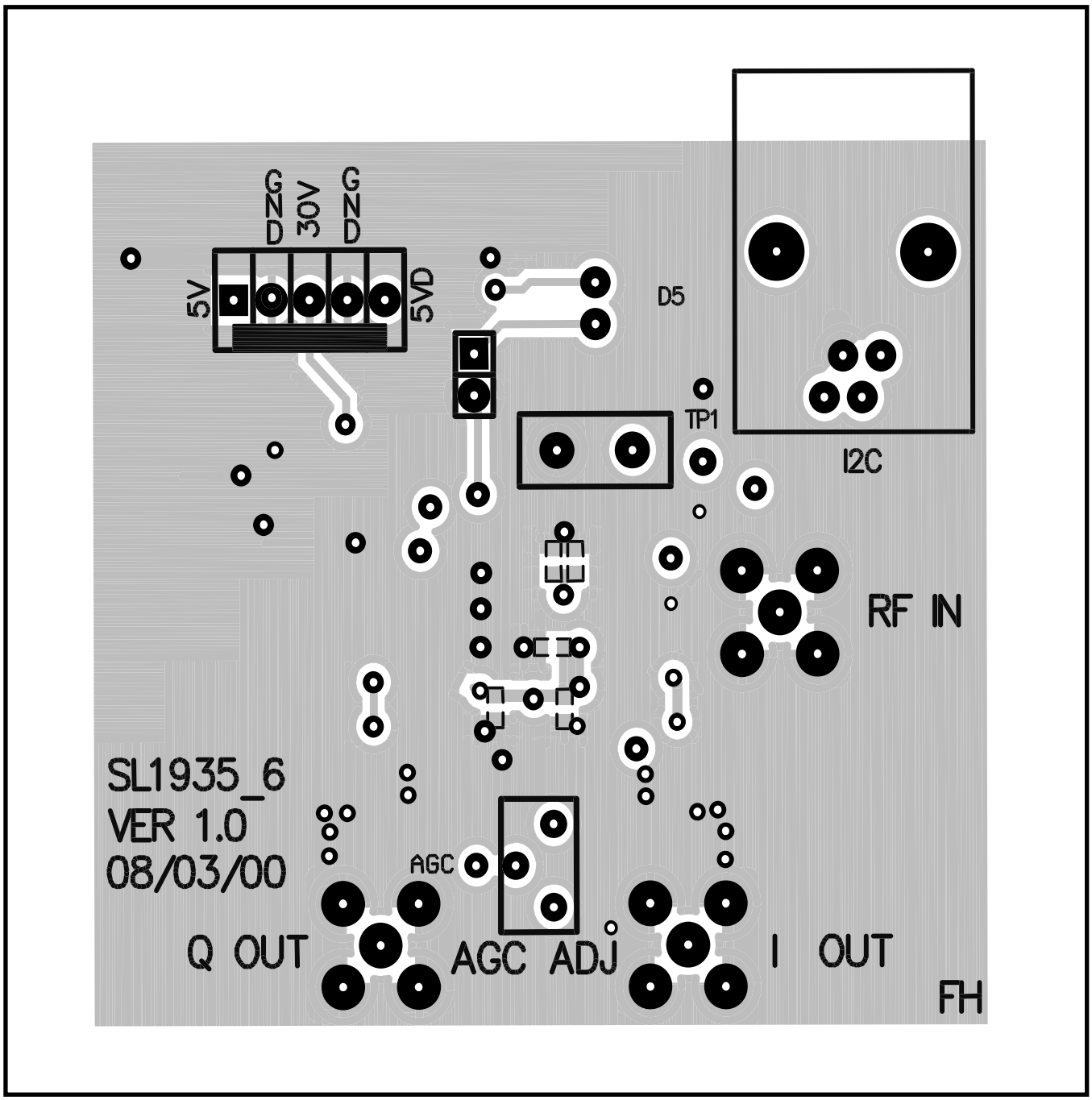


Figure 19. Top view

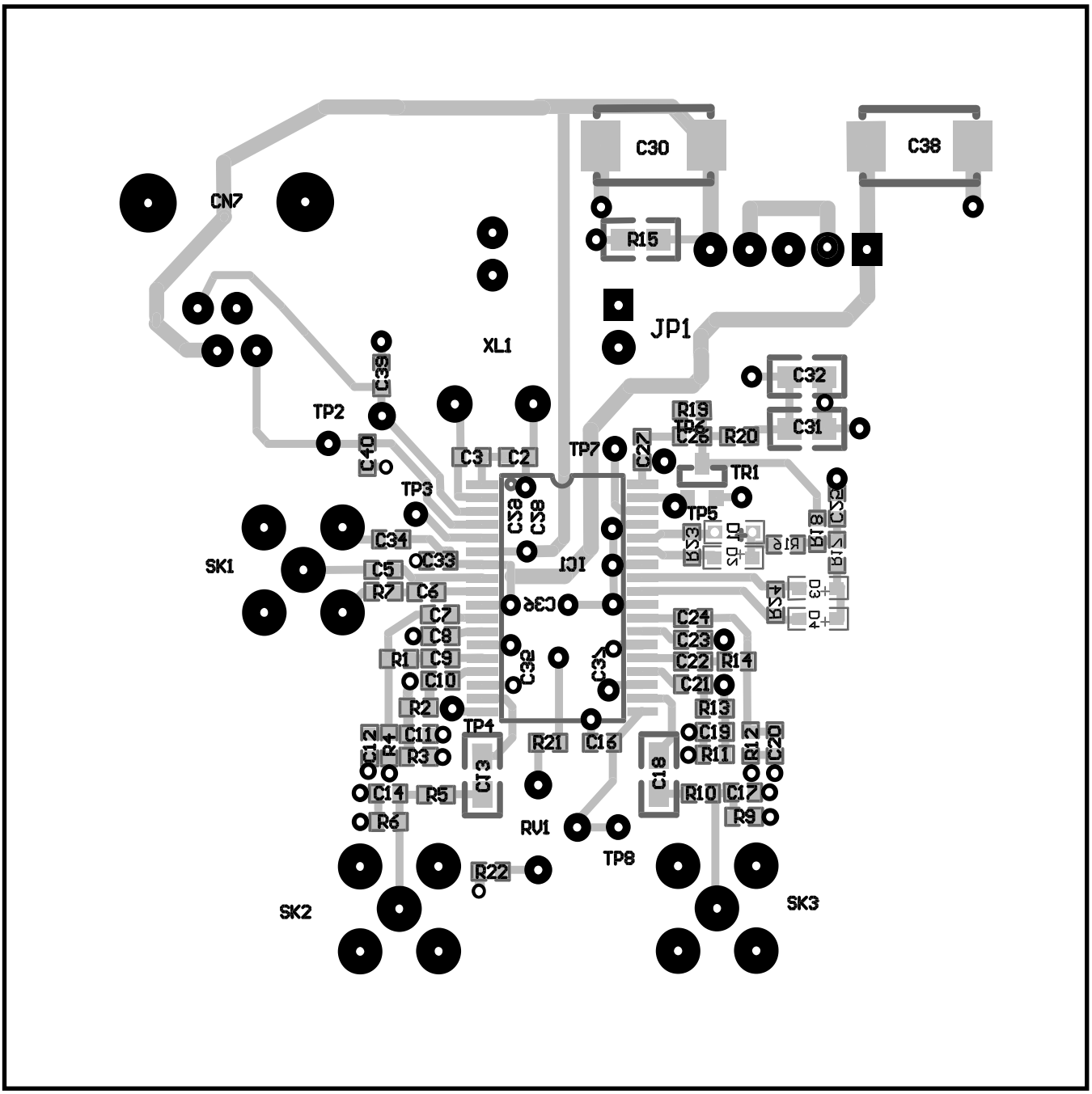


Figure 20. Bottom view

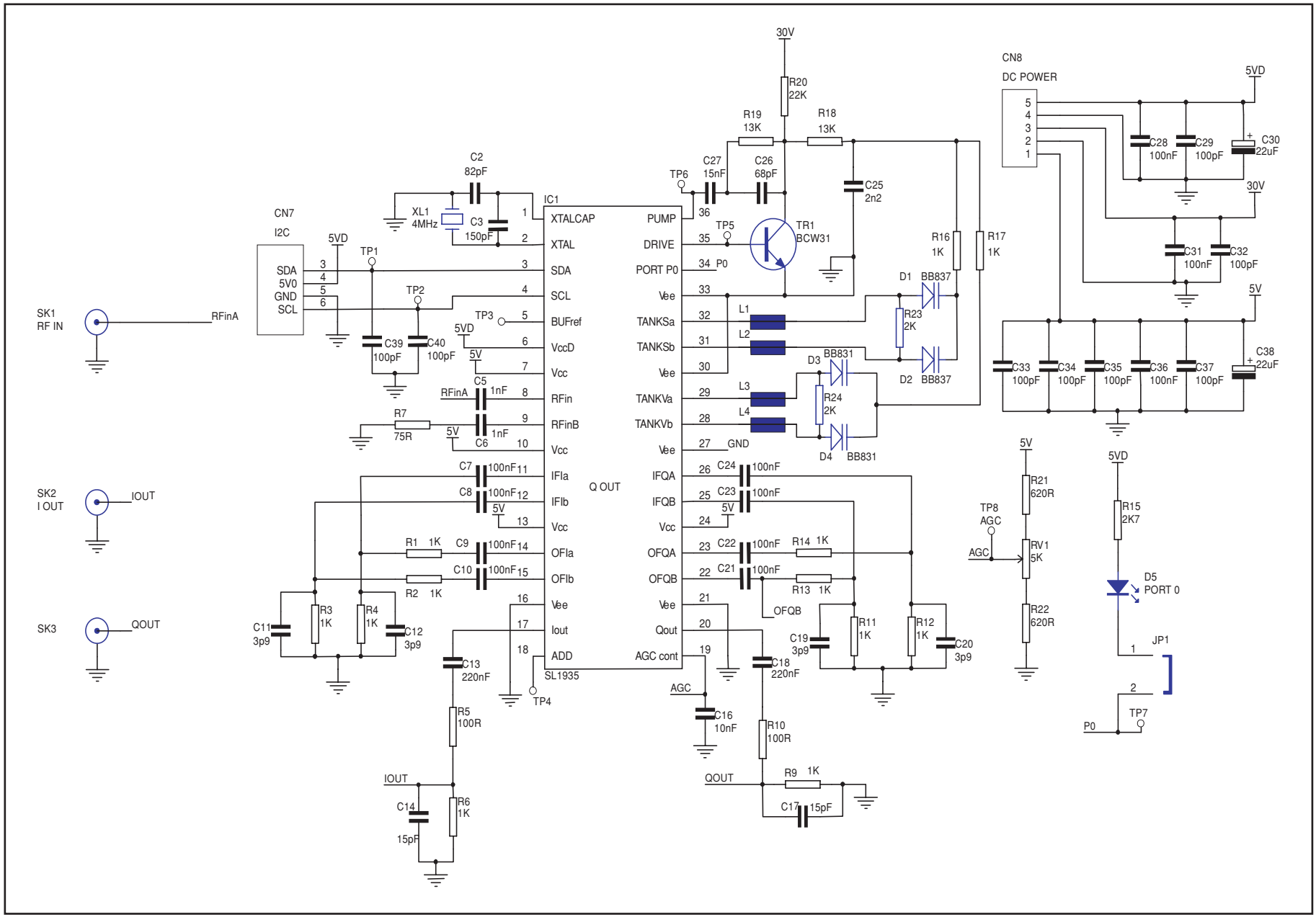
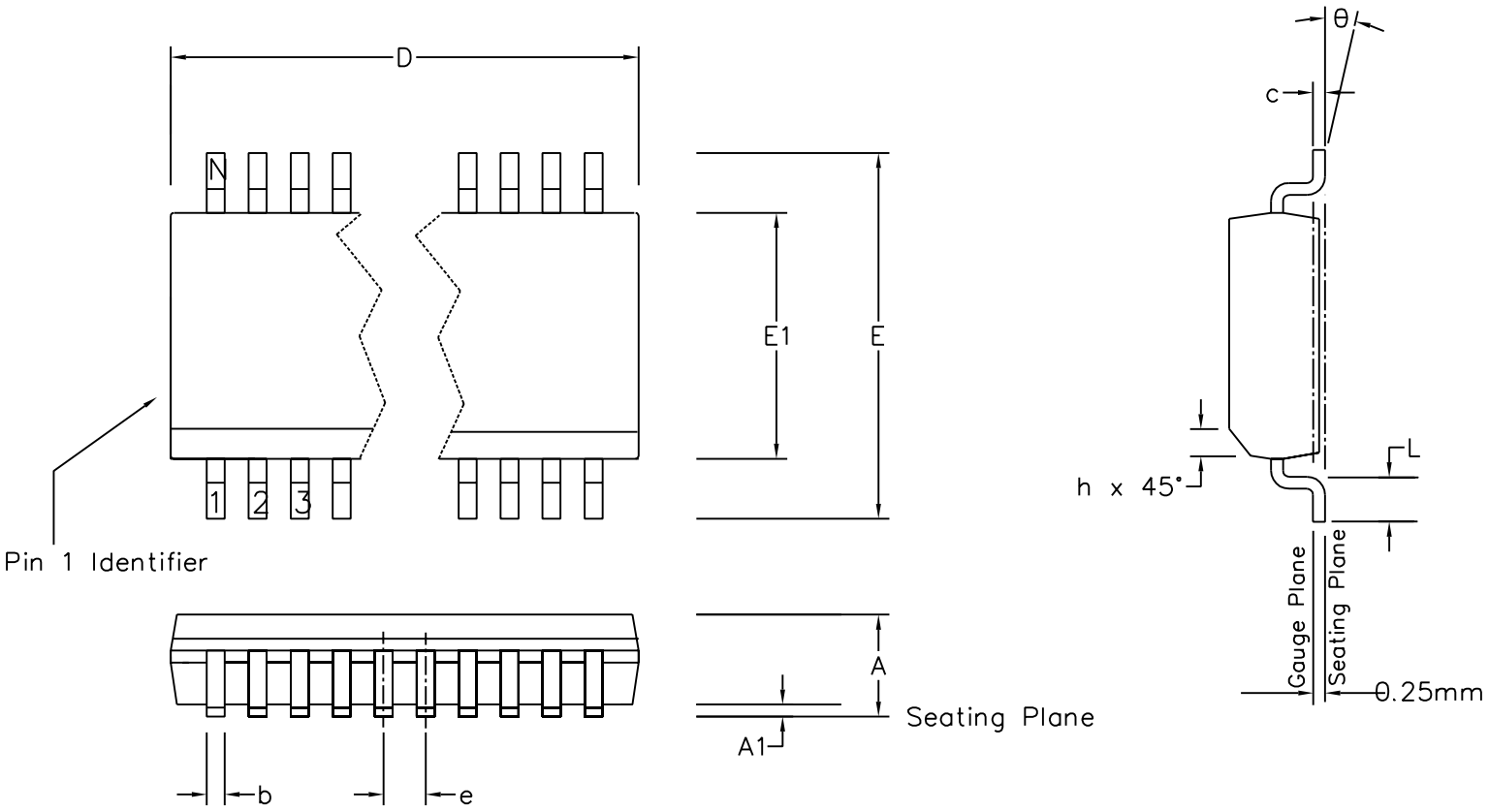

SK1
RF IN
RFinA
SK2
I OUT
IOUT
SK3
QOUT
CN7
I2C
SDA
5V0
GND
SCL
5VD
TP1
TP2
TP3
C39
100pF
C40
100pF
XL1
4MHz
C3
150pF
C2
82pF
IC1
XTALCAP
XTAL
SDA
SCL
BUFref
VccD
Vcc
RFin
RFinB
Vcc
IFIa
IFIb
Vcc
OFIa
OFIb
Vee
Iout
ADD
SL1935
Q OUT
PUMP
DRIVE
PORT P0
Vee
TANKSa
TANKSb
Vee
TANKVa
TANKVb
Vee
GND
IFQA
IFQB
Vcc
OFQA
OFQB
Vee
Qout
AGC cont
C5
1nF
C6
1nF
R7
75R
C7
100nF
C8
100nF
R1
1K
C9
100nF
C10
100nF
R2
1K
R3
1K
R4
1K
C11
3p9
C12
3p9
C13
220nF
R5
100R
C14
15pF
R6
1K
TP4
AGC
C16
10nF
R10
100R
QOUT
R9
1K
C17
15pF
C18
220nF
C19
3p9
C20
3p9
R11
1K
R12
1K
R13
1K
R14
1K
C22
100nF
C21
100nF
C24
100nF
C23
100nF
OFQB
30V
R20
22K
R19
13K
R18
13K
C27
15nF
C26
68pF
C25
2n2
TP6
TP5
TR1
BCW31
R16
1K
R17
1K
D1
BB837
D2
BB837
R23
2K
L1
L2
L3
L4
D3
BB831
D4
BB831
R24
2K
CN8
DC POWER
C28
100nF
C29
100pF
C30
22uF
C31
100nF
C32
100pF
C33
100pF
C34
100pF
C35
100pF
C36
100nF
C37
100pF
C38
22uF
TP8
AGC
R21
620R
RV1
5K
R22
620R
R15
2K7
D5
PORT 0
JP1
TP7
P0

Figure 21.

Purchase of Zarlink Semiconductor I²C components conveys a licence under the Phillips I²C Patent rights to use these components in an I²C system,provided that the system conforms to the I²C Standard Specification as defined by Phillips.



Symbol	Altern. Dimensions in inches		Control Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.096	0.104	2.44	2.64
A1	0.004	0.012	0.10	0.30
D	0.598	0.612	15.20	15.54
E1	0.291	0.299	7.40	7.60
E	0.398	0.414	10.11	10.51
L	0.016	0.050	0.40	1.27
e	0.0315 BSC.		0.80 BSC.	
b	0.011	0.020	0.28	0.51
c	0.009	0.013	0.23	0.32
θ	0°	8°	0°	8°
h	0.010	0.030	0.25	0.75
	Pin features			
N	36			
NON JEDEC STANDARD DRAWING				

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M – 1982
2. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located at pin 1 position.
3. Controlling dimensions are in millimeters
4. D & E1 do not include mould flash or protrusion. But do include mold mismatch.
5. Dimension E1 does not include inter–lead flash or protrusion. These shall not exceed 0.010" per side.
6. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension.
7. Not to Scale

ISSUE	1	2	3	
ACN	6741	207728	212423	
DATE	14MAR95	5NOV99	22Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

NP / N

Package Code DD

Package Outline for
36 lead SSOP
(7.5mm Body Width)

GPD00008

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE