N- and P- Channel Enhancement-Mode Dual MOSFET

Features

- Low threshold
- Low on resistance
- Low input capacitance
- Fast switching speeds
- Freedom from secondary breakdown
- Low input and output leakage
- Independent, electrically isolated N- and P-channels

Applications

- Medical ultrasound transmitters
- High voltage pulsers
- Amplifiers
- Buffers
- Piezoelectric transducer drivers
- General purpose line drivers

General Description

The Supertex TC6320 consists of high voltage low threshold N-channel and P-channel MOSFETs in an SO-8 package. Both MOSFETs have integrated gate-source resistors and gate-source zener diode clamps which are desired for high voltage pulser applications. The TC6320 is a complimentary, high-speed, high voltage, gate-clamped N- and P-channel MOSFET pair in an SO-8 package. These low threshold enhancement-mode (normally-off) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS}		$R_{DS(ON)}$ (MAX)	
	8-Lead SOIC (Narrow Body)		N-Channel	P-Channel	N-Channel	P-Channel
TC6320	TC6320TG	TC6320TG-G	200V	-200V	7.0Ω	8.0Ω

-G indicates package is RoHS compliant ('Green')

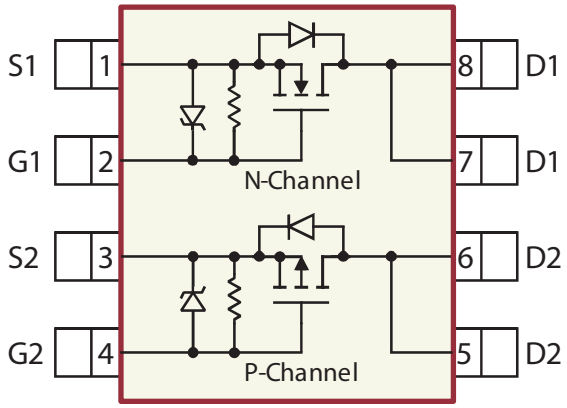
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV_{DSS}
Drain to gate voltage	BV_{DGS}
Operating and storage temperature	-55°C to +150°C
Soldering temperature[1]	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

***Note 1**. Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



SO-8 Package
(top view)

N- Channel Electrical Characteristics *(T_J = 25°C unless otherwise specified)*

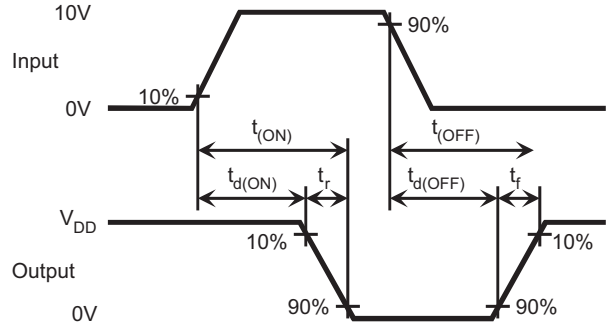
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	200	-	-	V	V_{GS} = 0V, I_D = 2.0mA
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
R_{GS}	Gate-Source Shunt Resistor	10	-	50	KΩ	I_{GS} = 100µA
ΔR_{GS}	Change in RGS with Temperature	-	-	TBD	%/°C	I_{GS} = 100µA
VZ_{GS}	Gate-Source Zener Voltage	13.2	-	25	V	I_{GS} = 2.0mA
ΔVZ_{GS}	Change in VZGS with Temperature	-		TBD	mV/°C	I_{GS} = 2.0mA
I_{DSS}	Zero gate voltage drain current	-	-	10.0	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-state drain current	1.0	-	-	A	V_{GS} = 4.5V, V_{DS} = 25V
		2.0	-	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	8.0	Ω	V_{GS} = 4.5V, I_D = 150mA
		-	-	7.0		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	V_{GS} = 4.5V, I_D =150mA
G_{FS}	Forward transconductance	400	-	-	mmho	V_{DS} = 25V, I_D = 200mA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common source output capacitance	-	-	60		
C_{RSS}	Reverse transfer capacitance	-	-	23		
$t_{d(ON)}$	Turn-ON delay time	-	-	10	ns	V_{DD} =25V, I_D = 1.0A, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 0.5A
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 0.5A

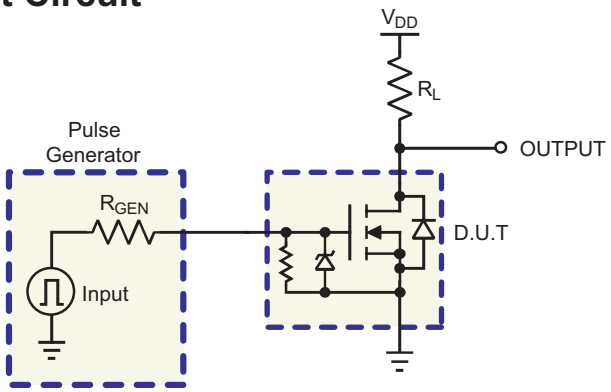
Notes:

1.All D.C. parameters 100% tested at 25C unless otherwise stated. (Pulse test: 300s pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

N- Channel Switching Waveforms and Test Circuit





P- Channel Electrical Characteristics *(T_J = 25°C unless otherwise specified)*

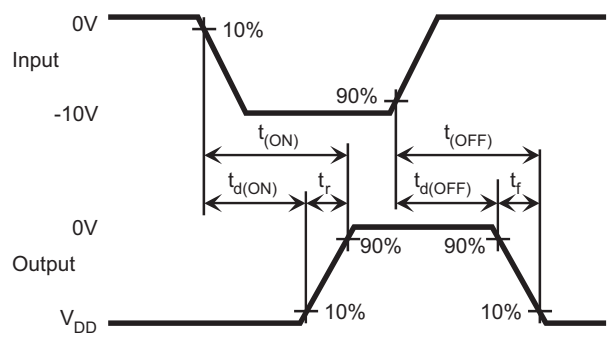
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-200	-	-	V	V_{GS} = 0V, I_D = -2.0µA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
R_{GS}	Gate-source shunt resistor	10	-	50	KΩ	I_{GS} = 100µA
ΔR_{GS}	Change in R_{GS} with temperature	-	-	TBD	%/°C	I_{GS} = 100µA
VZ_{GS}	Gate-source zener voltage	13.2	-	25	V	I_{GS} = -2mA
ΔVZ_{GS}	Change in RGS with temperature	-	-	TBD	mV/°C	I_{GS} = -2mA
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-state drain current	-1.0	-	-	A	V_{GS} = -4.5V, V_{DS} = -25V
		-2.0	-	-		V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	10	Ω	V_{GS} = -4.5V, I_D = -150mA
		-	-	8.0		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	V_{GS} = -10V, I_D =-200mA
G_{FS}	Forward transconductance	400	-	-	mmho	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input capacitance	-	-	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz
C_{OSS}	Common source output capacitance	-	-	55		
C_{RSS}	Reverse transfer capacitance	-	-	30		
$t_{d(ON)}$	Turn-ON delay time	-	-	10	ns	V_{DD} = -25V, I_D = -1.0A, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	V_{GS} = 0V, I_{SD} = -0.5A
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -0.5A

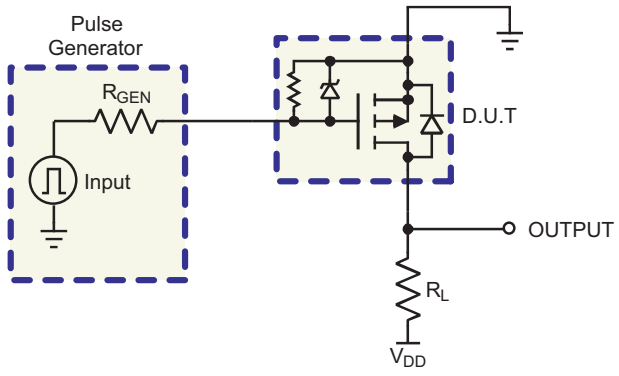
Notes:

1.All D.C. parameters 100% tested at 25C unless otherwise stated. (Pulse test: 300s pulse, 2% duty cycle.)

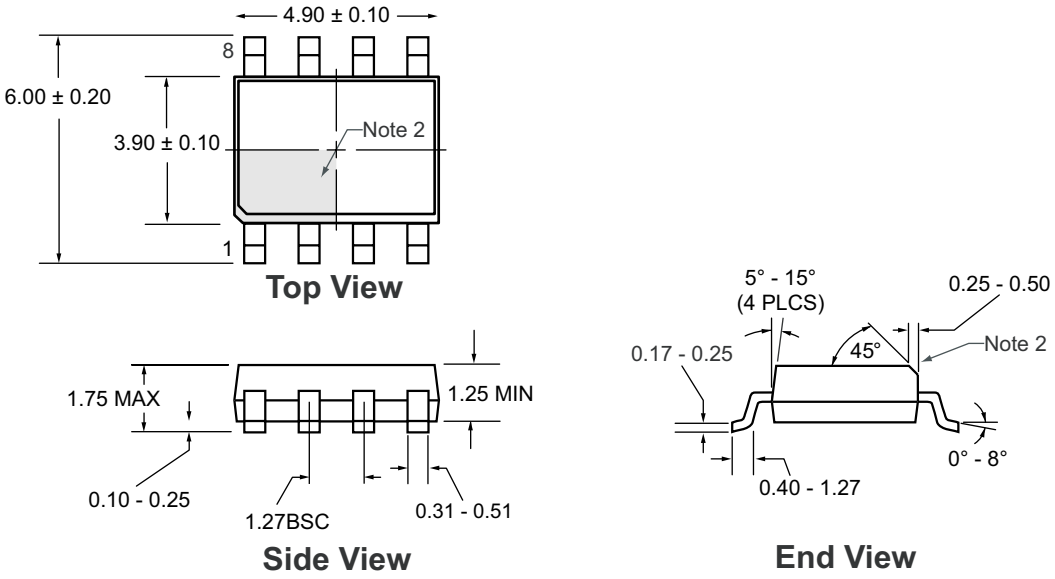
2.All A.C. parameters sample tested.

P- Channel Switching Waveforms and Test Circuit





8-Lead SO (TG) Package Outline



Notes:

1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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