87C196KB/87C196KB16
HIGH PERFORMANCE CHMOS MICROCONTROLLER

- 8 Kbytes of On-Chip EPROM
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 1.75 μs 16 x 16 Multiply (16 MHz)
- 3.0 μs 32/16 Divide (16 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- 12 MHz and 16 MHz Available
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ Bus Protocol

The 87C196KB is a 16-bit microcontroller with 8 Kbytes of on-chip EPROM and a high performance member of the MCS®-96 microcontroller family. The 87C196KB is 8096BH compatible and uses a true superset of the 8096BH instructions. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

Bit, byte, word and some 32-bit operations are available on the 87C196KB. With a 16 MHz oscillator a 16-bit addition takes 0.50 μs, and the instruction times average 0.37 μs to 1.1 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

The 87C196KB has a maximum guaranteed frequency of 12 MHz. The 87C198KB16 has a maximum guaranteed frequency of 16 MHz. All references to the 87C196KB also refer to the 87C196KB16 unless otherwise noted.

November 1991
Order Number: 270909-003

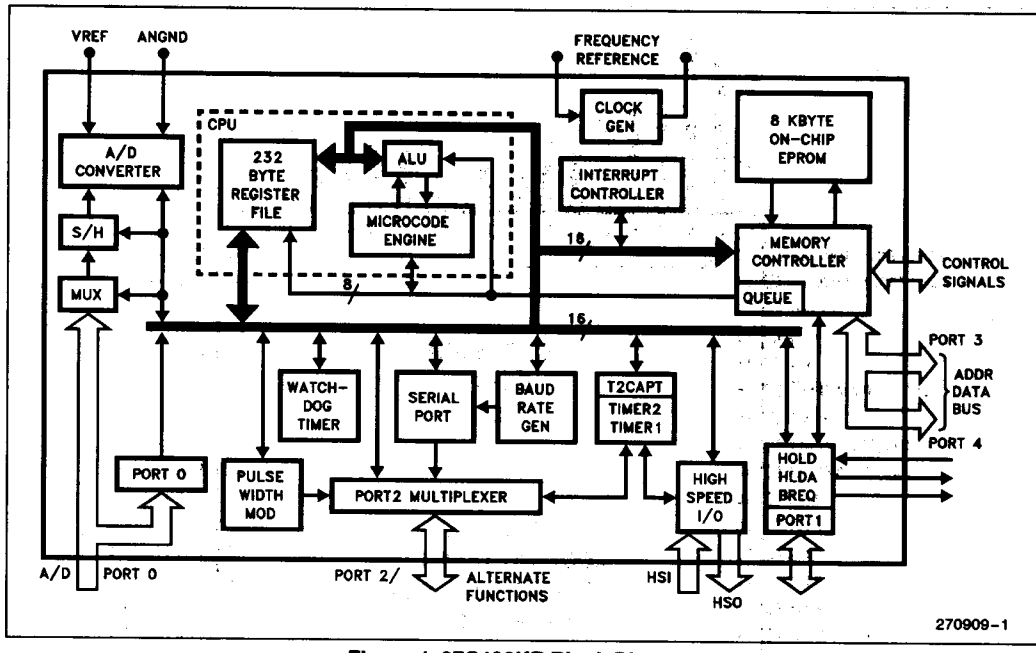

Figure 1. 87C196KB Block Diagram

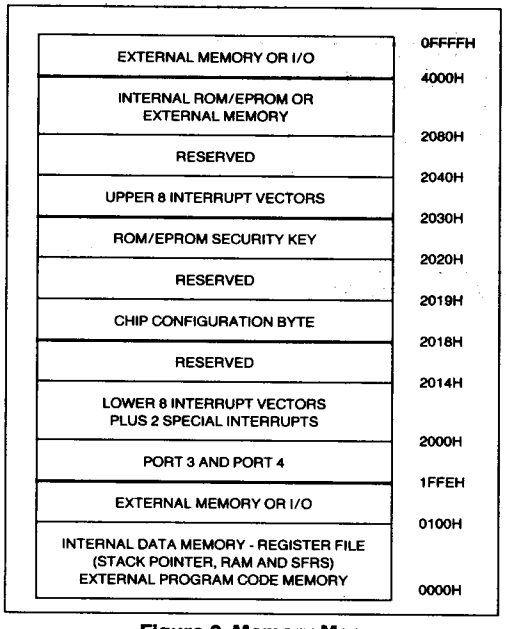

Figure 2. Memory Map

PACKAGING

The 87C196KB is available in the 68-pin PLCC and 80-pin Quad Flat Pack (One-Time Programmable) packages. Contact your local sales office to determine the exact ordering code for the part desired.

Package Designators: N = 68-pin PLCC
S = 80-pin QFP

Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	12°C/W
QFP	70°C/W	4°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

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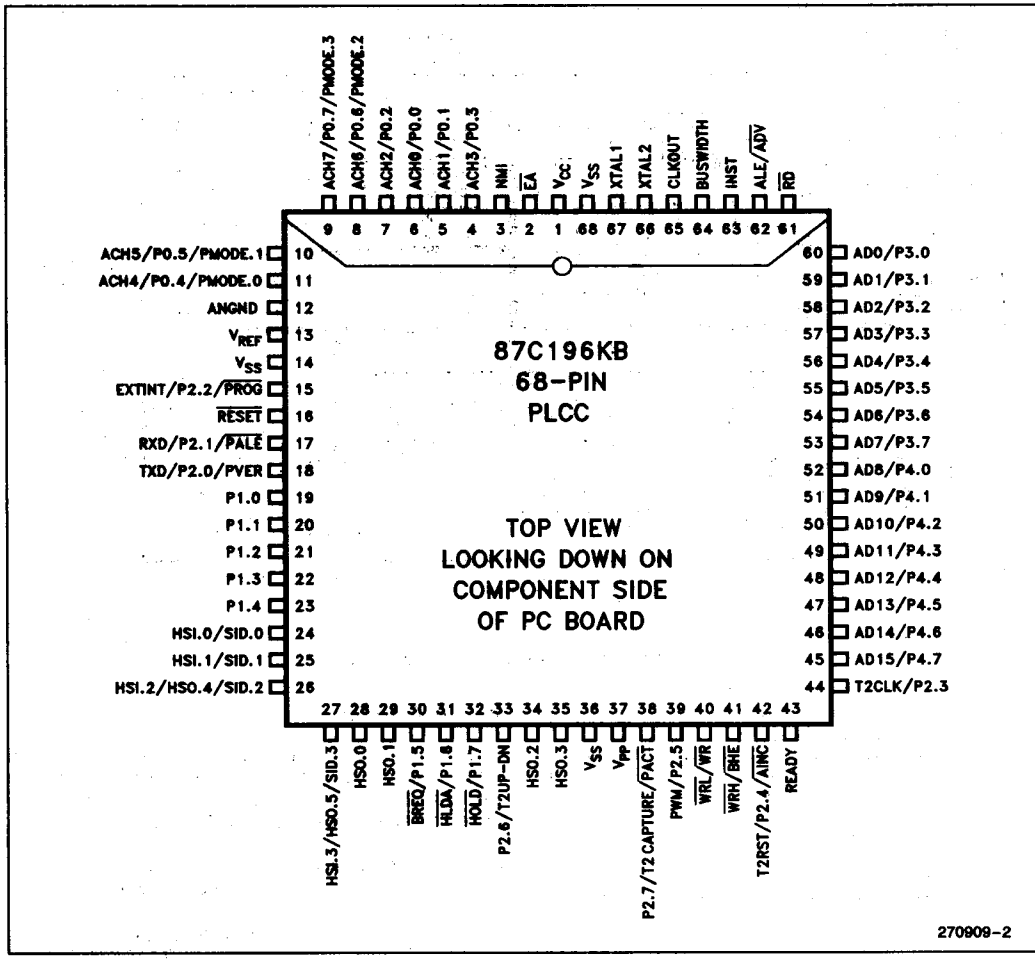
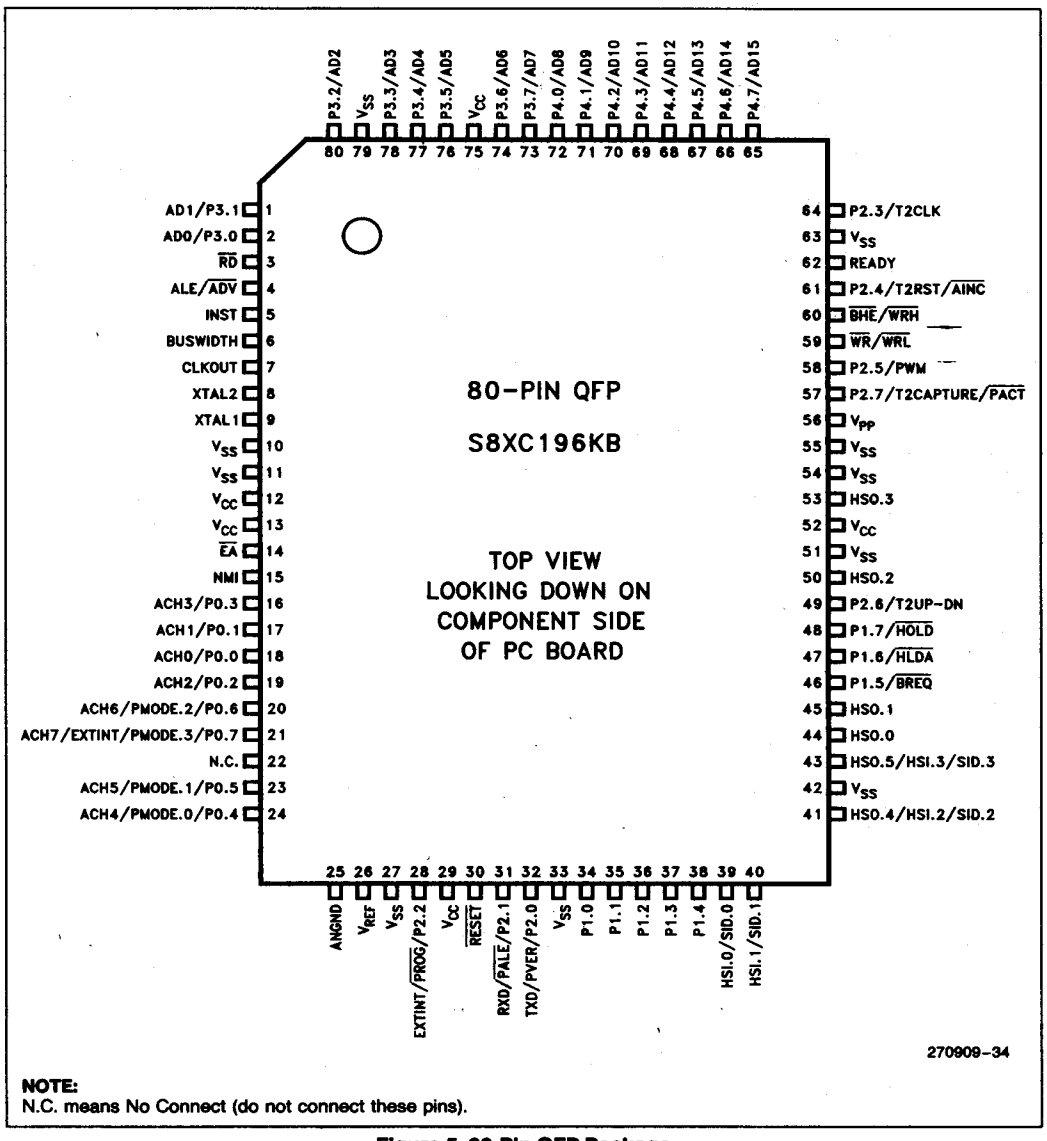


Figure 3. 68-Pin Package (PLCC—Top View)



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 5. 80-Pin QFP Package

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being addressed. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB. Pins P2.6 and P2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus, which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. In Mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. In Mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2.
PWM	The PWM output.
T2UP-DN	The T2UPDN pin controls the direction of Timer2 as an up or down counter.
T2CAPTURE	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register.
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
Ports 3 and 4 (Programming Mode)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} (15 kΩ).

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ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage from V_{PP} or $\overline{EA}$ to
V_{SS} or ANGND ..... −0.3V to +13.0V
Voltage On Any Other Pin to V_{SS} .. −0.5V to +7.0V
Power Dissipation(1) 1.5W

NOTE:
1. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency **12 MHz**	3.5	12	MHz
F_{OSC}	Oscillator Frequency **16 MHz**	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage(1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	µA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		+3	µA	0 < V_{IN} < V_{REF}
I_{TL}	1 to 0 Transition Current (QBD Pins)		−650	µA	V_{IN} = 2.0V
I_{IL}	Logical 0 Input Current (QBD Pins)(4)		−50	µA	V_{IN} = 0.45V

NOTE:
All pins except RESET and XTAL1.

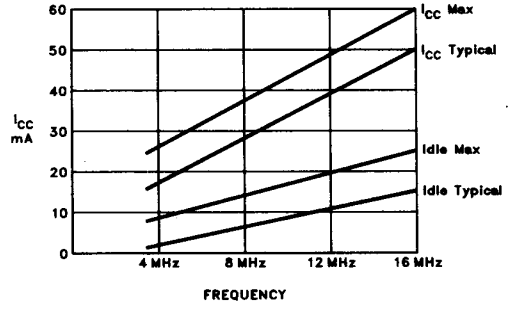
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(7)	Max	Units	Test Conditions
I_{IL1}	Logical 0 Input Current in Reset ALE, $\overline{RD}$, INST			−7	mA	V_{IN} = 0.45V
I_{IH1}	Logical 1 Input Current on NMI Pin			100	μA	V_{IN} = 2.0V
Hyst.	Hysteresis on RESET Pin	300			mV	
I_{CC}	Active Mode Current in Reset		50	60	mA	XTAL1 = 16 MHz V_{CC} = V_{PP} = V_{REF} = 5.5V
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		10	25	mA	
I_{CC1}	Active Mode Current		15	25	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		5	30	μA	V_{CC} = V_{PP} = V_{REF} = 5.5V
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, CDE, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and V_{REF} = V_{CC} = 5V.



I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

Figure 6. I_{CC} and I_{IDLE} vs Frequency

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AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The system must meet these specifications to work with the 87C196KB:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 60$	ns	
T_{YLYH}	NonREADY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$ where n = number of wait states.

AC CHARACTERISTICS (Continued)

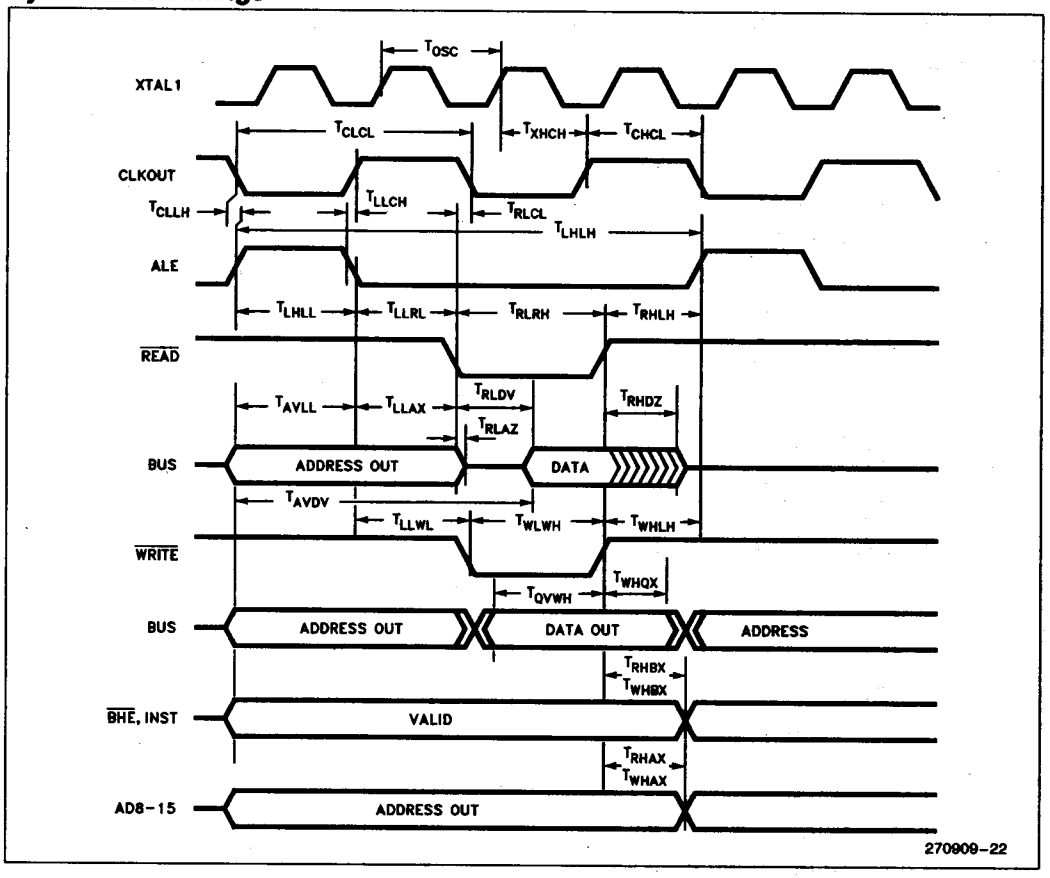
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The 87C196KB will meet these specifications:

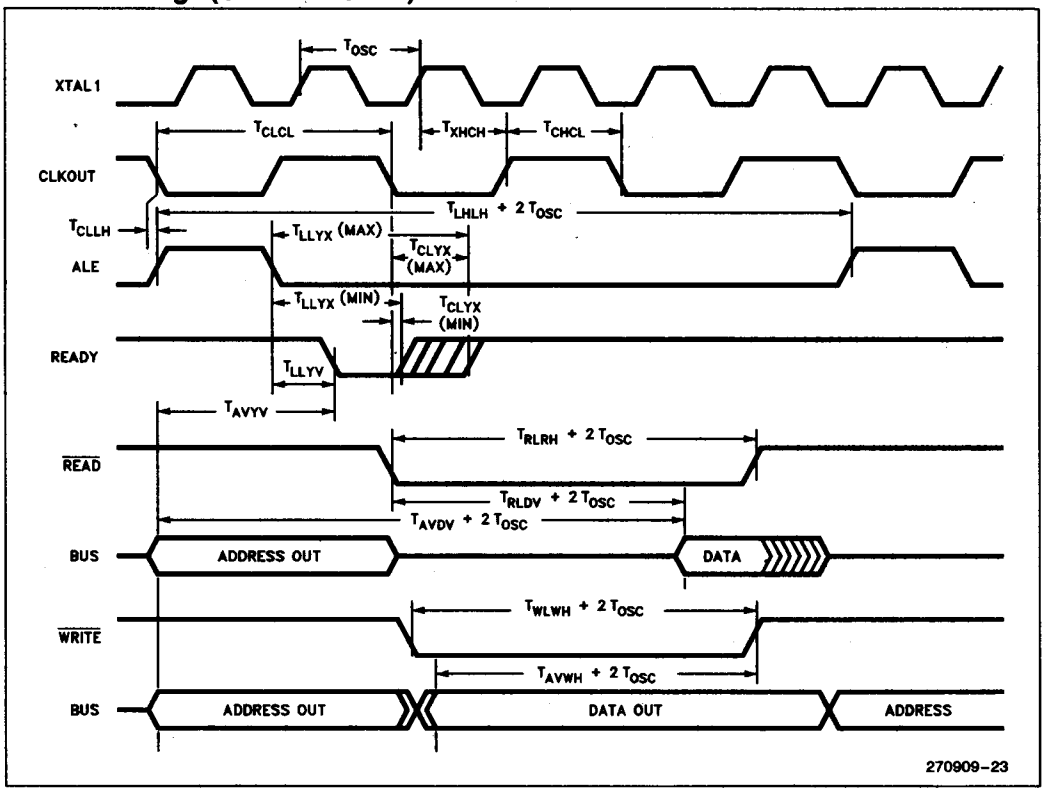
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **12 MHz**	3.5	12.0	MHz	(Note 2)
F_{XTAL}	Frequency on XTAL1 **16 MHz**	3.5	16.0	MHz	(Note 2)
T_{OSC}	$1/F_{XTAL}$ **12 MHz**	83.3	286	ns	
T_{OSC}	$1/F_{XTAL}$ **16 MHz**	62.5	286	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	+10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	(Note 3)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST HOLD after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{RHBX}	$\overline{BHE}$, INST HOLD after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8–15 hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Assuming back-to-back bus cycles.
2. Testing performed at 3.5 MHz, however, the device is static by design and will typically operate below 1 Hz.
3. When using wait states, all 2 T_{OSC} + n where n = number of wait states.

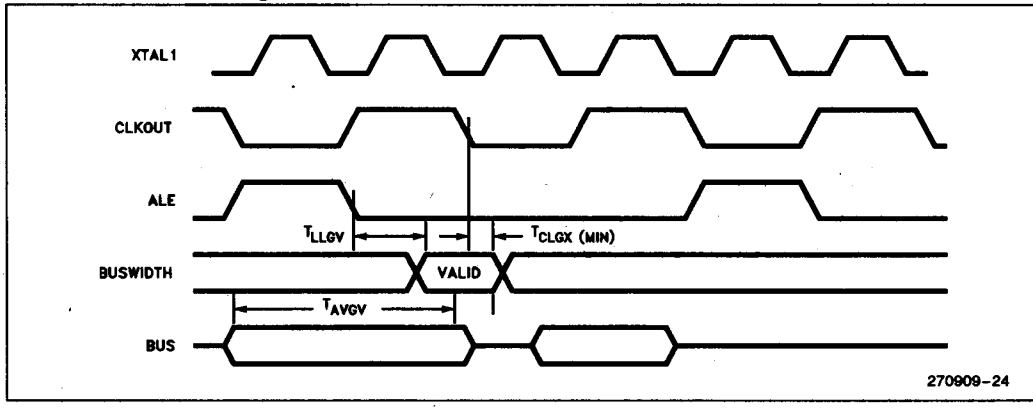
System Bus Timings



READY Timings (One Wait State)



Buswidth Bus Timings



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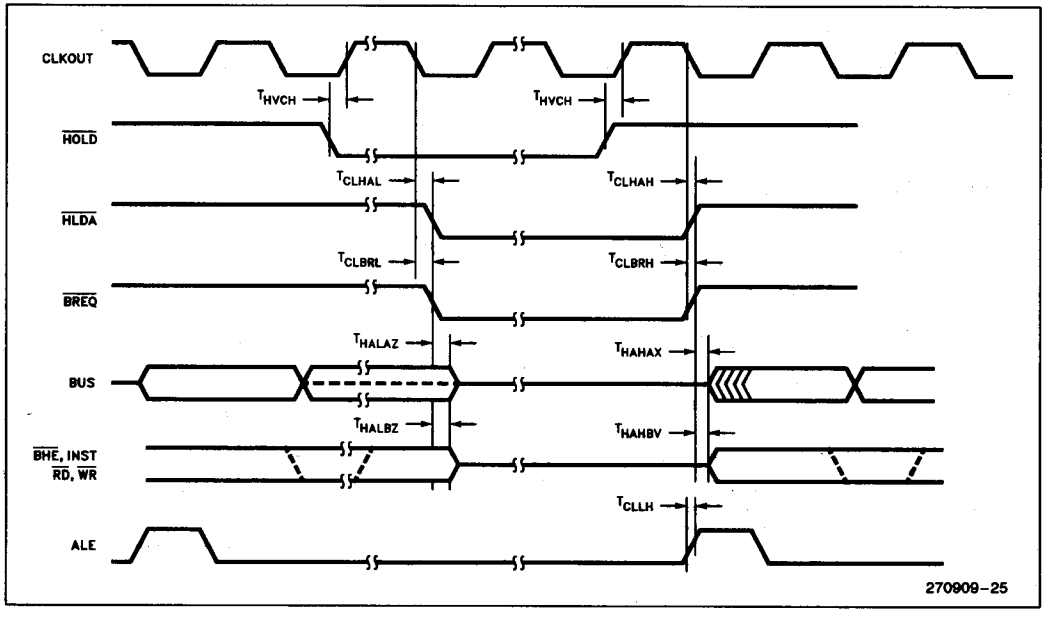
HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to HLDA Low		15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low		15	ns	
T_{HALAZ}	HLDA Low to Address Float		10	ns	
T_{HALBZ}	HLDA Low to BHE, INST, RD, WR Float		10	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−15		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

Maximum Hold Latency

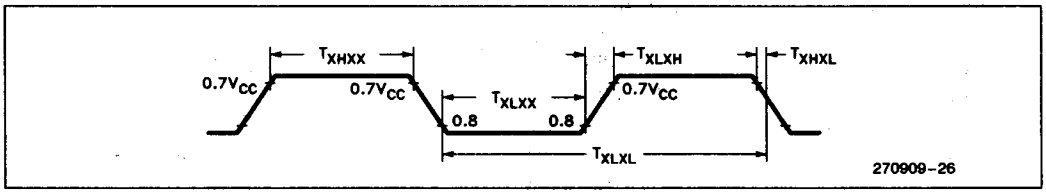
Bus Cycle Type	Latency
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External	4.5 States



EXTERNAL CLOCK DRIVE

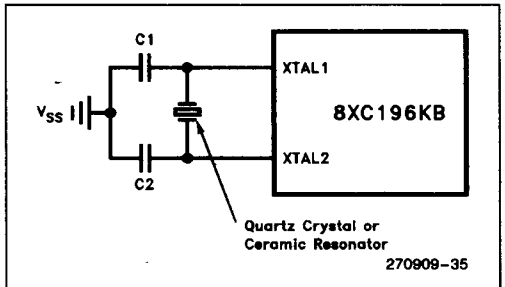
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency **12 MHz**	3.5	12.0	MHz
$1/T_{XLXL}$	Oscillator Frequency **16 MHz**	3.5	16	MHz
T_{XLXL}	Oscillator Period **12 MHz**	83.3	286	ns
T_{XLXL}	Oscillator Period **16 MHz**	62.5	286	ns
T_{XHXX}	High Time	21.25		ns
T_{XLXX}	Low Time	21.25		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



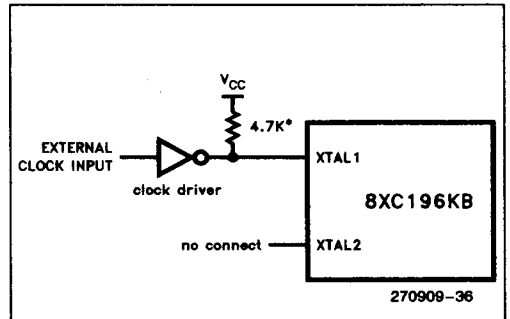
An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications, the capacitance will not exceed 20 pF.

EXTERNAL CRYSTAL CONNECTIONS



NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



* Required if TTL driver used
Not needed if CMOS driver is used.

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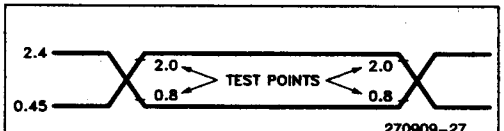
AC TESTING INPUT, OUTPUT WAVEFORMS



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AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS

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For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

- H - High
- L - Low
- V - Valid
- X - No Longer Valid
- Z - Floating

Signals:

- A - Address
- B - $\overline{BHE}$
- BR - $\overline{BREQ}$
- C - CLKOUT
- D - DATA IN
- G - Buswidth
- H - $\overline{HOLD}$
- HA - $\overline{HLDA}$
- L - ALE/$\overline{ADV}$
- Q - DATA OUT
- R - $\overline{RD}$
- W - $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
- X - XTAL1
- Y - READY

10-BIT A/D CHARACTERISTICS

The speed of the A/D converter in the 10-bit mode can be adjusted by setting a clock prescaler on or off. At high frequencies more time is needed for the comparator to settle. The maximum frequency with the clock prescaler disabled is 6 MHz. The conversion times with the prescaler turned on or off is shown in the table below. The AD_TIME register has not been characterized for the 10-bit mode.

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Converter Quick Reference for defintion of A/D terms.

Conversion Time

Clock Prescaler On IOC2.4 = 0	Clock Prescaler Off IOC2.4 = 1
156.5 States 19.5 μs @ 16 MHz	89.5 States 29.8 μs @ 6 MHz

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	−0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±3	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Time: Prescaler On Prescaler Off	15 8			States States	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

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EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages During Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	12.50	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}	Oscillator Frequency **12 MHz**	6.0	12.0	MHz
F_{OSC}	Oscillator Frequency **16 MHz**	6.0	16.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

AC EPROM PROGRAMMING CHARACTERISTICS

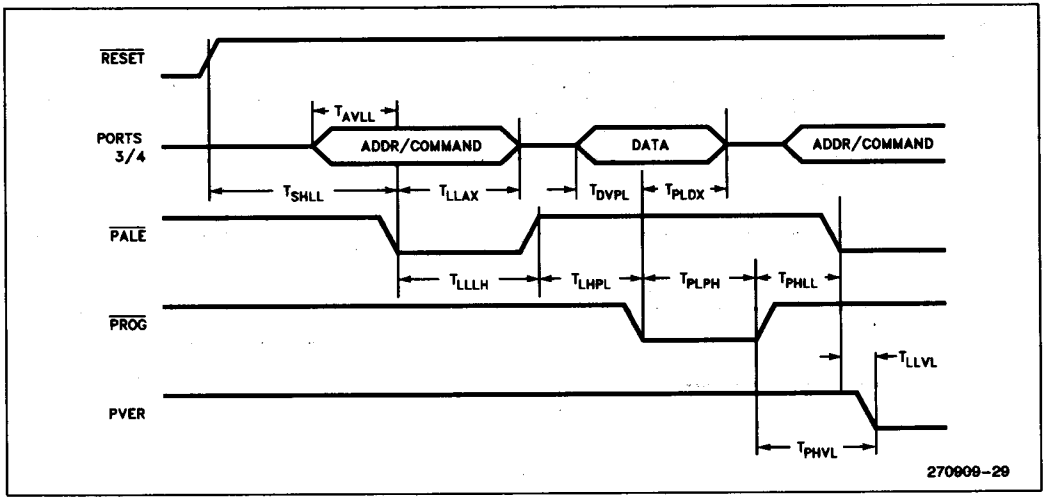
Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	40		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	50		T_{OSC}
T_{LLVL}	$\overline{PALE}$ Low to PVER Low		60	T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	40		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	120		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	120		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	40		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Low		90	T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

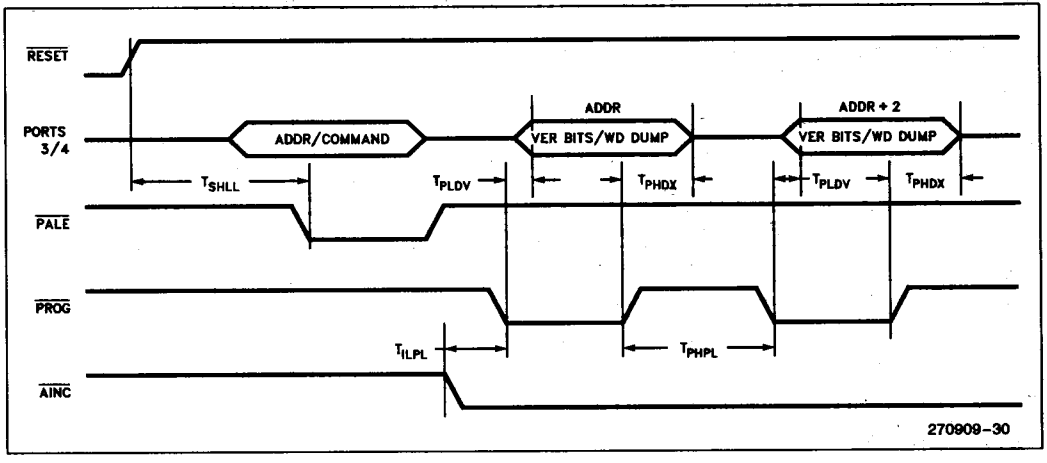
Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



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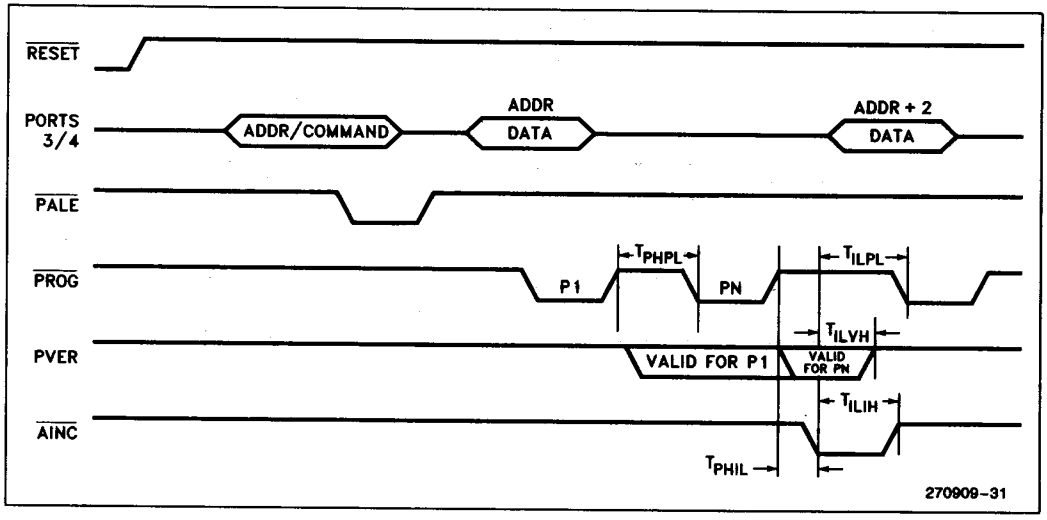
SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



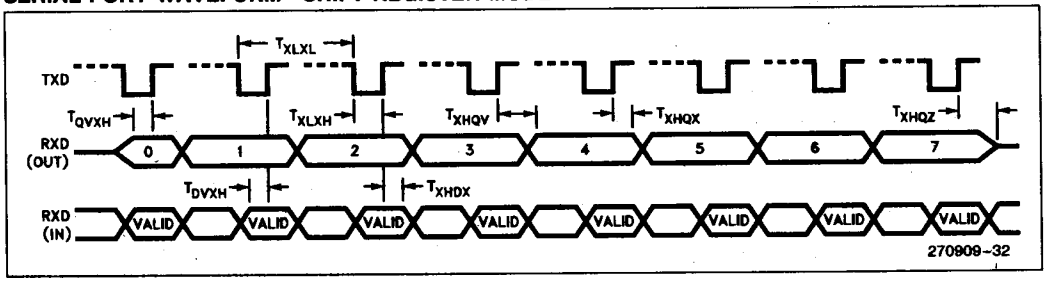
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} + 50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



FUNCTIONAL DEVIATIONS

Devices marked with a "E" have the following errata.

High Speed Inputs

The High Speed Input (HSI) has three deviations from the specifications. These deviations applied to devices covered by the previous data sheet (see Revision History) but they were not documented.

NOTE:
"Events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine state may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an empty FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

REVISION HISTORY

This data sheet (270909-003) is valid for devices with an "E" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet and the previous version (-002).

1. The 12 MHz and 16 MHz devices were combined in this data sheet. The 87C196KB 12 MHz only data sheet (272035-001) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed.
3. The -002 version of this data sheet was valid for devices marked with a "B" or a "D" at the end of the top side tracking number.
4. The OSCILLATOR errata was removed.
5. An errata was not documented in the -002 data sheet for devices marked with a "B" or a "D". This is the DIVIDE DURING HOLD/READY errata. When HOLD or READY is active and DIV/DIVB is the last instruction in the queue, the divide result may be incorrect.
6. T_{XCH} was changed from Min = 40 ns to Min = 20 ns.
7. T_{RLCL} was changed from Min = 5 ns to Min = 4 ns.
9. I_{IL1} was changed from Max = −6 mA to Max = −7 mA.
10. T_{HAHBV} was changed from Min = −10 ns to Min = −15 ns.

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Differences between the -002 and -001 data sheets.

1. The -001 version of this data sheet was valid for devices marked with a "C" at the end of the top side tracking number.
2. Added 64L SDIP and 80L QFP packages.
3. Added IIH1.
4. Changed T_{CHWH} Min from − 10 ns to − 5 ns.
5. Changed T_{CHWH} Max from + 10 ns to + 15 ns.
6. Changed T_{WLWH} Min from T_{OSC} − 20 ns to T_{OSC} − 15 ns.
7. Changed T_{WHQX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
8. Changed T_{WHLH} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
9. Changed T_{WHLH} Max from T_{OSC} + 15 ns to T_{OSC} + 10 ns.
10. Changed T_{WHBX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
11. Changed T_{HVCH} Min from 85 ns to 55 ns.
12. Remove T_{HVCH} Max.
13. Changed T_{CLHAL} Min from − 10 ns to − 15 ns.
14. Changed T_{CLHAL} Max from 20 ns to 15 ns.
15. Changed T_{CLBRL} Min from − 10 ns to − 15 ns:
16. Changed T_{CLBRL} Max from 20 ns to 15 ns.
17. Changed T_{HAHAX} Min from − 10 ns to − 15 ns.
18. Added HSI description to Functional Deviations.
19. Added Oscillator description to Functional Deviations.