

The MP62260-1/MP62261-1 Power Distribution

Switch features internal current limiting to

prevent damage to host devices due to faulty

load conditions. The MP62260-1/MP62261-1

operates from 2.7V to 5.5V nominal input

voltage and includes a 45mΩ Power MOSFET

to handle up to 2A continuous load with a 3A

typical current limit. The MP62260-1/MP62261-

1 has built-in protection for both over current

and increased thermal stress. For over-current

protection (OCP), the device will limit the

When continuous output overload condition

exceeds power dissipation of the package, the

thermal protection will shut the part off. The device will recover once the device temperature

The MP62260-1/MP62261-1 involves output discharge function that provides a resistive

discharge path for the external output capacitor

The MP62260-1/MP62261-1 is available in

current by going into a constant current mode.

DESCRIPTION

MP62260-1/MP62261-1

3.3V/5V, Single-Channel 2A Current-Limited Power Distribution Switch with Output Discharge

FEATURES

- 2A Continuous Current
- 3A Accurate Current Limit
- Output Discharge Function
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 45mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- SOIC8 Package

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

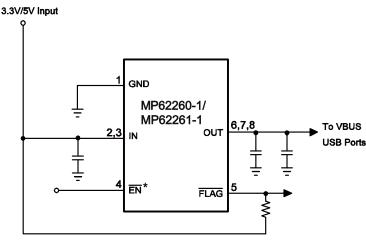
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TYPICAL APPLICATION

reduces to approx 120°C.

when the part is disabled.

SOIC8 package.



SINGLE-CHANNEL (*is active high for MP62261-1)

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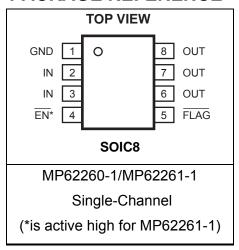
ORDERING INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short- Circuit Current @ T _A =25°C	Package	Top Marking	Free Air Temperature (T _A)
MP62260DS-1*	Active Low	Single	2A	3A	SOIC8	62260DS1	-40°C to +85°C
MP62261DS-1	Active High	Single	2A	3A	SOIC8	62261DS1	-40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP62260DS-1–Z).

For RoHS Compliant Packaging, add suffix –LF (eg. MP62260DS-1–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN	0.3V to +6.0V
EN, FLAG, OUT to GND	0.3V to +6.0V
Continuous Power Dissipation	$(T_A = +25^{\circ}C)^{(2)}$
SOIC8	1.4W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C
Operating Junct. Temp (T _J)	-40°C to +125°C

Thermal Resistance (3)	$oldsymbol{ heta}_{JA}$	$oldsymbol{ heta}_{JC}$	
SOIC8	90	42	°C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB.



ELECTRICAL CHARACTERISTICS (4)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

Parameter	Condition	Min	Тур	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	Device Enabled, I _{OUT} =0		90	120	μA
Shutdown Current	Device Disabled, V _{OUT} =float, V _{IN} =5.5V		1		μA
Off Switch Leakage	Device Disabled, V _{IN} =5.5V		1		μA
Current Limit		2.2	3	3.8	Α
Trip Current	Current Ramp (slew rate≤100A/s) on Output		3.3	4.3	Α
Under-voltage Lockout	Rising Edge	1.95	2.30	2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	I _{OUT} =100mA and -40°C≤T _A ≤85°C		45	70	mΩ
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	I _{SINK} =5mA			0.4	V
FLAG Output High Leakage Current	V _{IN} =V _{FLAG} =5.5V			1	μΑ
Thermal Shutdown			140		°C
Thermal Shutdown Hysteresis			20		°C
V _{OUT} Rising Time, Tr ⁽⁵⁾	V_{IN} =5.5V, C_L =1uF, R_L =5 Ω		0.9		ms
V ₀₀₁ rusing rime, ri	V_{IN} =2.7V, C_L =1uF, R_L =5 Ω		1.7		ms
V _{OUT} Falling Time, Tf ⁽⁶⁾	V_{IN} =5.5V, C_L =1uF, R_L =5 Ω			0.5	ms
	V_{IN} =2.7V, C_L =1uF, R_L =5 Ω			0.5	ms
Turn On Time, Ton (7)	C _L =100μF, R _L =5Ω			3	ms
Turn Off Time, Toff (8)	C _L =100μF, R _L =5Ω			10	ms
Discharge Resistance			100		Ω
FLAG Deglitch Time		4	8	15	ms
EN Input Leakage		-1			μA
Reverse Leakage Current	V _{OUT} =5.5V, V _{IN} =GND		0.2		μA

⁴⁾ Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

⁵⁾ Measured from 10% to 90% output signal.

⁶⁾ Measured from 90% to 10% output signal.

Measured from (50%) EN signal to (90%) output signal. Measured from (50%) EN signal to (10%) output signal.

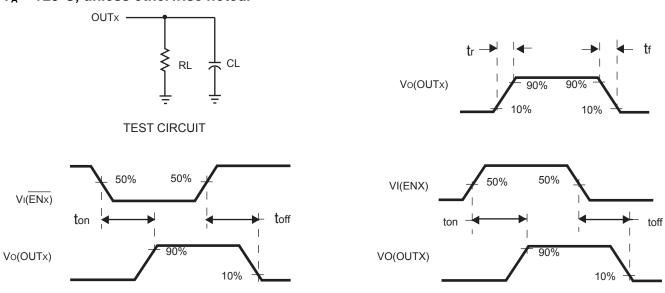


PIN FUNCTIONS

Pin # SOIC8	Name	Description
1	GND	Ground.
2, 3	IN	Input Voltage. Accepts 2.7V to 5.5V input.
4	EN	Active Low: (MP62260-1), Active High: (MP62261-1).
5	FLAG	IN-to-OUT Over-current, active-low output flag. Open-Drain.
6, 7, 8	OUT	IN-to-OUT Power-Distribution Output (for all 3 output pins).

TYPICAL PERFORMANCE CHARACTERISTICS

 $T_A = +25$ °C, unless otherwise noted.



VOLTAGE WAVEFORMS

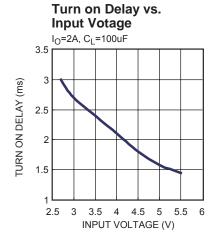
Figure 1—Test Circuit and Voltage Waveforms

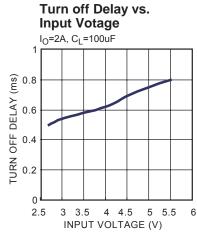
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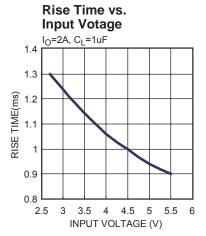


TYPICAL PERFORMANCE CHARACTERISTICS

 V_{IN} =5V, V_{EN} =0V for MP62260-1, V_{CC} =5V, C_L =2.2uF, T_A =25 $^{\circ}$ C unless otherwise noted.







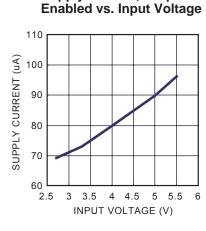
Static Drain-Source On-State

Resistance Variation vs.

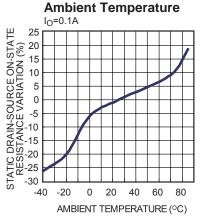
Fall Time vs. Input Votage

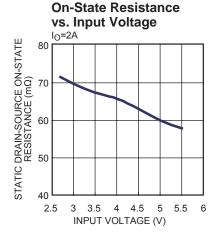
150
130
130
10
2.5 3 3.5 4 4.5 5 5.5 6
INPUT VOLTAGE (V)

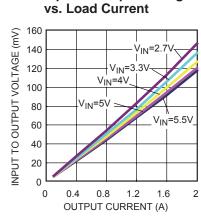
Static Drain-Source



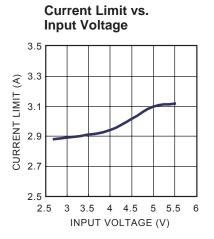
Supply Current, Output







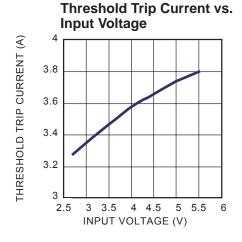
Input to Output Voltage

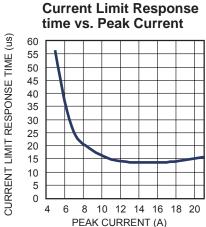


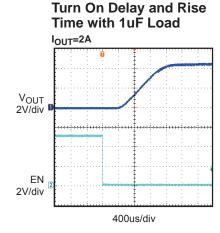


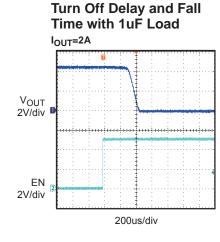
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

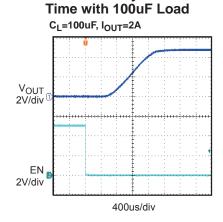
 V_{IN} =5V, V_{EN} =0V for MP62260-1, V_{CC} =5V, C_{L} =2.2uF, T_{A} =25 $^{\circ}$ C unless otherwise noted.



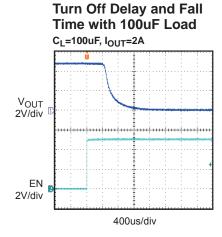


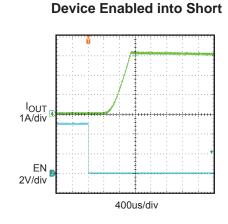




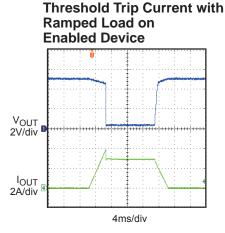


Turn On Delay and Rise





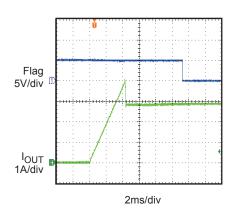
Short Circuit Current,



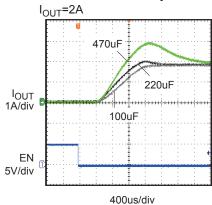


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

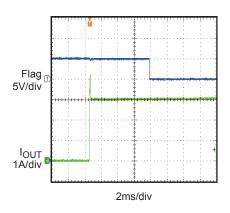




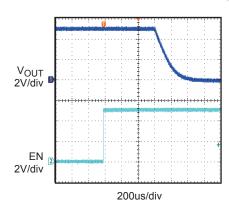
Inrush Current with Different Load Capacitance



1Ω Load Connected to Enabled Device

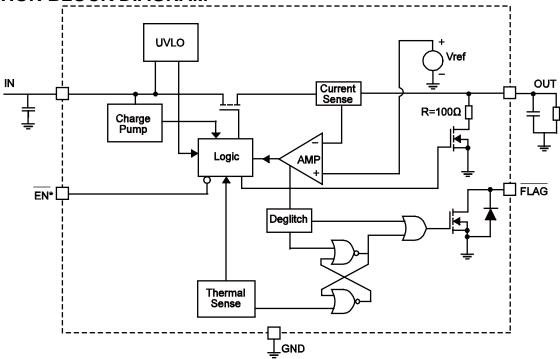


Turn Off Delay and Fall Time with Output Discharge





FUNCTION BLOCK DIAGRAM



*: EN is active high for MP62261-1

Figure2—Functional Block Diagram



DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62260-1/MP62261-1 switches into to a constant-current mode (current limit value). MP62260-1/MP62261-1 will be shutdown only if the over current condition stays long enough to trigger thermal protection.

Trigger over current protection for different overload conditions occurring in applications:

- The output has been shorted or overloaded before the device is enabled or input applied. MP62260-1/MP62261-1 detects the short or overload and immediately switches into a constant-current mode.
- 2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constantcurrent mode. However, high current may flow for a short period of time before the current-limit circuit can react.
- 3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62260-1/MP62261-1 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during over temperature or voltage lockout.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis, and would recover once cooling down to approx 120°C.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62260-1/MP62261-1 is operating correctly.

This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the switch to reduce overall supply current. Once the EN pin reaches EN threshold, the MP62260-1/MP62261-1 is enabled.

Output Discharge

The part involves a discharge function that provides a resistive discharge path for the external output capacitor. The function will be active when the part is disabled (Input voltage is under UVLO or enable is deasserted) and it will be done in a very limited time.



APPLICATION INFORMATION

Power-Supply Considerations

Over $10\mu F$ capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

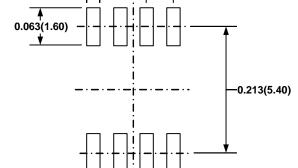
In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

0.024(0.61)



PACKAGE INFORMATION

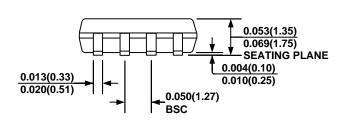
0.189(4.80) 0.197(5.00) 8 5 0.150(3.80) 0.228(5.80) 0.157(4.00) 0.244(6.20)



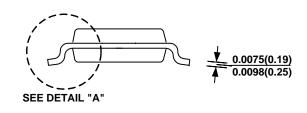
-0.050(1.27)

TOP VIEW

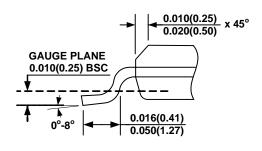
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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