

TRIPLE 8/10-BIT, 150/110 MSPS, VIDEO AND GRAPHICS DIGITIZER WITH ANALOG PLL

FEATURES

- Analog Channels
 - -6 dB to 6 dB Analog Gain
 - Analog Input MUXs
 - Auto Video Clamp
 - Three Digitizing Channels, Each With Independently Controllable Clamp, PGA, and ADC
 - Clamping: Selectable Clamping Between Bottom Level and Mid-level
 - Offset: 1024-Step Programmable RGB or YPbPr Offset Control
 - PGA: 8-Bit Programmable Gain Amplifier
 - ADC: 8/10-Bit 150/110 MSPS A/D Converter
 - Automatic Level Control Circuit
 - Composite Sync: Integrated Sync-on-Green Extraction From GreenLuminance Channel
 - Support for DC and AC-Coupled Input Signals
- PLL
 - Fully Integrated Analog PLL for Pixel Clock Generation
 - 12-150 MHz Pixel Clock Generation From HSYNC Input
 - Adjustable PLL Loop Bandwidth for Minimum Jitter
 - 5-Bit Programmable Subpixel Accurate Positioning of Sampling Phase
- Output Formatter
 - Support for RGB/YCbCr 4:4:4 and YCbCr 4:2:2 Output Modes to Reduce Board Traces
 - Dedicated DATACLK Output for Easy Latching of Output Data
- System
 - Industry-Standard Normal/Fast I²C Interface With Register Readback Capability
 - Space-Saving TQFP-100 Pin Package
 - Thermally-Enhanced PowerPAD™ Package for Better Heat Dissipation

APPLICATIONS

- LCD TV/Monitors/Projectors
- DLP TV/Projectors
- PDP TV/Monitors
- PCTV Set-Top Boxes
- Digital Image Processing
- Video Capture/Video Editing
- Scan Rate/Image Resolution Converters
- Video Conferencing
- Video/Graphics Digitizing Equipment

DESCRIPTION

TVP7000 is a complete solution for digitizing video and graphic signals in RGB or YPbPr color spaces. The device supports pixel rates up to 150 MHz. Therefore, it can be used for PC graphics digitizing up to the VESA standard of SXGA (1280 × 1024) resolution at 75 Hz screen refresh rate, and in video environments for the digitizing of digital TV formats, including HDTV up to 1080p. TVP7000 can be used to digitize CVBS and S-Video signal with 10-bit ADCs.

The TVP7000 is powered from 3.3-V and 1.8-V supply and integrates a triple high-performance A/D converter with clamping functions and variable gain, independently programmable for each channel. The clamping timing window is provided by an external pulse or can be generated internally. The TVP7000 includes analog slicing circuitry on the Y or G input to support sync-on-luminance or sync-on-green extraction. In addition, TVP7000 can extract discrete HSYNC and VSYNC from composite sync using a sync slicer.

TVP7000 also contains a complete analog PLL block to generate a pixel clock from the HSYNC input. Pixel clock output frequencies range from 12 MHz to 150 MHz.

All programming of the part is done via an industry-standard I²C interface, which supports both reading and writing of register settings. The TVP7000 is available in a space-saving TQFP 100-pin PowerPAD package.



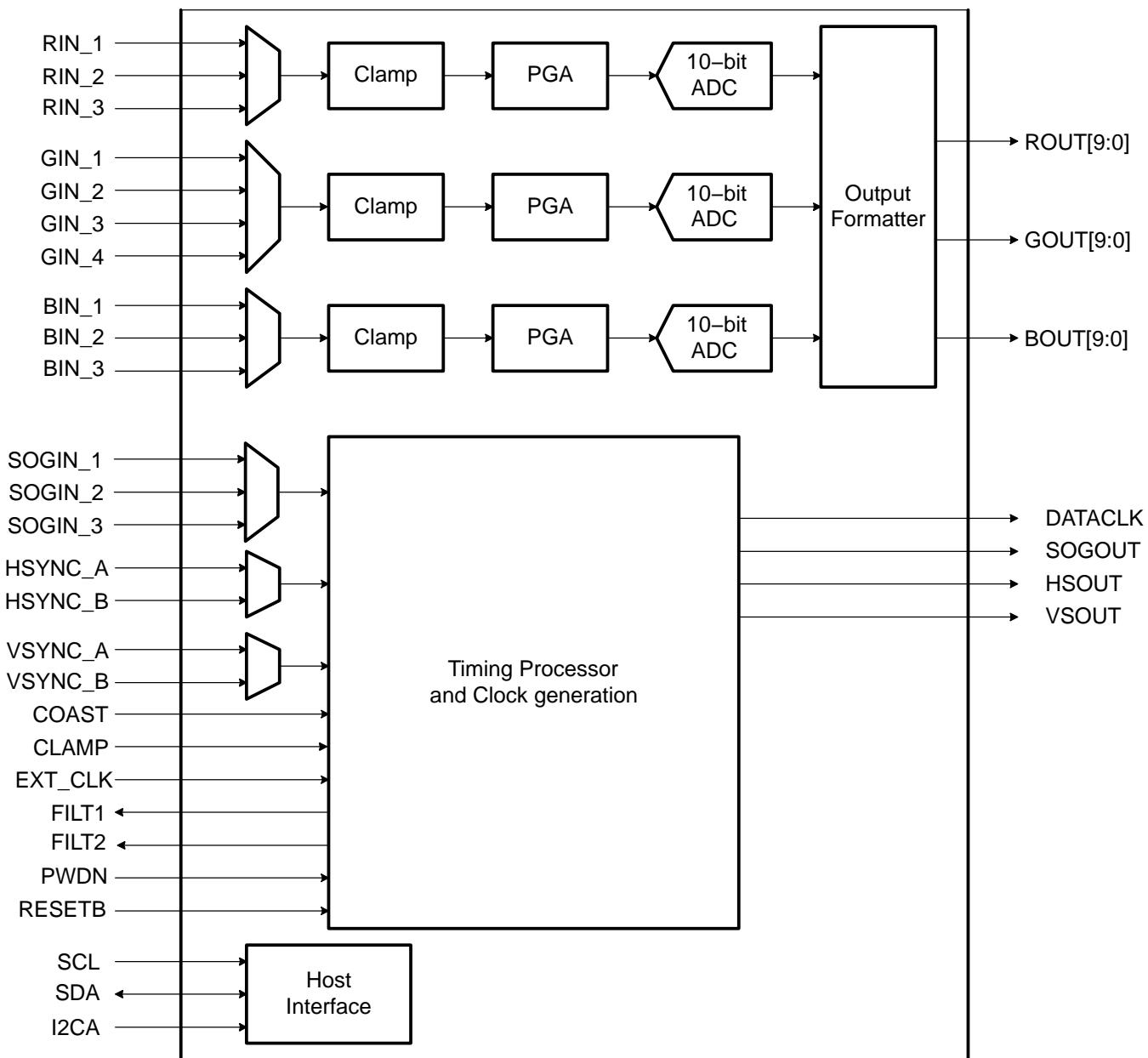
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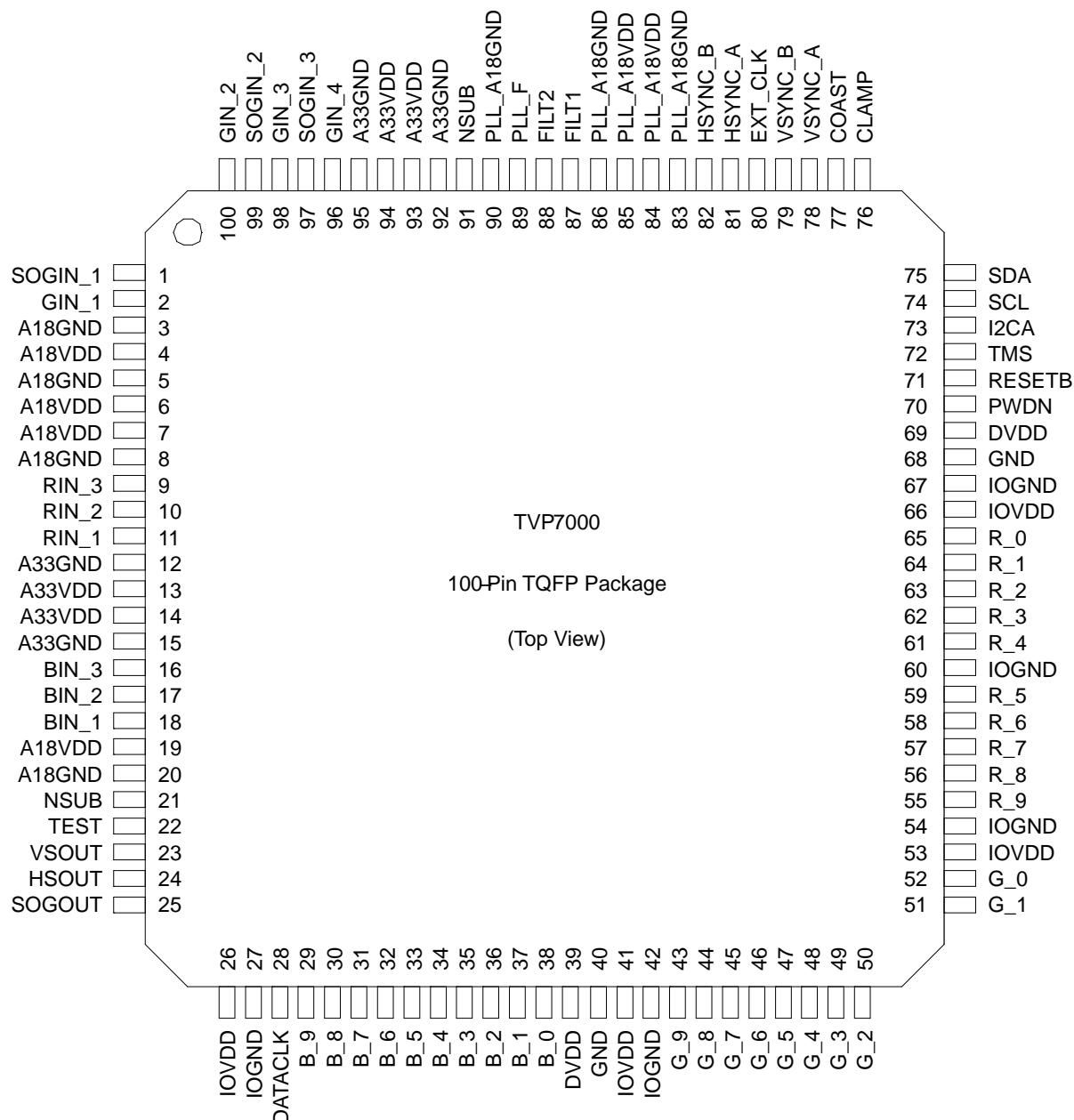
ORDERING INFORMATION

| T_A | PACKAGED DEVICES |
|-------------|------------------------------------|
| | 100-PIN PLASTIC FLATPACK PowerPAD™ |
| 0°C to 70°C | TVP7000PZP |

FUNCTIONAL BLOCK DIAGRAM



TERMINAL ASSIGNMENTS



TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|------------------------------|--------------------|-----|--|
| NAME | NO. | | |
| ANALOG VIDEO | | | |
| RIN_1 | 11 | I | Analog video input for R/Pr 1 |
| RIN_2 | 10 | I | Analog video input for R/Pr 2 |
| RIN_3 | 9 | I | Analog video input for R/Pr 3 |
| GIN_1 | 2 | I | Analog video input for G/Y 1 |
| GIN_2 | 100 | I | Analog video input for G/Y 2 |
| GIN_3 | 98 | I | Analog video input for G/Y 3 |
| GIN_4 | 96 | I | Analog video input for G/Y 4 |
| BIN_1 | 18 | I | Analog video input for B/Pb 1 |
| BIN_2 | 17 | I | Analog video input for B/Pb 2 |
| BIN_3 | 16 | I | Analog video input for B/Pb 3 The inputs must be AC coupled. The recommended coupling capacitor is 0.1 μ F. Unused analog inputs should be connected to ground using a 10 nF capacitor. |
| CLOCK SIGNALS | | | |
| DATACLK | 28 | O | Data clock output |
| EXT_CLK | 80 | I | External clock input for free running mode |
| TEST | 22 | O | Internal 5 MHz clock output, coast output, high-Z, or SOG output |
| DIGITAL VIDEO | | | |
| ROUT [9:0] | 55–59, 61–65 | O | Digital video output of R/Cr, ROUT [9] is MSB. |
| GOUT [9:0] | 43–52 | O | Digital video output of G/Y, GOUT [9] is MSB. |
| BOUT [9:0] | 29–38 | O | Digital video output of B/Cb, BOUT [9] is MSB. For a 4:2:2 mode BOUT outputs CbCr data. Unused outputs can be left unconnected. |
| MISCELLANEOUS SIGNALS | | | |
| PWDN | 70 | I | Power down input. 1: Power down 0: Normal mode |
| RESETB | 71 | I | Reset input, active low |
| TMS | 72 | I | Test Mode Select input. Used to enable JTAG test mode. Active high. Normal mode, this terminal should be connected to a ground. |
| FILT1 | 87 | O | External filter connection for PLL. The recommended capacitor is 0.1 μ F. see Figure 4 |
| FILT2 | 88 | O | External filter connection for PLL. The recommended capacitor is 4.7 nF. See Figure 4 |
| HOST INTERFACE | | | |
| I ² C A | 73 | I | I ² C Address input |
| SCL | 74 | I | I ² C Clock input |
| SDA | 75 | I/O | I ² C Data bus |
| POWER SUPPLIES | | | |
| NSUB | 21, 91 | I | Substrate ground. Connect to analog ground. |
| A33VDD | 13, 14, 93, 94 | I | Analog power. Connect to 3.3 V. |
| A33GND | 12, 15, 92, 95 | I | Analog 3.3 V return. Connect to Ground. |
| A18GND | 3, 5, 8, 20 | I | Analog 1.8V return. Connect to Ground |
| A18VDD | 4, 6, 7, 19 | I | Analog power. Connect to 1.8 V. |
| PLL_A18VDD | 84, 85 | I | PLL analog power. Connect to 1.8 V. |
| PLL_F | 89 | I | PLL filter internal supply connection |
| PLL_A18GND | 83, 86, 90 | I | PLL analog power return. Connect to Ground. |
| GND | 40, 68 | I | Digital return. Connect to Ground. |
| DVDD | 39, 69 | I | Digital power. Connect to 1.8 V |
| IOGND | 27, 42, 54, 60, 67 | I | Digital power return. Connect to Ground. |
| IOVDD | 26, 41, 53, 66 | I | Digital power. Connect to 3.3 V or less for reduced noise. |
| SYNC SIGNALS | | | |
| CLAMP | 76 | I | External Clamp input. Unused inputs can be connected to ground. |
| COAST | 77 | I | External PLL COAST signal input. Unused inputs can be connected to ground |

TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O | DESCRIPTION |
|----------|-----|-----|---|
| NAME | NO. | | |
| VSYNC_A | 78 | I | Vertical sync input A |
| VSYNC_B | 79 | I | Vertical sync input B. Unused inputs can be connected to ground. |
| HSYNC_A | 81 | I | Horizontal Sync input A |
| HSYNC_B | 82 | I | Horizontal Sync input B. Unused inputs can be connected to ground. |
| SOGIN1 | 1 | I | Sync-on-green input 1 |
| SOGIN2 | 99 | I | Sync-on-green input 2 |
| SOGIN3 | 97 | i | Sync-on-green input 3. Unused inputs should be connected to ground using a 10 nF capacitor. |
| VSOUT | 23 | O | Vertical sync output |
| HSOUT | 24 | O | Horizontal sync output |
| SOGOUT | 25 | O | Sync-on-green slicer output |

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | UNIT |
|------------------------------|---|-----------------|
| Supply voltage range | IOVDD to IOGND | −0.5 V to 4.5 V |
| | DVDD to GND | −0.5 V to 2.3 V |
| | PLL_A18VDD to PLL_A18GND and A18VDD to A18GND | −0.5 V to 2.3 V |
| | A33VDD to A33GND | −0.5 V to 4.5 V |
| Digital input voltage range | VI to GND | −0.5 V to 4.5 V |
| Analog input voltage range | AI to A33GND | −0.2 V to 2.3 V |
| Digital output voltage range | VO to GND | −0.5 V to 4.5 V |
| TA | Operating free-air temperature | 0°C to 70°C |
| Tstg | Storage temperature | −65°C to 150°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

 over operating free-air temperature range, $T_A = 0^\circ\text{C}$ to 70°C (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------|--|-----------|-----------|-----|------|
| IOVDD | Digital I/O supply voltage | 3.0 | 3.3 | 3.6 | V |
| DVDD | Digital supply voltage | 1.70 | 1.8 | 1.9 | V |
| PLL_A18VDD | Analog PLL supply voltage | 1.70 | 1.8 | 1.9 | V |
| A18VDD | Analog supply voltage | 1.70 | 1.8 | 1.9 | V |
| A33VDD | Analog supply voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{I(P-P)}$ | Analog input voltage (ac-coupling necessary) | 0.5 | | 2.0 | V |
| V_{IH} | Digital input voltage high | 0.7 IOVDD | | | V |
| V_{IL} | Digital input voltage low | | 0.3 IOVDD | | V |
| I_{OH} | High-level output current | | | 2 | mA |
| I_{OL} | Low-level output current | | | −2 | mA |
| $I_{OH_DATACLK}$ | DATACLK high-level output current | | | 4 | mA |
| $I_{OL_DATACLK}$ | DATACLK low-level output current | | | −4 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

ELECTRICAL CHARACTERISTICS

IOVDD = 3.3 V, DVDD = 1.8 V, PLL_A18VDD = 1.8 V, A18VDD = 1.8 V, A33VDD = 3.3 V, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX ⁽²⁾ | UNIT |
|---------------------|--|-----------|--------------------|--------------------|---------|
| POWER SUPPLY | | | | | |
| I_{IOVDDD} | 3.3-V supply current | 78.75 MHz | | 80 | 130 mA |
| I_{DVDD} | 1.8-V supply current | 78.75 MHz | | 253 | 260 mA |
| P_{TOT} | Total power dissipation, normal mode | 78.75 MHz | | 719 | 897 mW |
| I_{IOVDDD} | 3.3-V supply current | 108 MHz | | 101 | 160 mA |
| I_{DVDD} | 1.8-V supply current | 108 MHz | | 261 | 275 mA |
| P_{TOT} | Total power dissipation, normal mode | 108 MHz | | 803 | 1023 mW |
| I_{IOVDDD} | 3.3-V supply current | 148.5 MHz | | 128 | 240 mA |
| I_{DVDD} | 1.8-V supply current | 148.5 MHz | | 250 | 280 mA |
| P_{TOT} | Total power dissipation, normal mode | 148.5 MHz | | 872 | 1296 mW |
| P_{DOWN} | Total power dissipation, power-down mode | | | 1 | mW |

(1) SMPTE color bar RGB input pattern used.

(2) Worst case vertical line RGB input pattern used.

ELECTRICAL CHARACTERISTICS

IOVDD = 3.3 V, DVDD = 1.8 V \pm 0.1, PLL_A18VDD = 1.8 V \pm 0.1, A18VDD = 1.8 V \pm 0.1, A33VDD = 3.3 V, T_A = 0°C to 70°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----------|-----------|-----|-----------------|
| ANALOG INTERFACE | | | | | |
| Input voltage range | By design | 0.5 | 1.0 | 2.0 | V _{pp} |
| Z _i Input impedance, analog video inputs | By design | 500 | | | k Ω |
| DIGITAL LOGIC INTERFACE | | | | | |
| C _i Input capacitance | By design | 10 | | | pF |
| Z _i Input impedance | By design | 500 | | | k Ω |
| V _{OH} Output voltage high | I _{OH} = 2 mA | 0.8 IOVDD | | | V |
| V _{OL} Output voltage low | I _{OL} = -2 mA | 0.2 IOVDD | | | V |
| V _{OH_SCLK} DATACLK output voltage high | I _{OH} = 4 mA | 0.8 IOVDD | | | V |
| V _{OL_SCLK} DATACLK output voltage low | I _{OH} = -2 mA | 0.2 IOVDD | | | V |
| V _{IH} High-level input voltage | By design | 0.7 IOVDD | | | V |
| V _{IL} Low-level input voltage | By design | 0.3 IOVDD | | | V |
| A/D CONVERTERS | | | | | |
| Conversion rate | | 12 | 150 | | MSPS |
| DNL DC differential nonlinearity | 10 bit, 110 MHz | -1 | \pm 0.5 | +1 | LSB |
| | 8 bit, 150 MHz | -1 | \pm 0.5 | +1 | |
| INL DC integral nonlinearity | 10 bit, 110 MHz | -4 | \pm 1 | +4 | LSB |
| | 8 bit, 150 MHz | -4 | \pm 1 | +4 | |
| Missing code | 8 bit, 150 MHz | none | | | |
| SNR Signal-to-noise ratio | 10 MHz, 1.0 V _{P-P} at 110 MSPS | 52 | | | dB |
| Analog bandwidth | By design | 500 | | | MHz |
| PLL | | | | | |
| Clock jitter | | 500 | | | ps |
| Phase adjustment | | 11.6 | | | degree |
| VCO frequency range | | 12 | 150 | | MHz |

TIMING REQUIREMENTS

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|--|--------------------------------|-----|-----|-----|------|
| CLOCKS, VIDEO DATA, SYNC TIMING | | | | | |
| Duty cycle DATACLK | | | 50% | | |
| t_1 DATACLK rise time | 10% to 90% | | 1 | | ns |
| t_2 DATACLK fall time | 90% to 10% | | 1 | | ns |
| t_3 Output delay time | | 1.5 | | 3.5 | ns |

(1) Measured with a load of 15 pF.

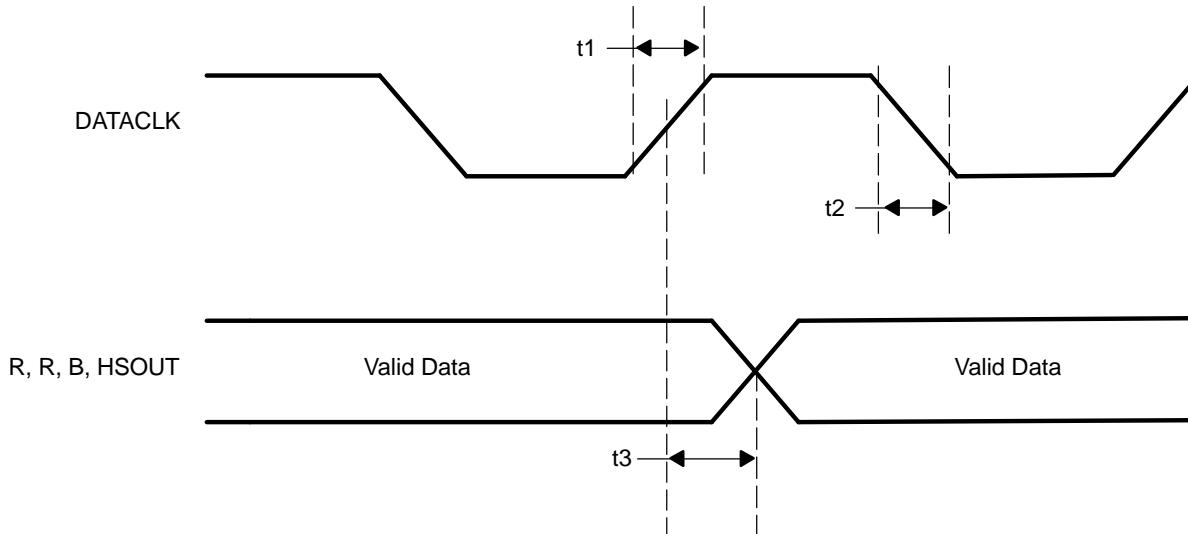


Figure 1. Clock, Video Data, and Sync Timing

TIMING REQUIREMENTS

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------|-----|-----|-----|------|
| I²C HOST PORT TIMING | | | | | |
| t ₁ Bus free time between STOP and START | Specified by design | 1.3 | | | μs |
| t ₂ Setup time for a (repeated) START condition | Specified by design | 0.6 | | | μs |
| t ₃ Hold time (repeated) START condition | Specified by design | 0.6 | | | μs |
| t ₄ Setup time for a STOP condition | Specified by design | 0.6 | | | ns |
| t ₅ Data setup time | Specified by design | 100 | | | ns |
| t ₆ Data hold time | Specified by design | 0 | 0.9 | | μs |
| t ₇ Rise time SDA and SCL signal | Specified by design | | 250 | | ns |
| t ₈ Fall time SDA and SCL signal | Specified by design | | 250 | | ns |
| C _b Capacitive load for each bus line | Specified by design | | 400 | | pF |
| f _{I²C} I ² C clock frequency | Specified by design | | 400 | | kHz |

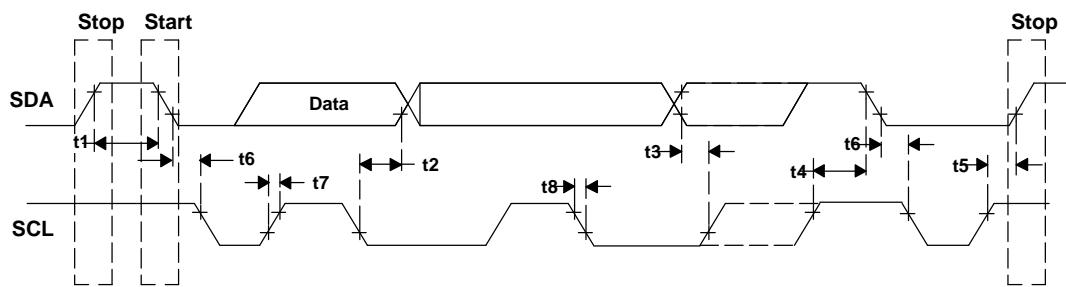


Figure 2. I²C Host Port Timing

FUNCTIONAL DESCRIPTION

Analog Channel

The TVP7000 contains three identical analog channels that are independently programmable. Each channel consists of a clamping circuit, a programmable gain amplifier, automatic offset control and an A/D converter.

Analog Input Switch Control

TVP7000 has 3 analog channels that accept up to 10 video inputs. The user can configure the internal analog video switches via the I²C interface. The 10 analog video inputs can be used for different input configurations some of which are:

- Up to 10 selectable individual composite video inputs
- Up to 2 selectable RGB graphics inputs
- Up to 3 selectable YPbPr video HD/SD inputs

The input selection is performed by the input select register at I²C subaddress 0x19 and 0x1A (see Input Mux Select 1 and Input Mux Select 2)

Analog Input Clamping

An internal clamping circuit restores the AC-coupled video/graphic signal to a fixed DC level. The clamping circuit provides line-by-line restoration of the signal black level to a fixed DC reference voltage. The selection between bottom and mid level clamping is performed by I²C subaddress 0x10 (see Sync On_Green Threshold)

The internal clamping time can be adjusted by I²C clamp start and width registers at subaddress 0x05 and 0x06 (see Clamp Start and Clamp Width)

Programmable Gain Amplifier (PGA)

The TVP7000 PGA can scale a signal with a voltage-input compliance of 0.5-V_{pp} to 2-V_{pp} to a full-scale 10-bit A/D output code range. A 4-bit code sets the coarse gain (Red Coarse Gain, Green Coarse Gain, Blue Coarse Gain) with individual adjustment per channel. Minimum gain corresponds to a code 0x0 (2-V_{pp} full-scale input, -6 dB gain) while maximum gain corresponds to code 0xF (0.5-V_{pp} full-scale, +6 dB gain). TVP7000 also has 8-bit fine gain control (Red Fine Gain, Green Fine Gain, Blue Fine Gain) for RGB independently ranging from 1 to 2. For a normal PC graphics input, the fine gain will be used mostly.

Programmable Offset Control and Automatic Level Control (ALC)

The TVP7000 supports a programmable offset control for RGB independently. A 6-bit code sets the coarse offset (Red Coarse Offset, Green Coarse Offset, Blue Coarse Offset) with individual adjustment per channel. The coarse offset ranges from -32 LSB to +31 LSB. The coarse offset registers apply before the ADC. A 10-bit fine offset registers (Red Fine Offset, Green Fine Offset, Blue Fine Offset) apply after the ADC. The fine offset ranges from -512 LSB to +511 LSB.

ALC circuit maintains the level of the signal to be set at a value which is programmed at fine offset I²C register. It consists of pixel averaging filter and feedback loop. This ALC function can be enabled or disabled by I²C register address at 0x26. ALC circuit needs a timing pulse generated internally but user should program the position properly. The ALC pulse must be positioned after the clamp pulse. The position of ALC pulse is controlled by ALC placement I²C register at address 0x31. This is available only for internal ALC pulse timing. For external clamp, the timing control of clamp is not applicable so the ALC pulse control is also not applicable. Therefore it is suggested to keep the external clamp pulse as long as possible. ALC is applied as same position of external clamp pulse.

A/D Converters

All ADCs have a resolution of 10-bits and can operate up to 150 MSPS. All A/D channels receive an identical clock from the on-chip phase-locked loop (PLL) at a frequency between 12 MHz and 150 MHz. All ADC reference voltages are generated internally. Also the external sampling clock can be used.

Analog PLL

The analog PLL generates a high-frequency internal clock used by the ADC sampling and data clocking out to derive the pixel output frequency with programmable phase. The reference signal for this PLL is the horizontal sync signal supplied on the HSYNC input or from extracted horizontal sync of sync slicer block for embedded sync signals. The analog PLL consisted of phase detector, loop filter, voltage controlled oscillator (VCO), divider and phase select. The analog block diagram is shown at [Figure 3](#).

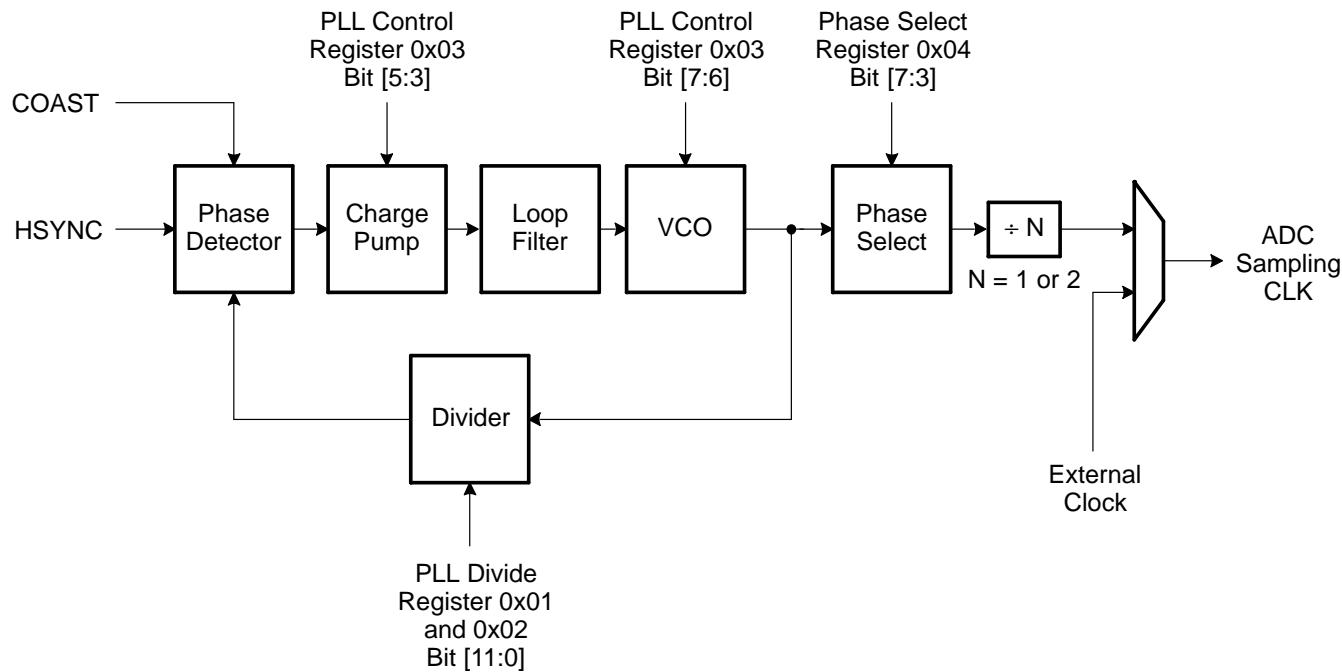


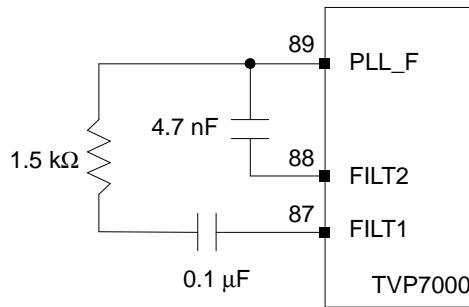
Figure 3. PLL Block Diagram

The COAST signal is used to allow the PLL to keep running at the same frequency, in the absence of the incoming HSYNC signal or disordered HSYNC period. This is useful during the vertical sync period, or any other time that the HSYNC is not available.

There are several PLL controls to produce the correct sampling clock. The 12-bit divider register is programmable to select exact multiplication number to generate the pixel clock in the range of 12 MHz to 150 MHz. The 3-bit loop filter current control register is to control the charge pump current that drives the low-pass loop filter. The applicable current values are listed in the [Table 1](#).

The 2-bit VCO range control is to improve the noise performance of the TVP7000. The frequency ranges for the VCO are shown in [Table 1](#). The phase of the PLL generated clock can be programmed in 32 uniform steps over a single clock period ($360/32=11.25$ degrees phase resolution) so that the sampling phase of the ADC can be accurately controlled.

In addition to sourcing the ADC channel clock from the PLL, an external pixel clock can be used (from pin 80). The PLL characteristics are determined by the loop filter design, by the PLL charge pump current, and by the VCO range setting. The loop filter design is shown in [Figure 4](#). Supported settings of VCO range and charge pump current for VESA standard display modes are listed in [Table 1](#).

**Figure 4. PLL Loop Filter****Table 1. Recommended VCO Range and Charge Pump Current Settings for Supporting Standard Display Formats**

| STANDARD | RESOL- UTION | REFRESH RATE | HORIZON- TAL FRE- QUENCY (kHz) | PIXEL RATE (MHz) | PLL Divider Total pix/line | PLL DIV MSB Reg 01h | PLL DIV LSB Reg 02h [11:4] | Reg 03h | Output Div- ider Reg 04h [0] | VCO RANGE Reg 03h [7:6] | CP CUR- RENT Reg 03h [5:3] |
|----------|-----------------|-----------------|---|---------------------|----------------------------------|---------------------------|----------------------------------|---------|------------------------------------|-------------------------------|----------------------------------|
| VGA | 640 × 480 | 60 Hz | 31.5 | 25.175 | 1600(2x) | 64h | 00h | 68h | 1 | Low (01b) | 101b |
| | | 72 Hz | 37.9 | 31.5 | 1664(2x) | 68h | 00h | 58h | 1 | Low (01b) | 011b |
| | | 75 Hz | 37.5 | 31.5 | 1680(2x) | 69h | 00h | 58h | 1 | Low (01b) | 011b |
| | | 85 Hz | 43.3 | 36 | 832 | 34h | 00h | 68h | 0 | Low (01b) | 101b |
| SVGA | 800 × 600 | 56 Hz | 35.1 | 36 | 1024 | 40h | 00h | 68h | 0 | Low (01b) | 101b |
| | | 60 Hz | 37.9 | 40 | 1056 | 42h | 00h | 68h | 0 | Low (01b) | 101b |
| | | 72 Hz | 48.1 | 50 | 1040 | 41h | 00h | 68h | 0 | Low (01b) | 101b |
| | | 75 Hz | 46.9 | 49.5 | 1056 | 42h | 00h | 68h | 0 | Low (01b) | 101b |
| | | 85 Hz | 53.7 | 56.25 | 1048 | 41h | 80h | 68h | 0 | Low (01b) | 101b |
| XGA | 1024 × 768 | 60 Hz | 48.4 | 65 | 1344 | 54h | 00h | 58h | 0 | Low (01b) | 011b |
| | | 70 Hz | 56.5 | 75 | 1328 | 53h | 00h | A8h | 0 | Med (10b) | 101b |
| | | 75 Hz | 60 | 78.75 | 1312 | 52h | 00h | A8h | 0 | Med (10b) | 101b |
| | | 85 Hz | 68.7 | 94.5 | 1376 | 56h | 00h | A8h | 0 | Med (10b) | 101b |
| SXGA | 1280 × 1024 | 60 Hz | 64 | 108 | 1688 | 69h | 80h | A8h | 0 | Med (10b) | 101b |
| | | 75 Hz | 80 | 135 | 1688 | 69h | 80h | 98h | 0 | Med (10b) | 011b |
| Video | 720 × 480p | 60 Hz | 31.468 | 27 | 1716(2x) | 6Bh | 40h | 68h | 1 | Low (01b) | 101b |
| | 720 × 576p | 50 Hz | 31.25 | 27 | 1728(2x) | 6Ch | 00h | 68h | 1 | Low (01b) | 101b |
| | 1280 × 720p | 60 Hz | 45 | 74.25 | 1650 | 67h | 20h | A8h | 0 | Med (10b) | 101b |
| | 1280 × 720p | 50 Hz | 37.5 | 74.25 | 1980 | 7Bh | C0h | A8h | 0 | Med (10b) | 101b |
| | 1920 × 1080i | 60 Hz | 33.75 | 74.25 | 2200 | 89h | 80h | A8h | 0 | Med (10b) | 101b |
| | 1920 × 1080i | 50 Hz | 28.125 | 74.25 | 2640 | A5h | 00h | A8h | 0 | Med (10b) | 101b |
| | 1920 × 1080p | 60 Hz | 67.5 | 148.5 | 2200 | 89h | 80h | D8h | 0 | High (11b) | 011b |
| | 1920 × 1080p | 50 Hz | 56.25 | 148.5 | 2640 | A5h | 00h | D8h | 0 | High (11b) | 011b |

Sync Slicer

TVP7000 includes a circuit that compares the input signal on Green channel to a level 150mV (typical value) above the clamped level (sync tip). The slicing level is programmable by I²C register subaddress at 0x10. The digital output of the composite sync slicer is available on the SOGOUT pin.

Sync Separator

The sync separator automatically extracts VSYNC and HSYNC from the sliced composite sync input supplied at the SOG input. The G or Y input containing the composite sync must be AC coupled to the SOG input pin using a 10-nF capacitor. Support for PC graphics, SDTV, and HDTV up to 1080p is provided.

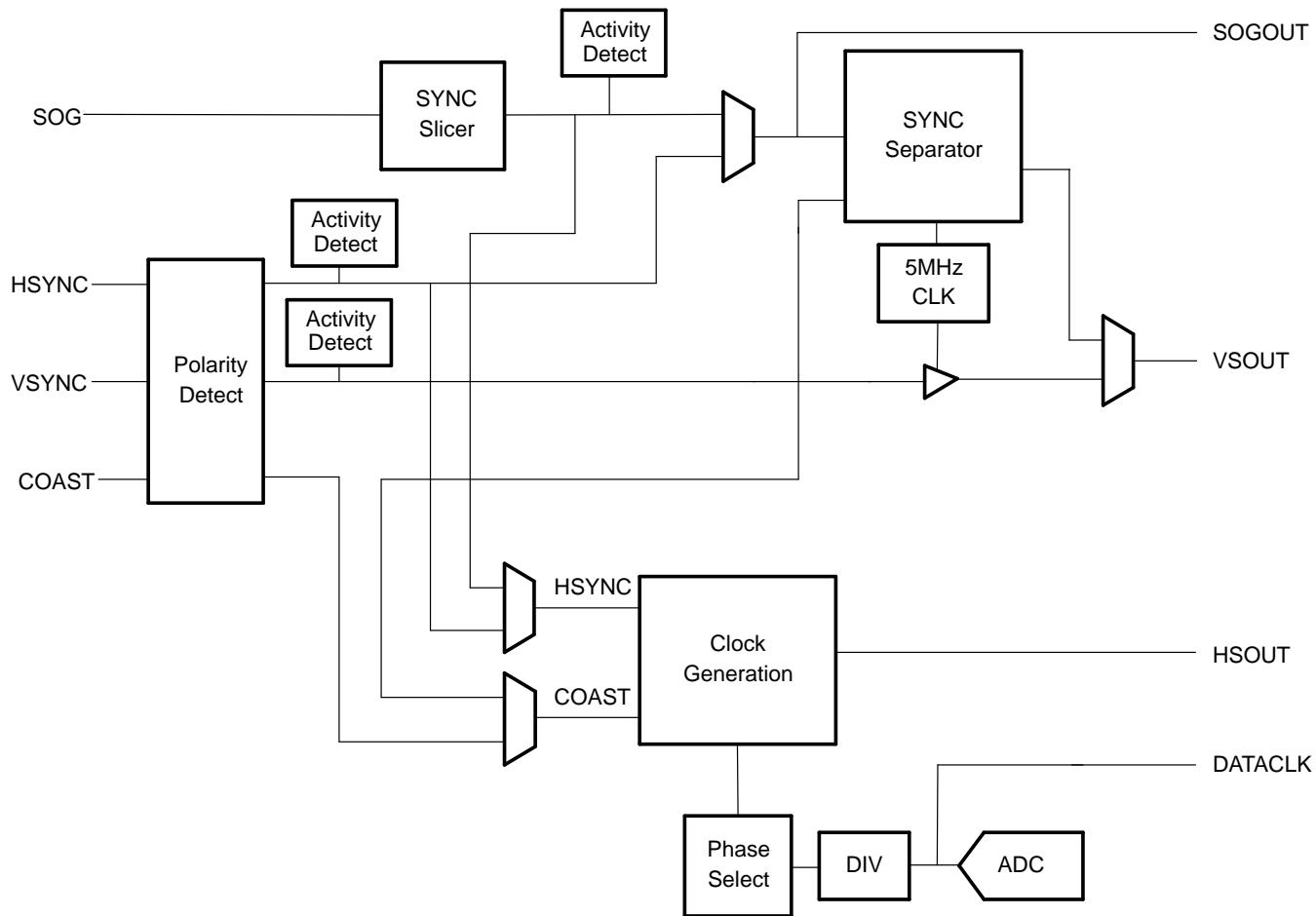
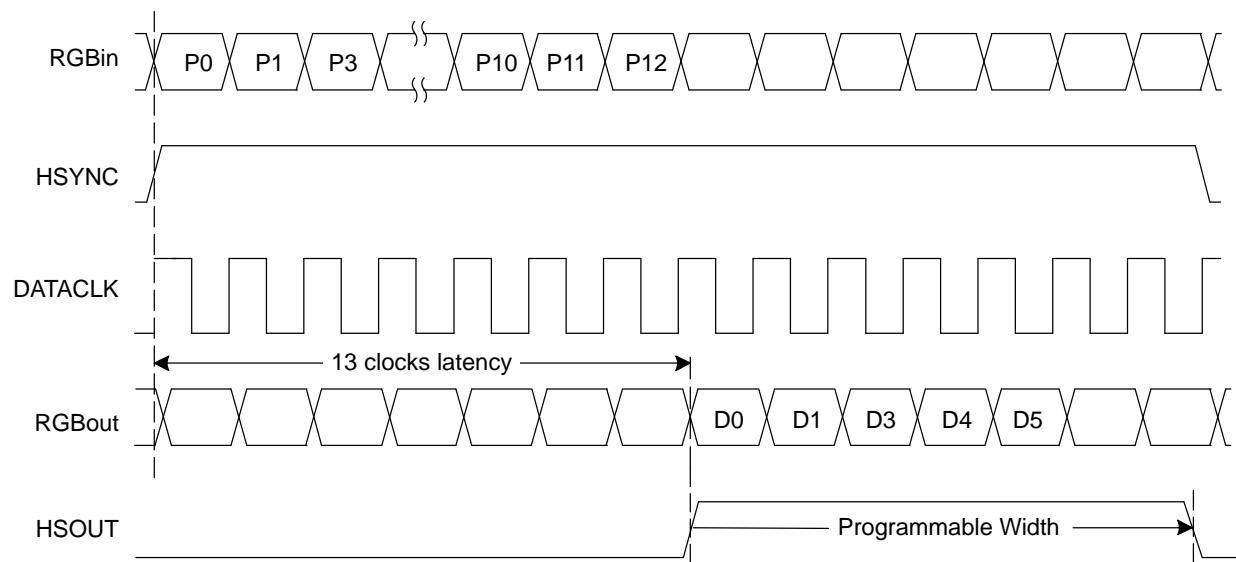


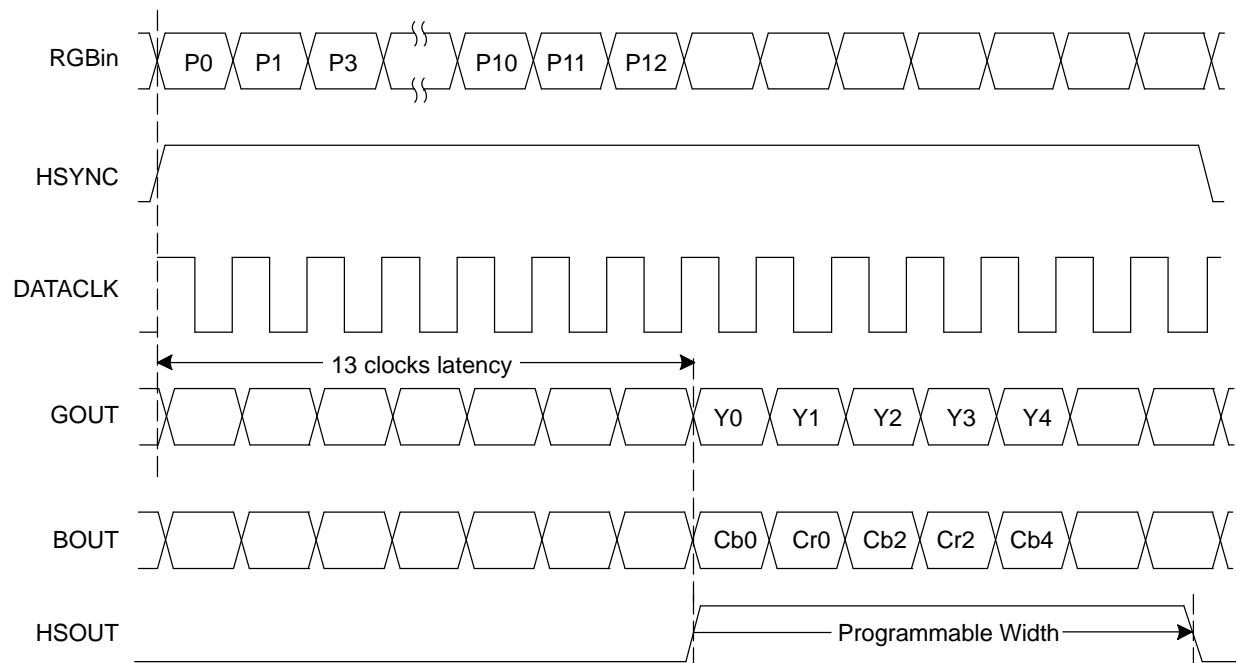
Figure 5. Sync Processing

Timing

The TVP7000 supports RGB/YCbCr 4:4:4 and YCbCr 4:2:2 modes. Output timing is shown in [Figure 6](#). All timing diagrams are shown for operation with internal PLL clock at phase 0. For a 4:2:2 mode, CbCr data outputs at BOUT[9:0] pins.



4:4:4: RGB/YCbCr Output Timing



4:2:2 YCbCr Output Timing

Figure 6. Output Timing Diagram

I²C Host Interface

Communication with the TVP7000 device is via an I²C host interface. The I²C standard consists of two signals, serial input/output data (SDA) line and input clock line (SCL), which carry information between the devices connected to the bus. A third signal (I²CA) is used for slave address selection. Although an I²C system can be multi-mastered, the TVP7000 can function as a slave device only.

Since SDA and SCL are kept open-drain at logic high output level or when the bus is not driven, the user should connect SDA and SCL to a positive supply voltage via a pull up resistor on the board. SDA is implemented bi-directional. The slave addresses select, terminal 73 (I²CA), enables the use of two TVP7000 devices tied to the same I²C bus since it controls the least significant bit of the I²C device address

Table 2. I²C Host Interface Terminal Description

| SIGNAL | TYPE | DESCRIPTION |
|--------------------|------|-------------------------|
| I ² C A | I | Slave address selection |
| SCL | I | Input clock line |
| SDA | I/O | Input/output data line |

Reset and I²C Bus Address Selection

TVP7000 can respond to two possible chip addresses. The address selection is made at reset by an externally supplied level on the I²C A pin. The TVP7000 device samples the level of terminal 73 at power-up or at the trailing edge of RESETB and configures the I²C bus address bit A0. The I²C A terminal has an internal pull-down resistor to pull the terminal low to set a zero.

Table 3. I²C Host Interface Device Addresses

| A6 | A5 | A4 | A3 | A2 | A1 | A0 (I ² C A) | R/W | HEX |
|----|----|----|----|----|----|-------------------------|-----|-------|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 (default) | 1/0 | B9/B8 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 ⁽¹⁾ | 1/0 | BB/BA |

(1) If terminal 73 strapped to DVDD via a 2.2 kΩ resistor, I²C device address A0 is set to 1.

I²C Operation

Data transfers occur utilizing the following illustrated formats.

| | | | | | | | |
|---|----------|-----|------------|-----|-----------|-----|---|
| S | 10111000 | ACK | subaddress | ACK | send data | ACK | P |
|---|----------|-----|------------|-----|-----------|-----|---|

Read from I²C control registers

| | | | | | | | | | | |
|---|----------|-----|------------|-----|---|----------|-----|--------------|-----|---|
| S | 10111000 | ACK | subaddress | ACK | S | 10111001 | ACK | receive data | NAK | P |
|---|----------|-----|------------|-----|---|----------|-----|--------------|-----|---|

S = I²C Bus Start condition

P = I²C Bus Stop condition

ACK = Acknowledge generated by the slave

NAK = Acknowledge generated by the master, for multiple byte read master with ACK each byte except last byte

Subaddress = Subaddress byte

Data = Data byte, if more than one byte of DATA is transmitted (read and write), the subaddress pointer is automatically incremented

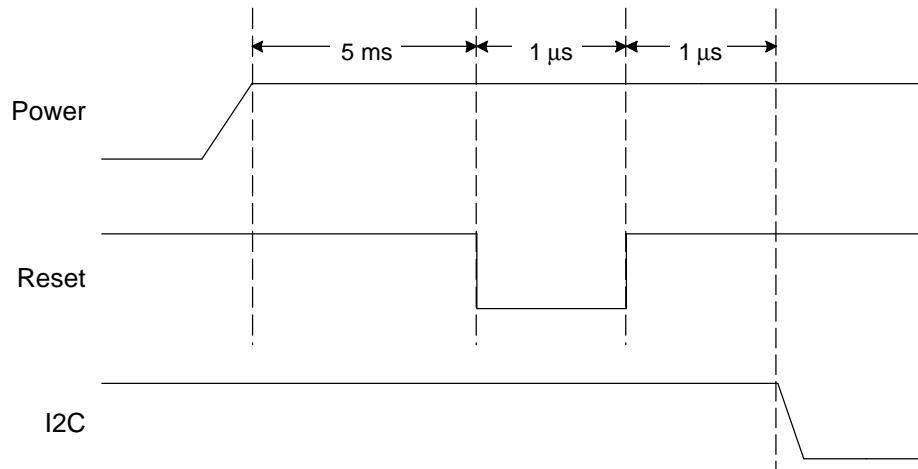
I²C bus address = Example shown that I²C A is in default mode. Write (B8h), Read (B9h)

Power-up, Reset, and Initialization

No specific power-up sequence is required, but all power supplies should be active and stable within 500 ms of each other. Reset may be low during power-up, but must remain low for at least 1 μs after the power supplies become stable. Alternately reset may be asserted any time with minimum 5 ms delay after power-up and must remain asserted for at least 1 μs. Reset timing is shown in [Figure 7](#). It is also recommended that any I²C operation starts 1 μs after reset ended. [Table 4](#) describes the status of the TVP7000 terminals during and immediately after reset.

Table 4. Reset Sequence

| SIGNAL NAME | DURING RESET | RESET COMPLETED |
|---------------------------------|----------------|-----------------|
| ROUT[9:0], BOUT[9:0], BOUT[9:0] | High impedance | Output |
| HSOUT, VSOUT, SOGOUT | High impedance | Output |
| DATACLK | High impedance | Output |

**Figure 7. Reset Timing**

Control Registers

The TVP7000 is initialized and controlled by a set of internal registers that define the operating parameters of the entire device. Communication between the external controller and the TVP7000 is through a standard I²C host port interface, as described earlier.

[Table 5](#) shows the summary of these registers. Detailed programming information for each register is described in the following sections.

Table 5. Control Registers Summary⁽¹⁾⁽²⁾

| Register Name | I ² C Subaddress | Default | R/W |
|-----------------------|-----------------------------|---------|-----|
| Chip Revision | 00h | | R |
| PLL Divide MSB | 01h | 69h | R/W |
| PLL Divide LSB | 02h | D0h | R/W |
| PLL Control | 03h | 48h | R/W |
| Phase Select | 04h | 80h | R/W |
| Clamp Start | 05h | 80h | R/W |
| Clamp Width | 06h | 80h | R/W |
| H SYNC Output Width | 07h | 20h | R/W |
| Blue Fine Gain | 08h | 80h | R/W |
| Green Fine Gain | 09h | 80h | R/W |
| Red Fine Gain | 0Ah | 80h | R/W |
| Blue Fine Offset | 0Bh | 80h | R/W |
| Green Fine Offset | 0Ch | 80h | R/W |
| Red Fine Offset | 0Dh | 80h | R/W |
| Sync Control 1 | 0Eh | 40h | R/W |
| PLL and Clamp Control | 0Fh | 4Eh | R/W |

(1) Register addresses not shown in the register map summary are reserved and must not be written to.

(2) Writing to or reading from any value labeled "Reserved" register may cause erroneous operation of the TVP7000. For registers with reserved bits, a 0b must be written to reserved bit locations unless otherwise stated.

Table 5. Control Registers Summary (continued)

| Register Name | I ² C Subaddress | Default | R/W |
|--------------------------------|-----------------------------|---------|-----|
| Sync On Green Threshold | 10h | B8h | R/W |
| Sync Separator Threshold | 11h | 20h | R/W |
| Pre-Coast | 12h | 00h | R/W |
| Post-Coast | 13h | 00h | R/W |
| Sync Detect Status | 14h | | R |
| Output Formatter | 15h | 00h | R/W |
| Test Register | 16h | 00h | R/W |
| Reserved | 17h–18h | | |
| Input Mux Select 1 | 19h | 00h | R/W |
| Input Mux Select 2 | 1Ah | 00h | R/W |
| Blue and Green Coarse Gain | 1Bh | 55h | R/W |
| Red Coarse Gain | 1Ch | 05h | R/W |
| Fine Offset LSB | 1Dh | 00h | R/W |
| Blue Coarse Offset | 1Eh | 20h | R/W |
| Green Coarse Offset | 1Fh | 20h | R/W |
| Red Coarse Offset | 20h | 20h | R/W |
| HSOUT Output Start | 21h | 09h | R/W |
| MISC Control | 22h | 00h | R/W |
| Reserved | 23h–25h | | |
| Automatic Level Control Enable | 26h | 00h | R/W |
| Reserved | 27h | | |
| Automatic Level Control Filter | 28h | 00h | R/W |
| Reserved | 29h | | |
| Fine Clamp Control | 2Ah | 00h | R/W |
| Power Control | 2Bh | | |
| ADC Setup | 2Ch | 00h | R/W |
| Coarse Clamp Control 1 | 2Dh | 00h | R/W |
| SOG Clamp | 2Eh | 00h | R/W |
| Reserved | 2Fh–30h | | |
| ALC Placement | 31h | 00h | R/W |

R = Read only

W = Write only

R/W = Read Write

Register Definitions

Chip Revision

Subaddress 00h

Read Only

| | | | | | | | |
|---------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Chip revision [7:0] | | | | | | | |

Chip revision [7:0]: Chip revision number

PLL Divide**Subaddress 01h-02h**

Default (69D0h)

| | | | | | | | |
|-----------------------|---|---|---|---|----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLL divide MSB [11:4] | | | | | | | |
| PLL divide LSB [3:0] | | | | | Reserved | | |

PLL divide [11:0]: PLL divide number sets the number of pixels per line. Controls the PLL feedback divider. MSB [11:4] bits should be loaded first whenever a change is required

PLL Control**Subaddress 03h**

Default (48h)

| | | | | | | | |
|----------|---|---------------------------|---|---|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VCO[1:0] | | Charge Pump Current [3:1] | | | Reserved | Reserved | Reserved |

VCO [1:0]: Selects VCO frequency range

00 = Ultra low

01 = Low (default)

10 = Medium

11 = High

Charge Pump Current [3:0]: Selects charge current of PLL LPF

000 = Small (default)

111 = Large

Phase Select**Subaddress 04h**

Default (80h)

| | | | | | | | |
|--------------------|---|---|---|---|---|----------|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Phase Select [4:0] | | | | | | Reserved | DIV2 |

Phase Select [4:0]: ADC Sampling clock phase select. (1 LSB = $360/32 = 11.25^\circ$)

DATACLK Divide-by-2

0 = DATACLK/1

1 = DATACLK/2

Clamp Start**Subaddress 05h**

Default (80h)

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Clamp Start [7:0] | | | | | | | |

Clamp Start [7:0]: Positions the clamp signal an integer number of clock periods after the HSYNC signal. If external clamping is selected this value has no meaning

Clamp Width**Subaddress 06h**

Default (80h)

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Clamp Width [7:0] | | | | | | | |

Clamp Width [7:0]: Sets the width in pixels for clamp. See register Clamp Start.

Table 6. Recommended Fine Clamp Settings

| VIDEO STANDARD | CLAMP START | CLAMP WIDTH |
|------------------|-------------|-------------|
| HDTV (tri-level) | 50 (32h) | 32 (20h) |
| SDTV (bi-level) | 6 (06h) | 16 (10h) |
| PC Graphics | 6 (06h) | 16 (10h) |

HSYNC Output Width

 Subaddress **07h**

Default (20h)

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HSOUT Width [7:0] | | | | | | | |

HSOUT Width [7:0]: Sets the width in pixels for HSYNC output.

Blue Fine Gain

 Subaddress **08h**

Default (80h)

| | | | | | | | |
|-----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Blue Gain [7:0] | | | | | | | |

 Blue Gain [7:0]: PGA digital gain (contrast) for Blue channel applied after the ADC. Gain = 1 + Blue Gain[7:0]/256
 80h = Recommended setting for 700 mVp-p input and default Coarse Gain (default).

Green Fine Gain

 Subaddress **09h**

Default (80h)

| | | | | | | | |
|------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Green Gain [7:0] | | | | | | | |

 Green Gain [7:0]: PGA digital gain (contrast) for Green channel applied after the ADC. Gain = 1 + Green Gain[7:0]/256
 80h = Recommended setting for 700 mVp-p input and default Coarse Gain (default).

Red Fine Gain

 Subaddress **0Ah**

Default (80h)

| | | | | | | | |
|----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Red Gain [7:0] | | | | | | | |

 Red Gain [7:0]: Sets PGA digital gain (contrast) for Red channel applied after the ADC. Gain = 1 + Red Gain[7:0]/256
 80h = Recommended setting for 700 mVp-p input and default Coarse Gain (default).

Blue Fine Offset

Subaddress 0Bh

Default (80h)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

Blue Offset [9:2]

Blue Offset [9:2]: DC digital offset (brightness) for Blue channel applied after the ADC.

The default setting of 80h will place the bottom-level (YRGB) clamped output blank levels at 0 and mid-level clamped (PbPr) output blank levels at 512.

| Blue Offset | Description |
|-------------|-------------|
| 11111111 | maximum |
| 100000001 | 1 LSB |
| 10000000 | 0 (default) |
| 01111111 | -1 LSB |
| 00000000 | minimum |

Green Fine Offset

Subaddress 0Ch

Default (80h)

| | | | | | | | |
|--------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Green Offset [9:2] | | | | | | | |

Green Offset [9:2]: DC digital offset (brightness) for Green channel applied after the ADC. See Red Fine Offset register at I²C address 0x0B.

Red Fine Offset

Subaddress 0Dh

Default (80h)

| | | | | | | | |
|------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Red Offset [9:2] | | | | | | | |

Red Offset [9:2]: DC digital offset (brightness) for Red channel applied after the ADC. See Blue Fine Offset register at I²C address 0x0B.

Sync Control 1

 Subaddress **0Eh**

Default (40h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|-----|
| HSPO | HSIP | HSOP | AHSO | AHSS | VSOI | AVSO | AVS |

HSPO: HSYNC Polarity Override

- 0 = Polarity determined by chip (default)
- 1 = Polarity set by Bit 6 in register 0Eh

HSIP: HSYNC Input Polarity

- 0 = Indicates input HSYNC polarity active low
- 1 = Indicates input HSYNC polarity active high (default)

HSOP: HSYNC Output Polarity

- 0 = Active low (default)
- 1 = Active high

AHSO: Active HSYNC Override

- 0 = The active interface is selected via Bit 6 in register 14h, selected by chip (default)
- 1 = The user can select HSYNC to be used via Bit 3

AHSS: Active HSYNC Select. The indicated HSYNC will be used only if Bit 4 is set to 1 or both syncs are active (Bits 1,7 =1 in 14h)

- 0 = Select HSYNC as the active sync (default)
- 1 = Select Sync-on-green as the active sync

VSOI: VSYNC Output Invert (relative to VSYNC IN polarity)

- 0 = No invert (default)
- 1 = Invert

AVSO: Active VSYNC Override

- 0 = The active interface is selected via Bit3 in register 14h, selected by chip (default)
- 1 = The user can select the VSYNC to be used via Bit 0

AVS: Active VSYNC select, This bit is effective when AVSO Bit 1 is set to 1.

- 0 = Raw VSYNC (default)
- 1 = Sync separated VSYNC

PLL and Clamp Control

| Subaddress | 0Fh | Default (4Eh) | | | | | | |
|------------|-----|---------------|-----|-----|----------|------|----------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| CF | CP | Coast Sel | CPO | CPC | Reserved | FCPD | Free run | |

Clamp Function:

- 0 = Internal Clamp (default)
- 1 = External Clamp

Clamp Polarity:

- 0 = Active high
- 1 = Active low (default)

Coast Select:

- 0 = External coast (default)
- 1 = Internal Coast

Coast Polarity Override:

- 0 = Polarity determined by chip (default)
- 1 = Polarity set by Bit 3 in register 0Fh

Coast Polarity Change:

- 0 = Active low
- 1 = Active high (default)

Full Chip Power-Down:

- 0 = Power-down mode
- 1 = Normal operation (default)

Free run: Also ADC test mode, ADC uses external clock

- 0 = PLL normal operation (default)
- 1 = Enabled

Sync On_Green Threshold

| Subaddress | 10h | Default (B8h) | | | | | | |
|---------------------|-----|---------------|---|---|---------|----------|--------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| SOG Threshold [4:0] | | | | | Blue CS | Green CS | Red CS | |

SOG Threshold [4:0]: Sets the voltage level of the SOG slicer comparator. The minimum setting is 0 mV and the maximum is 350 mV. The step is 11 mV. (default 17h, 10h recommended)

Blue Clamp Select: When free running mode this bit is no effect

- 0 = Bottom level clamp (default)
- 1 = Mid level clamp

Green Clamp Select: When free running mode this bit is no effect

- 0 = Bottom level clamp (default)
- 1 = Mid level clamp

Red Clamp Select: When free running mode this bit is no effect.

- 0 = Bottom level clamp (default)
- 1 = Mid level clamp

Sync Separator Threshold

Subaddress 11h

Default (20h)

| | | | | | | | |
|--------------------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Sync Separator Threshold [7:0] | | | | | | | |

Sync Separator Threshold [7:0]: Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high or low. The selection of this register affects the VSYNC out position relative to HSYNC out.

Pre-Coast

Subaddress 12h

Default (00h)

| | | | | | | | |
|-----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Pre-Coast [7:0] | | | | | | | |

Pre-Coast [7:0]: Sets the number of HSYNC periods that coast becomes active prior to VSYNC.

Post-Coast

Subaddress 13h

Default (00h)

| | | | | | | | |
|------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Post-Coast [7:0] | | | | | | | |

Post-Coast [7:0]: Sets the number of HSYNC periods that coast stays active following VSYNC.

Table 7. Recommended Pre and Post-Coast Settings

| STANDARD | PRE_COAST | POST-COAST |
|-------------------------|-----------|------------|
| 480i/p with Macrovision | 3 | 0Ch |
| 576i/p with Macrovision | 3 | 0Ch |
| 1080i | 3 | 0 |
| 1080p | 0 | 0 |
| 720p | 0 | 0 |

Sync Detect Status

Subaddress 14h

Read Only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-------|-----|-----|------|------|------|
| HSD | AHS | IHSPD | VSD | AVS | VSPD | SOGD | ICPD |

Hsync Detect:

0 = No Hsync detected

1 = Hsync detected

Active Hsync:

0 = Hsync input pin

1 = Hsync from SOG

Input Hsync Polarity Detect:

0 = Active low

1 = Active high

Vsync Detect:

0 = No Vsync detected

1 = Vsync detected

AVS:

0 = Vsync input pin

1 = Vsync from Sync separator

Vsync Polarity Detect:

0 = Active low

1 = Active high

SOG Detect:

0 = No SOG detected

1 = SOG is present on the SOG interface

Input Coast Polarity Detect:

0 = Active low

1 = Active high

Output Formater

Subaddress 15h

Default (00h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|-----------|------------|---------|----------|
| Reserved | | | | Clamp REF | CbCr order | 422/444 | Reserved |

Clamp REF:

0 = Clamp pulse placement respect to the trailing edge of Hsync (default)

1 = Clamp pulse placement respect to the leading edge of Hsync

CbCr order: This bit is effective when Bit 1 is set to 1.

0 = CrCb (default)

1 = CbCr

422/444:

0 = Output is in 4:4:4 format (default)

1 = Output is in 4:2:2 format

Test Register
Subaddress 16h

Default (00h)

| | | | | | | | |
|-----------------------|---|----------|---|-------------|---|--------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Pixel tolerance [2:0] | | Reserved | | Test output | | PLL PD | STRTB |

Pixel tolerance:

- 000 = No tolerance (default)
- 001 = 1 pixel tolerance (recommended setting for best SOG performance)
- 111 = 7 pixel tolerance (maximum)

Test output: Controls TEST 1 pin output

- 00 = 5 MHz clock (default)
- 01 = Coast output
- 10 = Clamp
- 11 = High impedance

PLL PD: PLL power-down

- 0 = Normal operation (default)
- 1 = PLL powered down

STRTB: PLL start-up circuit enable

- 0 = Disabled (default)
- 1 = Enabled

Input Mux Select 1
Subaddress 19h

Default (00h)

| | | | | | | | |
|------------------|---|------------------|---|--------------------|---|-------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOG Select [1:0] | | Red Select [1:0] | | Green Select [1:0] | | Blue Select [1:0] | |

SOG Select [1:0]:

- 00 = CH1 selected (default)
- 01 = CH2 selected
- 10 = CH3 selected
- 11 = Reserved

Red Select [1:0]:

- 00 = CH1 selected (default)
- 01 = CH2 selected
- 10 = CH3 selected
- 11 = Reserved

Green Select [1:0]:

- 00 = CH1 selected (default)
- 01 = CH2 selected
- 10 = CH3 selected
- 11 = CH4 selected

Blue Select [1:0]:

- 00 = CH1 selected (default)
- 01 = CH2 selected
- 10 = CH3 selected
- 11 = Reserved

Input Mux Select 2

| Subaddress 1Ah | | | | | | | | Default (00h) |
|----------------|---|----------|---|---|--------------|----------|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 1 | | Reserved | | | VSYNC Select | Reserved | | Hsync Select |

Bit 7: It must be written to 1.

VSYNC Select:

- 0 = VSYNC_A selected (default)
- 1 = VSYNC_B selected

Hsync Select [1:0]:

- 0 = HSYNC_A selected (default)
- 1 = HSYNC_B selected

Blue and Green Coarse Gain

| Subaddress 1Bh | | | | | | | | Default (55h) |
|----------------|---|------------------|---|---|---|-----------------|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | Green Gain [3:0] | | | | Blue Gain [3:0] | | |

Green Coarse Gain [3:0]: Coarse analog gain for Green channel applied before the ADC.

Gain [3:0] Description

| | |
|------|-------|
| 0000 | = 0.5 |
| 0001 | = 0.6 |
| 0010 | = 0.7 |
| 0011 | = 0.8 |
| 0100 | = 0.9 |
| 0101 | = 1.0 |
| 0110 | = 1.1 |
| 0111 | = 1.2 |
| 1000 | = 1.3 |
| 1001 | = 1.4 |
| 1010 | = 1.5 |
| 1011 | = 1.6 |
| 1100 | = 1.7 |
| 1101 | = 1.8 |
| 1110 | = 1.9 |
| 1111 | = 2.0 |

Maximum recommended gain for 700mVp-p input.

Blue Coarse Gain [3:0]: Coarse gain for Blue channel

Red Coarse Gain

| Subaddress 1Ch | | | | | | | | Default (05h) |
|----------------|---|----------|---|---|---|----------------|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | Reserved | | | | Red Gain [3:0] | | |

Red Coarse Gain [3:0]: Coarse analog gain for Red channel applied before the ADC.

Fine Offset LSB

| Subaddress 1Dh | | | | | | | | Default (00h) |
|----------------|---|---|------------------|--------------------|-------------------|---|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reserved | | | Red Offset [1:0] | Green Offset [1:0] | Blue Offset [1:0] | | | |

Red Offset [1:0] : Offset LSB for red channel. This is LSB of register 0x0D

Green Offset [1:0] : Offset LSB for green channel. This is LSB of register 0x0C

Blue Offset [1:0] : Offset LSB for blue channel. This is LSB of register 0x0B

Blue Coarse Offset

| Subaddress 1Eh | | | | | | | | Default (20h) |
|----------------|---|---|---|-------------------|---|---|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reserved | | | | Blue offset [5:0] | | | | |

Blue Coarse offset [5:0]: Coarse analog offset for blue channel applied before the ADC.

1Fh = +31 LSB (Recommended for optimum ALC performance)

00h = 0 LSB

20h = -1 LSB (default)

3Fh = -32 LSB

Green Coarse Offset

| Subaddress 1Fh | | | | | | | | Default (20h) |
|----------------|---|---|---|---------------------------|---|---|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reserved | | | | Coarse Green offset [5:0] | | | | |

Green Coarse offset [5:0]: Coarse analog offset for green channel applied before the ADC.

1Fh = +31 LSB (Recommended for optimum ALC performance)

Red Coarse Offset

| Subaddress 20h | | | | | | | | Default (20h) |
|----------------|---|---|---|-------------------------|---|---|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reserved | | | | Coarse Red offset [5:0] | | | | |

Red Coarse offset [5:0]: Coarse analog offset for blue channel applied before the ADC.

1Fh = +31 LSB (Recommended for optimum ALC performance)

HSOUT Output Start

| Subaddress 21h | | | | | | | | Default (09h) |
|----------------|---|---|---|-------------------|---|---|---|---------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Reserved | | | | HSOUT Start [7:0] | | | | |

HSOUT Start [7:0]: HSYNC output Start pixel number.

MISC Control**Subaddress 22h**

Default (00h)

| | | | | | | | |
|---|---|----------|---|--------|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | Reserved | | MAC_EN | Reserved | VS_ALIGN | Reserved |

MAC_EN:

0 = Macrovision compatibility disabled (default)

1 = Macrovision compatibility enabled

VS_ALIGN

0 = VSOUT alignment relative to HSOUT varies with SyncSep Threshold

1 = VSOUT alignment not affected by SyncSep Threshold

Automatic Level Control Enable**Subaddress 26h**

Default (00h)

| | | | | | | | |
|------------|---|---|---|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ALC enable | | | | Reserved | | | |

ALC enable: Automatic level control enable

0 = Disabled (default)

1 = Enabled

Automatic Level Control Filter

Subaddress 28h

Default (00h)

| | | | | | | | |
|----------|---|----------|---|---|-----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | NSV[3:0] | | | NSH [2:0] | | |

The horizontal ALC coefficient (NSH) specifies the number of the horizontal samples (N) used to calculate the average blank level per horizontal line. Offset error correction is applied immediately based on the vertical (NSV) coefficient.

The vertical coefficient (NSV) specifies the amount of offset error correction (derived from NSH) that is applied to each line update.

NSV [3:0]: ALC vertical filter coefficient

| NSV [3:0] | Description |
|--------------------|--|
| 0000 = 1 (default) | Maximum error correction applied per line update |
| 0001 = 1/2 | |
| 0010 = 1/4 | |
| 0011 = 1/8 | |
| 0100 = 1/16 | |
| 0101 = 1/32 | |
| 0110 = 1/64 | |
| 0111 = 1/128 | |
| 1000 = 1/256 | |
| 1001 = 1/512 | |
| 1010 = 1/1024 | |
| 1011 = 1/2048 | |
| 1100 = 1/4096 | |
| 1101 = 1/8192 | |
| 1110 = 1/16384 | |
| 1111 = 1/32768 | Minimum error correction applied per line update |

NSH [2:0]: ALC horizontal sample filter coefficient

| NSH [2:0] | Description |
|-------------------|--|
| 000 = 1 (default) | Minimum number of pixels used in horizontal filter |
| 001 = 1/2 | |
| 010 = 1/4 | |
| 011 = 1/8 | |
| 100 = 1/16 | |
| 101 = 1/32 | |
| 110 = 1/64 | |
| 111 = 1/128 | Maximum number of pixels used in horizontal filter |

Fine Clamp Control

Subaddress 2Ah

(Default 00h)

| | | | | | | | |
|---|----------|---|---|-----------------|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Reserved | | | Fine swsel[1:0] | Fine B | Fine G | Fine R |

Fine swsel: Fine clamp time constant adjustment

00 = Highest (default)

01 =

10 =

11 = Lowest

Fine B:

0 = Blue channel fine clamp is off (default)

1 = Blue channel fine clamp is on

Fine G:

0 = Green channel fine clamp is off (default)

1 = Green channel fine clamp is on

Fine R:

0 = Red channel fine clamp is off (default)

1 = Red channel fine clamp is on

Power Control

Subaddress 2Bh

(Default 00h)

| | | | | | | | |
|---|-----|--------|-----|---------|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | SOG | SLICER | REF | CURRENT | PW ADC B | PW ADC G | PW ADC R |

SOG:

0 = Normal operation (default)

1 = SOG power-down

Slicer:

0 = Normal operation (default)

1 = Slicer power-down

Reference:

0 = Normal operation (default)

1 = Reference block power-down

Current control:

0 = Normal operation (default)

1 = Current control block power-down

PW ADC B: Power-down ADC blue channel

0 = PW ADC R: Power-down ADC red channel

1 = ADC channel 1 power-down

PW ADC G: Power-down ADC green channel

0 = PW ADC R: Power-down ADC red channel

1 = ADC channel 2 power-down

PW ADC R: Power-down ADC red channel

0 = PW ADC R: Power-down ADC red channel

1 = ADC channel 3 power-down

ADC Setup

 Subaddress **2Ch**

(Default 00h)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

50h = Recommended setting

Coarse Clamp Control

 Subaddress **2Dh**

Default (00h)

| | | | | | | | |
|---------------|---|----------|---|----------|----------|----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CCCLP_cur_CH1 | | Reserved | | Coarse B | Coarse G | Coarse R | |

Coarse clamp charge current switch selection:

00 = Highest (default)

01 =

10 =

11 = Lowest

Course B:

0 = Coarse clamp off at BLUE channel (default)

1 = Coarse clamp on at BLUE channel

Coarse G :

0 = Coarse clamp off at GREEN channel (default)

1 = Coarse clamp on at GREEN channel

Coarse R :

0 = Coarse clamp off at RED channel (default)

1 = Coarse clamp on at RED channel

SOG Clamp

 Subaddress **2Eh**

(Default 00h)

| | | | | | | | |
|--------|---|----------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOG_CE | | Reserved | | | | | |

SOG_CE:

0 = SOG Clamp disabled (default)

1 = SOG Clamp enabled. Set to 1 for SOG operation.

ALC Placement

 Subaddress **31h**

(Default 00h)

| | | | | | | | |
|---------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ALC placement [7:0] | | | | | | | |

ALC placement [7:0]:

0 = Default

 18h = PC graphics and SDTV with
bi-level syncs

5Ah = HDTV with tri-level syncs

Positions the ALC signal an integer number of clock periods after the HSYNC signal. ALC must be applied after the clamp end.

APPLICATION INFORMATION

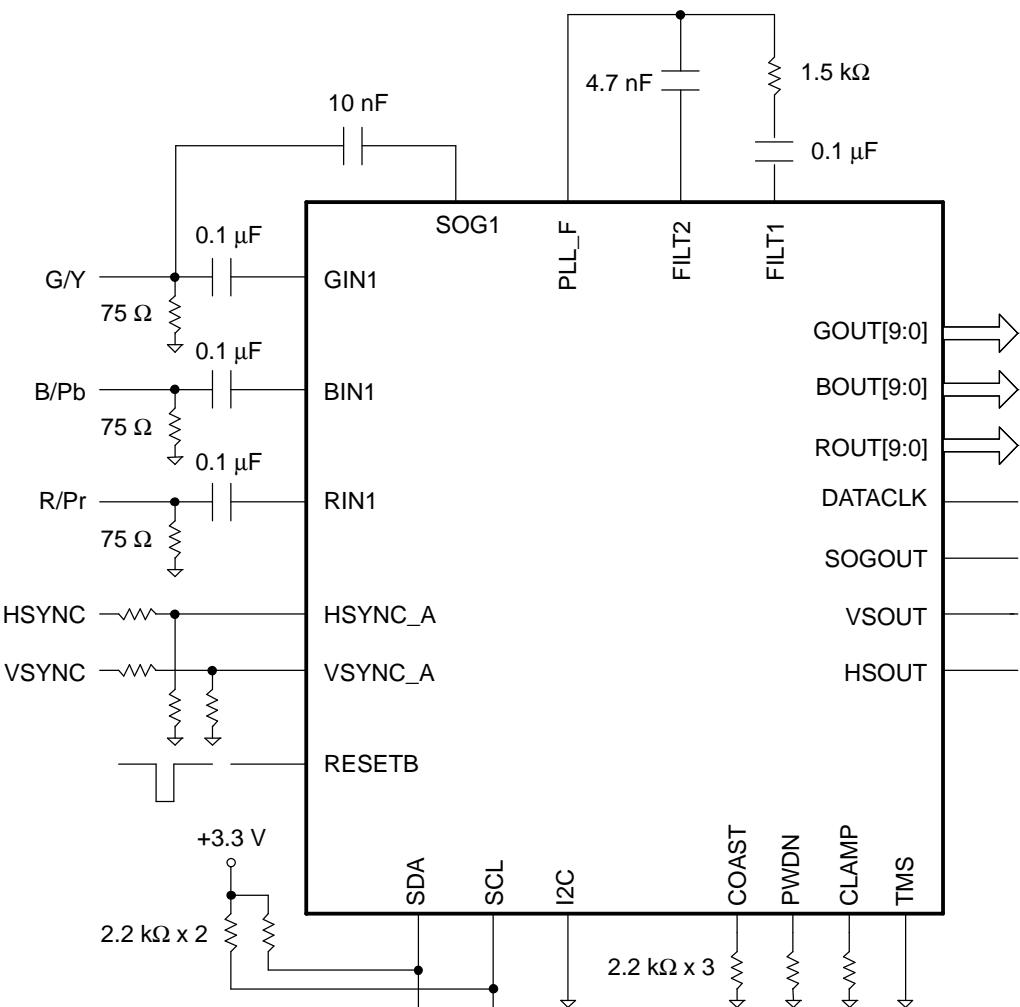
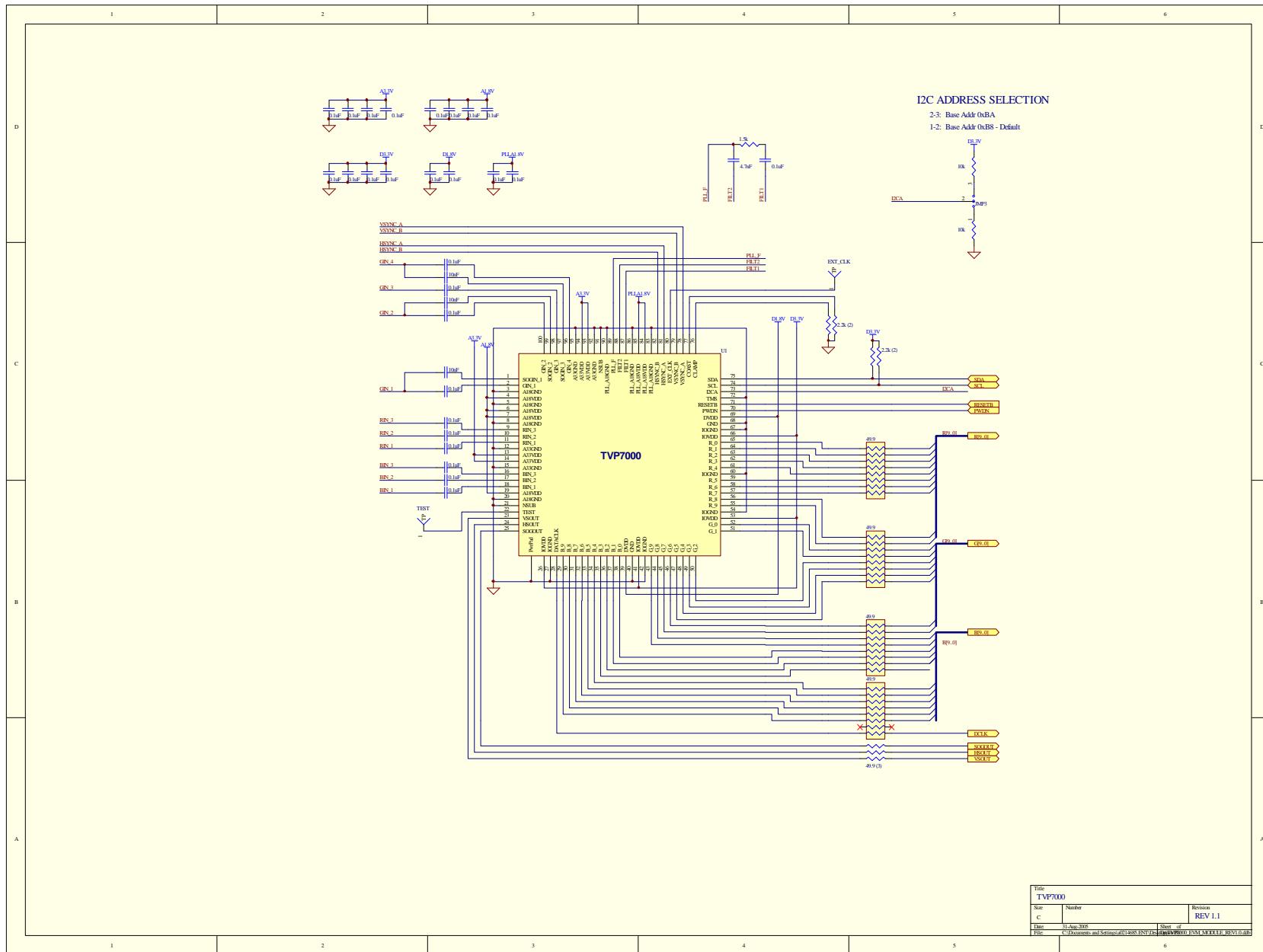


Figure 8. TVP7000 Application Example

Schematic



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TVP7000PZP | ACTIVE | HTQFP | PZP | 100 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TVP7000PZPG4 | ACTIVE | HTQFP | PZP | 100 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TVP7000PZPR | ACTIVE | HTQFP | PZP | 100 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| TVP7000PZPRG4 | ACTIVE | HTQFP | PZP | 100 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

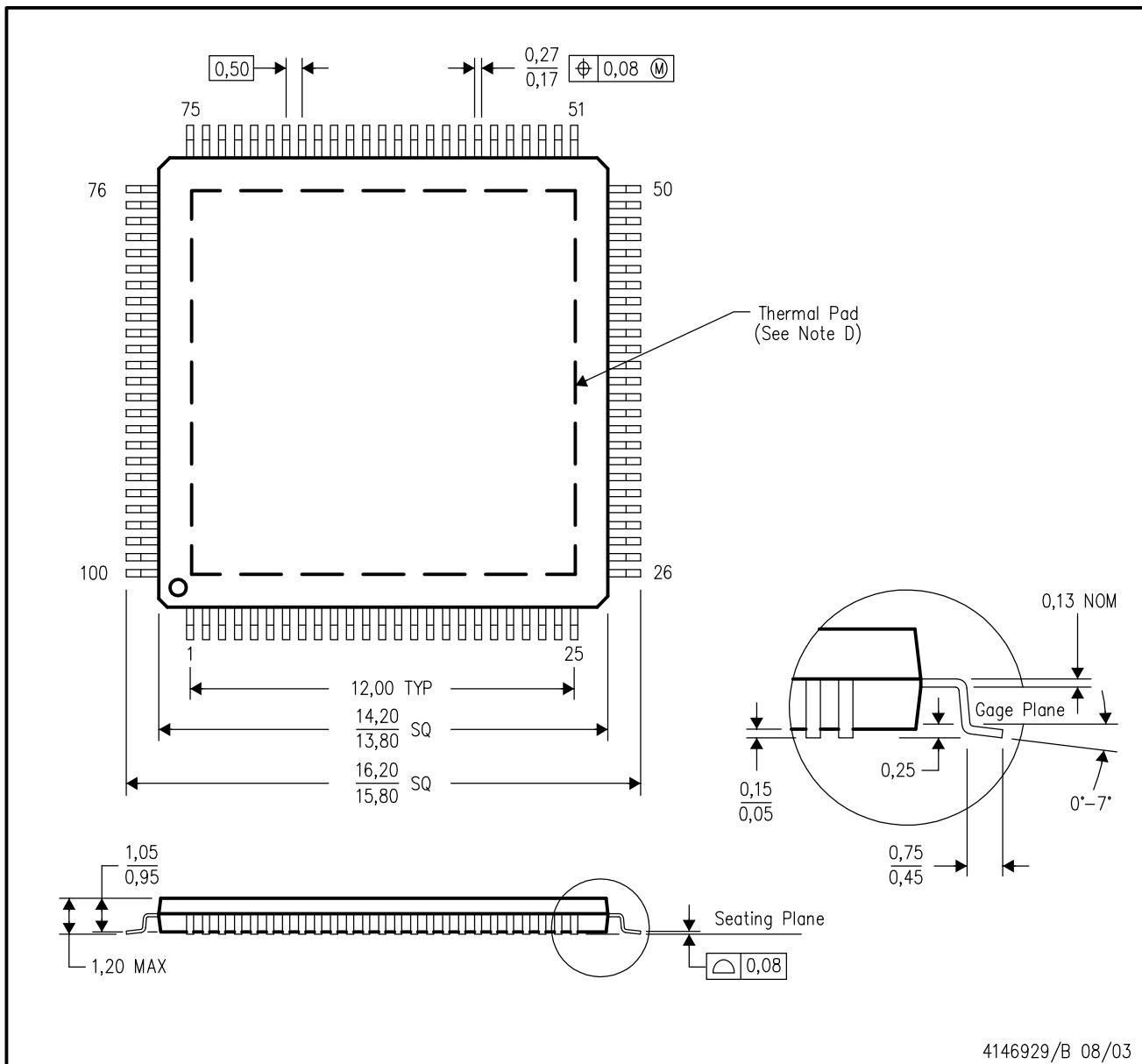
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PZP (S-PQFP-G100)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MS-026

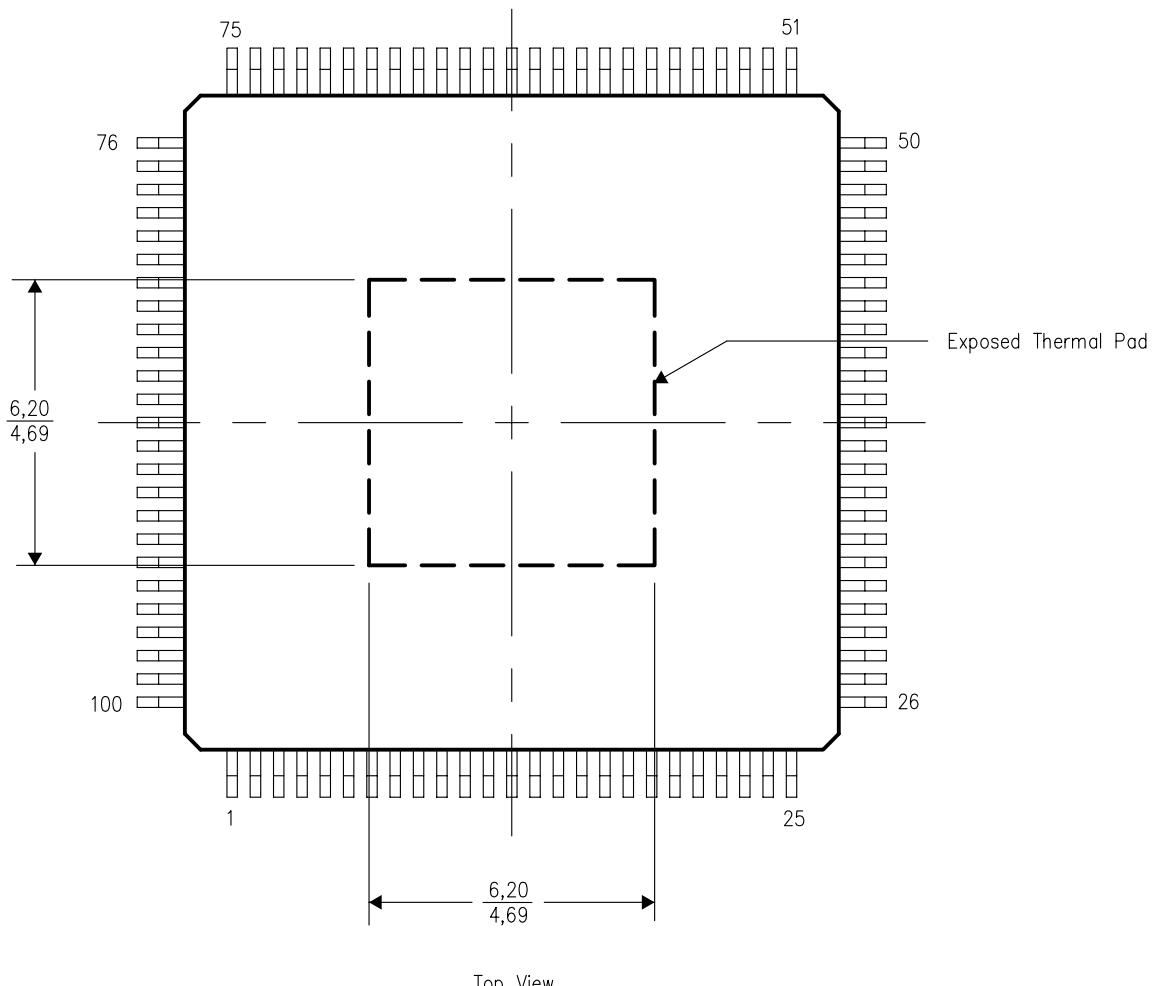
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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