
Real-Time Clock + 64Kbit (8192 x 8) EEPROM

Features

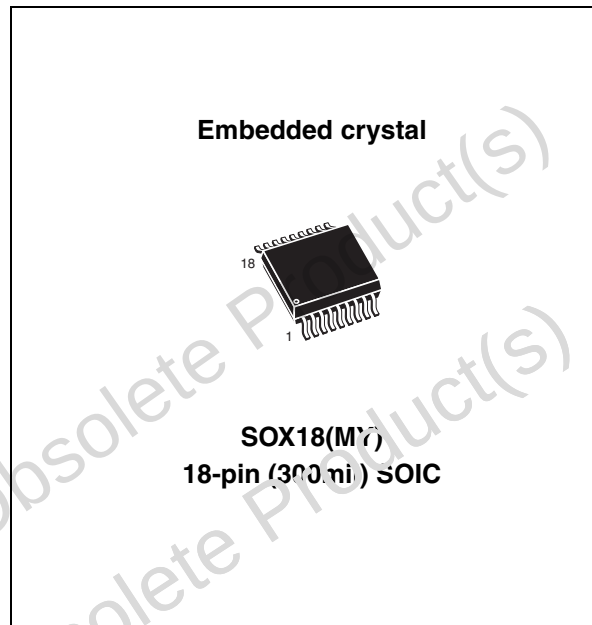
- 2.7V to 5.5V supply voltage
- I²C bus compatible
- Operating temperature of –40 to 85°C
- Packaging includes:
 - 18-lead SOIC (with embedded crystal)
- RoHS compliant

Serial RTC features (M41T00S)

- Counters for seconds, minutes, hours, day, date, month, years, and century
- Embedded crystal package
- Software clock calibration
- Factory calibrated to ± 5 ppm
- Automatic power-fail detect and switch-over circuitry
- Ultra-low battery supply current of 600nA (typ)
- Automatic leap year compensation
- Special software programmable output
- Two-wire I²C serial interface supports 400kHz protocol

Serial EEPROM features (M24C64)

- 8192 bytes of general purpose EEPROM (more than 1E6 erase/write cycles)
- Two-wire I²C serial interface supports 400kHz protocol
- Byte and page write (up to 32 bytes)
- More than 40 year data retention
- Self-timed programming cycle



Contents

1	Summary description	5
1.1	Calibration	5
2	Pin settings	6
2.1	Pin description	6
2.2	Pin connections	6
3	Application	7
4	Operation	9
4.1	Serial RTC device	9
4.2	EEPROM device	9
5	Maximum rating	10
6	DC and AC parameters	11
7	Package mechanical data	15
8	Order codes	17
9	Revision history	18

List of tables

Table 1.	Signal names	6
Table 2.	Device select code	8
Table 3.	Absolute maximum ratings	10
Table 4.	Operating and AC measurement conditions	11
Table 5.	Capacitance and input parameters	12
Table 6.	DC characteristics	12
Table 7.	AC characteristics, (serial RTC, M41T00S)	13
Table 8.	AC characteristics (serial EEPROM, M24C64)	14
Table 9.	SOX18 – 18-lead plastic small outline, 300mils, embedded crystal, package mech.	16
Table 10.	Ordering information scheme	17
Table 11.	Revision history	18

List of figures

Figure 1.	Logic diagram	5
Figure 2.	18-pin SOIC connection	6
Figure 3.	Block diagram	7
Figure 4.	Crystal accuracy across temperature	7
Figure 5.	AC measurement I/O waveform	11
Figure 6.	AC Bus timing requirements sequence (serial RTC)	13
Figure 7.	SOX18 – 18-lead plastic small outline, 300mils, embedded crystal	16

1 Summary description

The M41T00SC64 is a low power, Serial Real Time Clock plus a 64Kb EEPROM (see [Figure 3](#)). A built-in 32,768Hz oscillator (crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line, bi-directional bus. The built-in address register is incremented automatically after each WRITE or READ data byte.

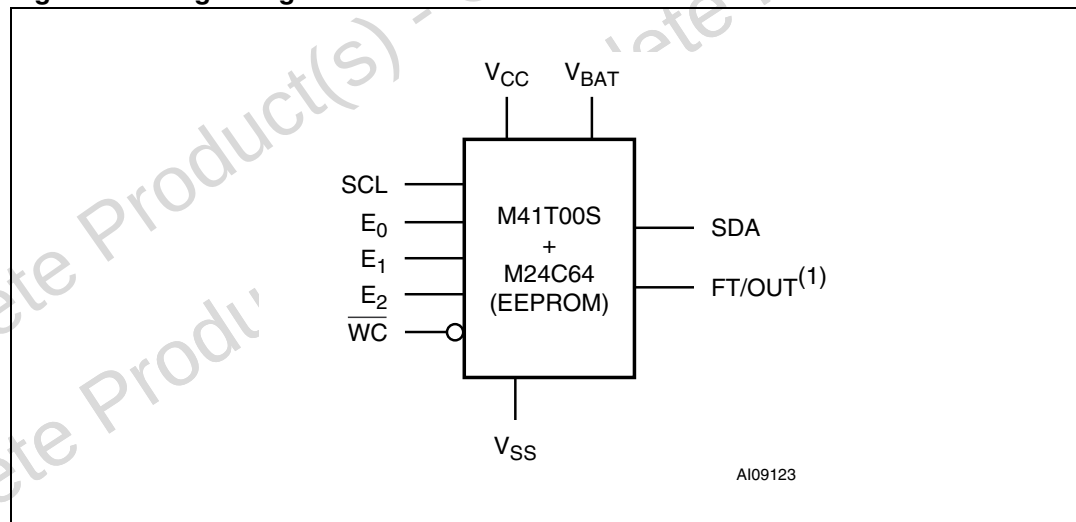
The M41T00SC64 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the clock operations can be supplied from a small lithium coin cell.

Typical data retention time for the Serial RTC is in excess of 9.5 years with a 50mAh, 3V lithium cell. The M41T00SC64 is supplied in an 18-lead Plastic SOIC package.

1.1 Calibration

As the crystal is molded together with the silicon in this package, ST can program the appropriate calibration value necessary to achieve ± 5 ppm accuracy at 25°C after two SMT reflows (see [Figure 4](#)). This calibration value will be written into address 1550h of the EEPROM. This clock accuracy can then be guaranteed to drift no more than ± 3 ppm the first year, and ± 1 ppm for each following year due to crystal aging.

Figure 1. Logic diagram



1. Open drain output

2 Pin settings

2.1 Pin description

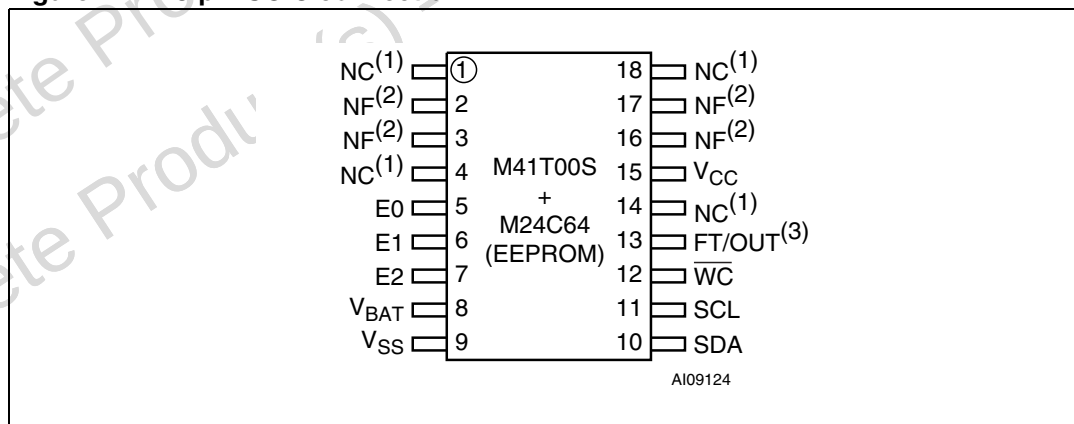
Table 1. Signal names

FT/OUT ⁽¹⁾	Frequency test / output driver (open drain)
SDA	Serial data address input / output
SCL	Serial clock
$\overline{WC}$	Write control
E0, E1, E2	Chip enables
V _{BAT}	Battery supply voltage
V _{CC}	Supply voltage
V _{SS}	Ground
NC ⁽²⁾	No connect
NF ⁽³⁾	No function

1. Open drain output
2. No connect (NC) pins should be tied to V_{SS}.
3. No function (NF) pins should be tied to V_{SS}. Pins 2 and 3, and pins 16 and 17 are internally shorted together.

2.2 Pin connections

Figure 2. 18-pin SOIC connection



1. No connect (NC) pins should be tied to V_{SS}.
2. No function (NF) pins should be tied to V_{SS}. Pins 2 and 3, and pins 16 and 17 are internally shorted together.
3. Open drain output.

3 Application

Figure 3. Block diagram

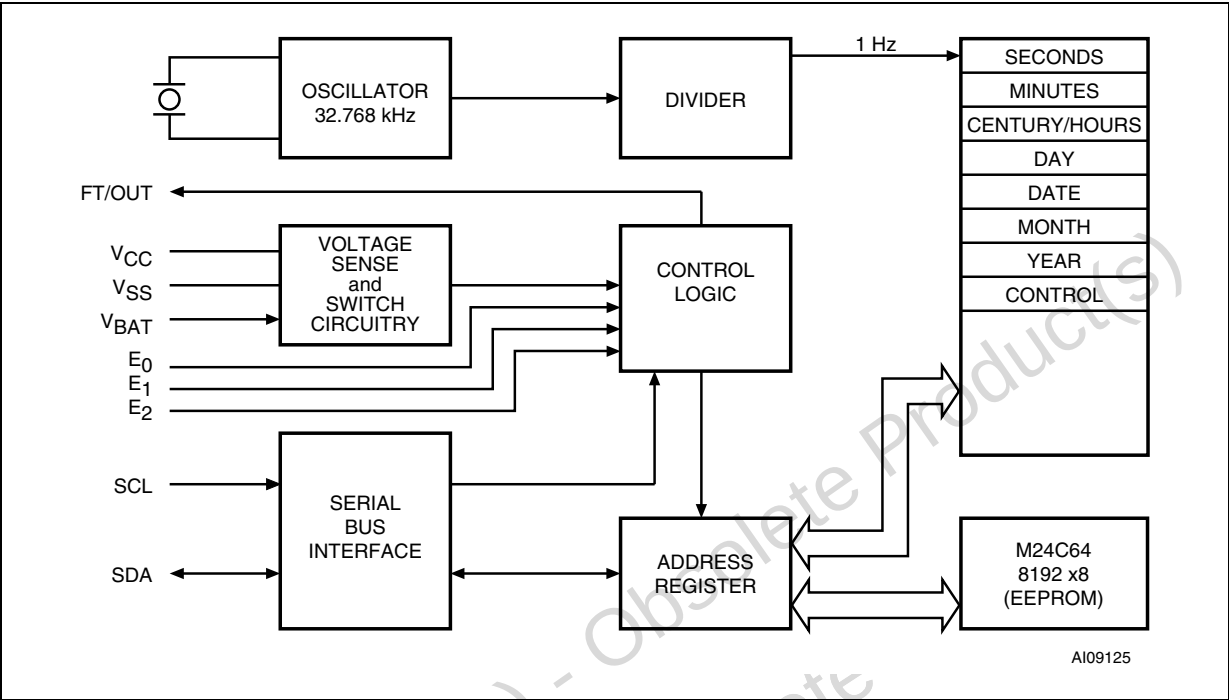


Figure 4. Crystal accuracy across temperature

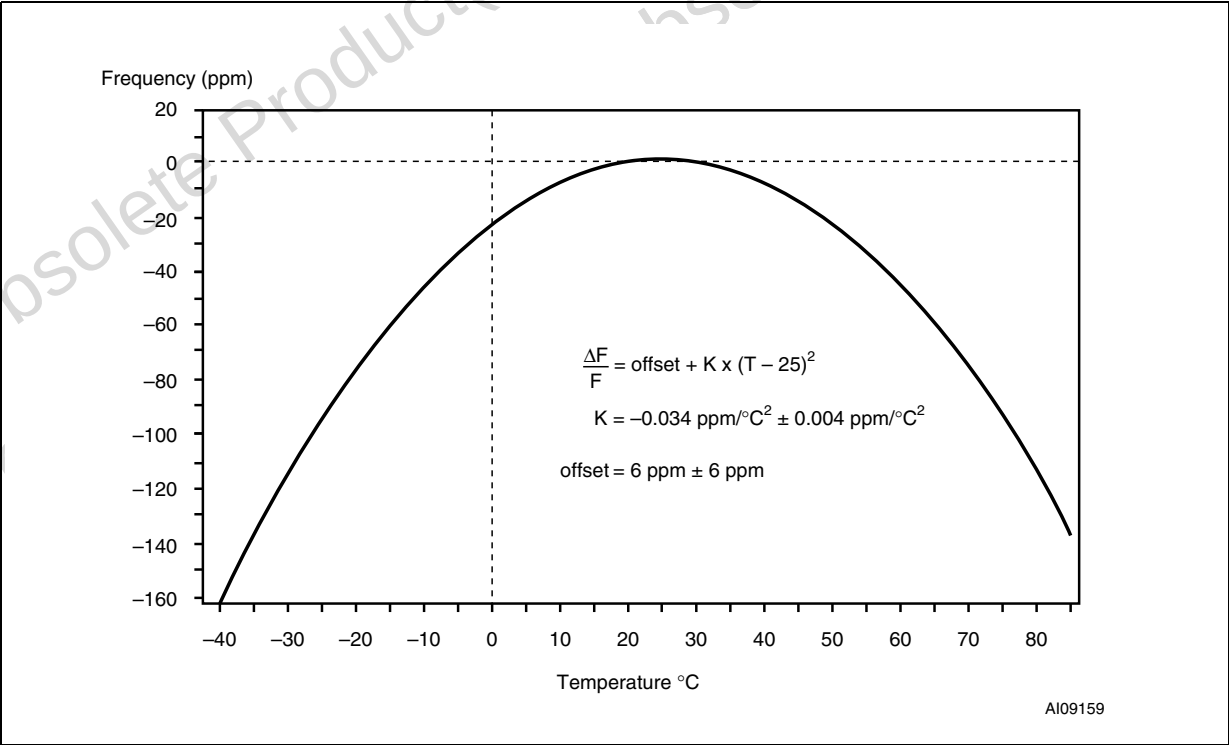


Table 2. Device select code

	Device type identifier ⁽¹⁾				Chip enable address ⁽²⁾			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
M24C64	1	0	1	0	E2	E1	E0	$\overline{RW}$
M41T00S	1	1	0	1	0	0	0	RW

1. The most significant bit, b7, is sent first.

2. E0, E1, and E2 are compared against the respective external pins on the memory device.

4 Operation

4.1 Serial RTC device

The M41T00SC64 contains one Serial RTC (M41T00S). For detailed information on how to use the devices, see the M41T00S datasheet, which is available from your local STMicroelectronics distributor or from the STMicroelectronics website, <http://www.st.com/rtc/>.

4.2 EEPROM device

The M41T00SC64 contains a 64 Kbit Serial EEPROM (M24C64). For detailed information on how to use the devices, see the M24C64 datasheet, which is available from your local STMicroelectronics distributor or from the STMicroelectronics website, <http://www.st.com/eeprom/>.

5 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	–40 to 85	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–55 to 125	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	240	°C
V_{IO}	Input or output voltages	–0.3 to 6.5	V
V_{CC}	Supply voltage	–0.3 to 6.5	V
I_O	Output current	20	mA
P_D	Power dissipation	0.25	W

1. For SOX18 package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 240°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds). No direct exposure to infrared (IR) reflow, or IR preheat allowed, to avoid damaging the embedded 32KHz crystal.

Caution: *Negative undershoots below –0.3V are not allowed on any pin while in the battery back-up mode.*

6 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC measurement conditions⁽¹⁾

Parameter	Value	Unit
Supply voltage (V_{CC})	2.7 to 5.5	V
Ambient operating temperature (T_A)	-40 to 85	°C
Load capacitance (C_L)	100	pF
Input rise and fall times	< 5	ns
Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$	V
Input and output timing ref. voltages	$0.3V_{CC}$ to $0.7V_{CC}$	V

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC measurement I/O waveform

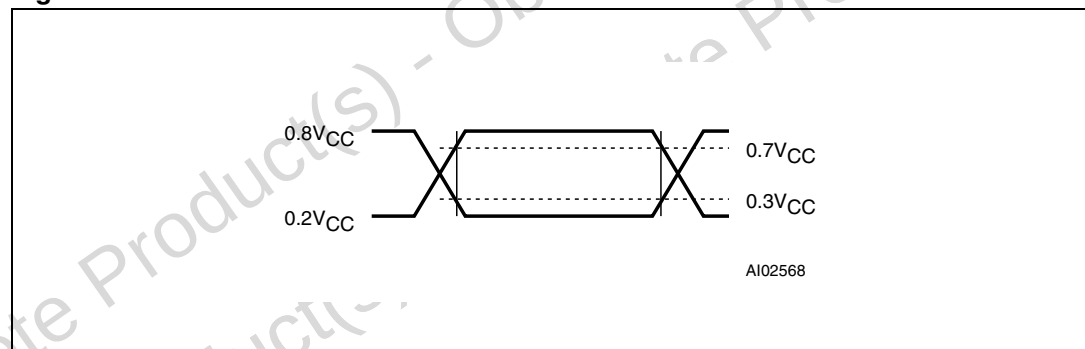


Table 5. Capacitance and input parameters

Symbol	Parameter ⁽¹⁾⁽²⁾	Test condition	Min	Max	Unit
C _{IN}	Input capacitance (SCL)			13	pF
	Input capacitance (SDA)			18	pF
	Input Capacitance (Other pins)			6	pF
Z _{WCL}	$\overline{WC}$ input impedance	V _{IN} < 0.3V	50	200	kΩ
Z _{WCH}	$\overline{WC}$ input impedance	V _{IN} < 0.7V _{CC}	500		kΩ
C _{OUT} ⁽³⁾	Output capacitance (SDA)			18	pF
	Output capacitance (FT/OUT)			10	pF

1. Effective capacitance measured with power supply at 5V; sampled, not 100% tested.

2. At 25°C, f = 400kHz..

3. Outputs deselected.

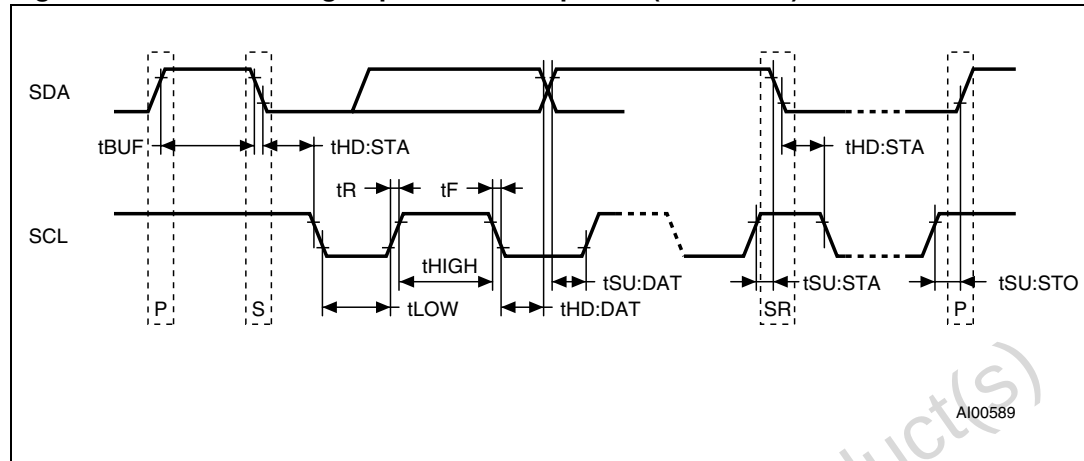
Table 6. DC characteristics

Symbol	Parameter	Test Condition ⁽¹⁾	Min	Typ	Max	Unit
I _{LI}	Input leakage current	0V ≤ V _{IN} ≤ V _{CC}			±3	μA
I _{LO}	Output leakage current	0V ≤ V _{OUT} ≤ V _{CC}			±3	μA
I _{CC1}	Supply current (serial RTC active)	Switch frequency = 400kHz			300	μA
	Supply current (serial EEPROM active)	V _{CC} = 5V, f _c =400kHz (rise/fall time < 30ns)			2	mA
I _{CC2}	Supply current (standby)	SCL, SDA = V _{CC} - 0.3V		100		μA
V _{IL}	Input low voltage		-0.3		0.3 V _{CC}	V
V _{IH}	Input high voltage		0.7V _{CC}		V _{CC} + 0.3	V
V _{OL} ⁽²⁾	Output low voltage	I _{OL} = 2.1mA			0.4	V
	Output voltage (open drain) ⁽²⁾	I _{OL} = 10mA			0.4	V
V _{BAT} ⁽³⁾	Battery supply voltage		2.5	3	3.5	V
I _{BAT}	Battery supply current	T _A = 25°C, V _{CC} = 0V, Oscillator ON, V _{BAT} = 3V		0.6	1	μA

1. Valid for ambient operating temperature: T_A = -40 to 85°C; V_{CC} = 2.7 to 5.5V (except where noted).

2. For FT/OUT pin (open drain)

3. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.

Figure 6. AC Bus timing requirements sequence (serial RTC)**Table 7. AC characteristics, (serial RTC, M41T00S)**

Symbol	Parameter ⁽¹⁾	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
t_{LOW}	Clock low period	1.3		μs
t_{HIGH}	Clock high period	600		ns
t_R	SDA and SCL rise time		300	ns
t_F	SDA and SCL fall time		300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{HD:DAT}^{(2)}$	Data hold time	0		μs
$t_{SU:STO}$	STOP condition setup time	600		ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		μs
t_{LP}	Low-pass filter input time constant (SDA and SCL) for Serial RTC		50	ns

1. Valid for ambient operating temperature: $T_A = -40$ to $85^\circ C$; $V_{CC} = 2.7$ to $5.5V$ (except where noted).

2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

Table 8. AC characteristics (serial EEPROM, M24C64)

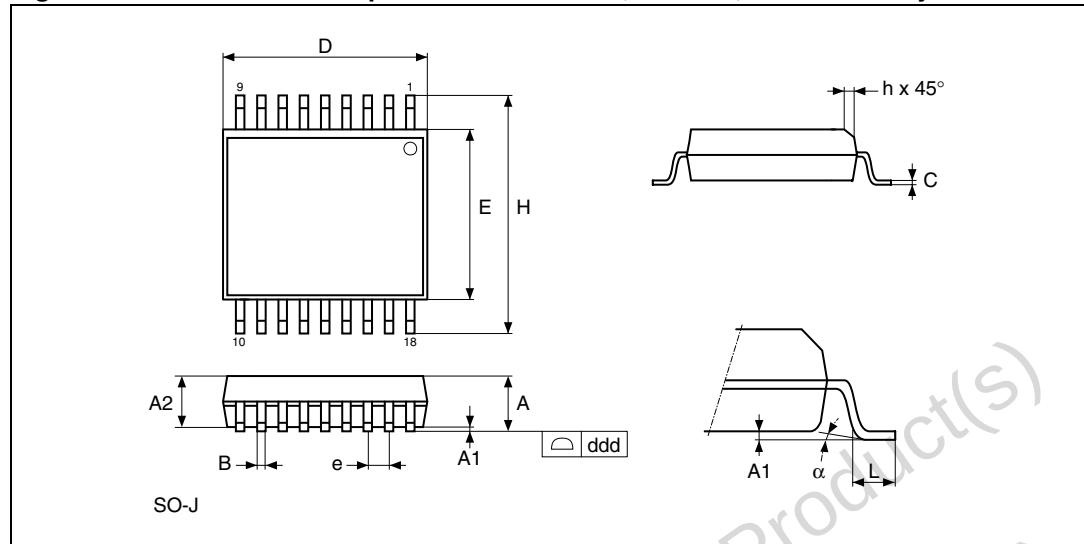
Symbol	Alt.	Parameter	Test condition	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency			400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high		600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low		1300		ns
$t_{DL1DL2}^{(1)}$	t_F	SDA fall time		20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time		100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time		0		ns
t_{CLQX}	t_{DH}	Data out hold time		200		ns
$t_{CLQV}^{(2)}$	t_{AA}	Clock low to next data valid (access time)		200	900	ns
$t_{CHDX}^{(3)}$	$t_{SU:STA}$	Start condition set up time		600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time		600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time		600		ns
t_{DHDL}	t_{BUF}	Time between stop condition and next start condition		1300		ns
t_W	t_{WR}	Write time			5	ms
t_{NS}		Pulse width ignored (input filter on SCL and SDA for serial EEPROM)	Single glitch		200	ns

1. Sampled only, not 100% tested.
2. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA
3. For a reSTART condition, or following a Write cycle.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

Figure 7. SOX18 – 18-lead plastic small outline, 300mils, embedded crystal

1. Drawing is not to scale.

Table 9. SOX18 – 18-lead plastic small outline, 300mils, embedded crystal, package mech.

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.44	2.69		0.096	0.106
A1		0.15	0.31		0.006	0.012
A2		2.29	2.39		0.090	0.094
B		0.41	0.51		0.016	0.020
C		0.20	0.31		0.008	0.012
D	11.61	11.56	11.66	0.457	0.455	0.459
ddd			0.10			0.004
E		7.57	7.67		0.298	0.302
e	1.27	–	–	0.050	–	–
H		10.16	10.52		0.400	0.414
L		0.51	0.81		0.020	0.032
a		0°	8°		0°	8°
N		18			18	

8 Order codes

Table 10. Ordering information scheme

Example: M41T 00S C64 MY 6 E

Device type

M41T = Serial RTC

Supply voltage and write protect voltage

00S = V_{CC} = 2.7 to 5.5V

EEPROM density

C64 = 64 Kbit (8192 bit x 8)

Package

MY⁽¹⁾ = SOX18

Temperature range

6 = -40°C to 85°C

Shipping method

E = Lead-free package ECOPACK®, tubes

F = Lead-free package ECOPACK®, tape & reel

1. The SOX18 package includes an embedded 32,768Hz crystal.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

9 Revision history

Table 11. Revision history

Date	Version	Description
20-Jul-2006	1	First Edition
25-Sep-2006	2	Added information on EEPROM density and ECOPACK® packages in Table 10: Ordering information scheme
30-Jan-2007	3	Updates in DC and AC parameters (Table 4 and Table 6).

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