



ALPHA & OMEGA
SEMICONDUCTOR



AOD4189

P-Channel Enhancement Mode Field Effect Transistor

General Description

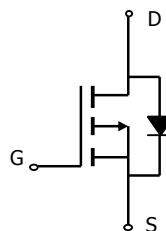
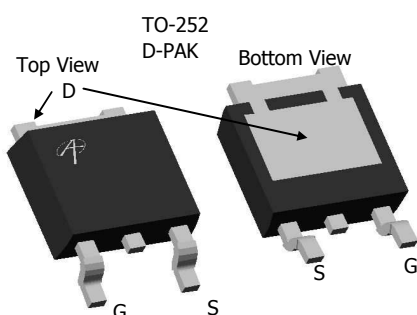
The AOD4189 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

- RoHS Compliant
- Halogen Free*

Features

V_{DS} (V) = -40V
 I_D = -40A (V_{GS} = -10V)
 $R_{DS(ON)} < 22m\Omega$ (V_{GS} = -10V)
 $R_{DS(ON)} < 29m\Omega$ (V_{GS} = -4.5V)

100% UIS Tested!
100% Rg Tested!



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{B,H}	I_D	-40	A
$T_C=25^\circ\text{C}$		-28	
$T_C=100^\circ\text{C}$	I_{DM}	-50	
Pulsed Drain Current ^C	I_{AR}	-35	
Avalanche Current ^C	E_{AR}	61	mJ
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	P_D	62.5	W
$T_C=25^\circ\text{C}$		31	
Power Dissipation ^B	P_{DSM}	2.5	
$T_A=25^\circ\text{C}$		1.6	
Power Dissipation ^A	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Junction and Storage Temperature Range			

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
$t \leq 10\text{s}$		41	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JC}$	2	2.4	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case ^{D,F}				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1.7	-1.9	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-50			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-12A T _J =125°C		18 27	22 33	mΩ
		V _{GS} =-4.5V, I _D =-8A		23	29	
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-12A		35		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.74	-1	V
I _S	Maximum Body-Diode Continuous Current				-20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, f=1MHz		1870		pF
C _{oss}	Output Capacitance			185		pF
C _{rss}	Reverse Transfer Capacitance			155		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	2.5	4.5	6.5	Ω
SWITCHING PARAMETERS						
Q _g (-10V)	Total Gate Charge	V _{GS} =-10V, V _{DS} =-20V, I _D =-12A		31.4	41	nC
Q _g (-4.5V)	Total Gate Charge			7.9	10	
Q _{gs}	Gate Source Charge			7.6		nC
Q _{gd}	Gate Drain Charge			6.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-20V, R _L =1.6Ω, R _{GEN} =3Ω		10		ns
t _r	Turn-On Rise Time			18		ns
t _{D(off)}	Turn-Off DelayTime			38		ns
t _f	Turn-Off Fall Time			24		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-12A, dI/dt=100A/μs		32	42	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-12A, dI/dt=100A/μs		30		nC

A: The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on T_{J(MAX)}=150°C, using steady state junction-to-ambient thermal resistance.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using t ≤ 300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H: The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1: Oct 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

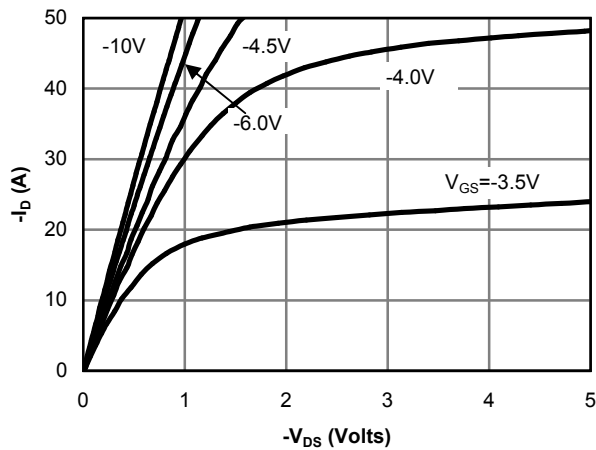


Figure 1: On-Region Characteristics

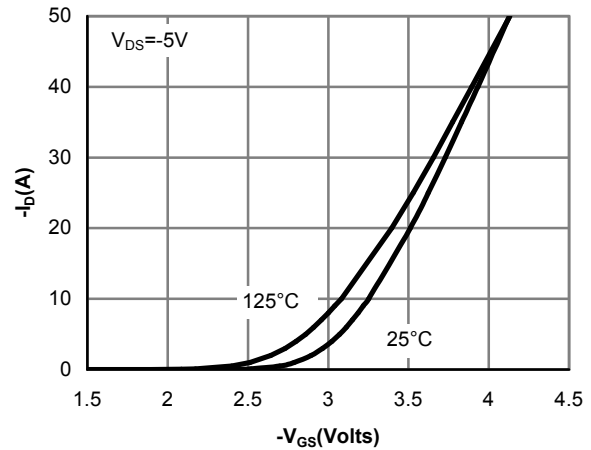


Figure 2: Transfer Characteristics

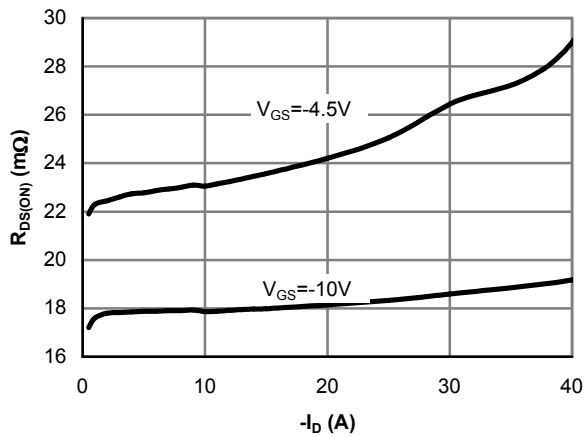


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

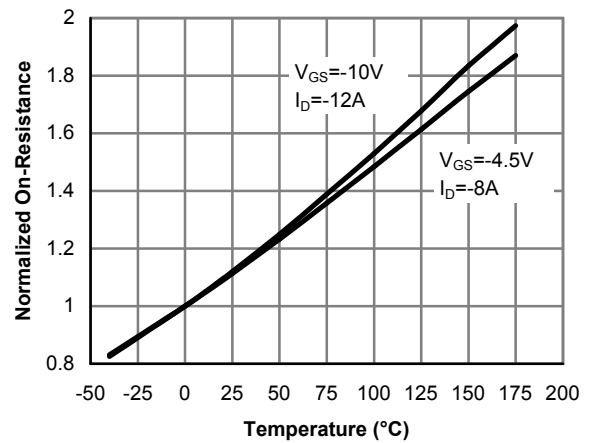


Figure 4: On-Resistance vs. Junction Temperature

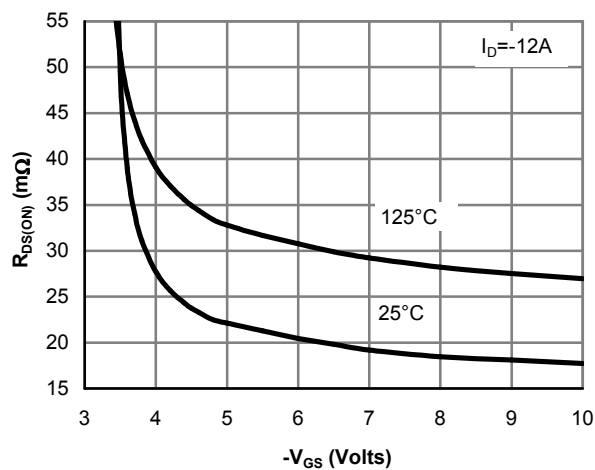


Figure 5: On-Resistance vs. Gate-Source Voltage

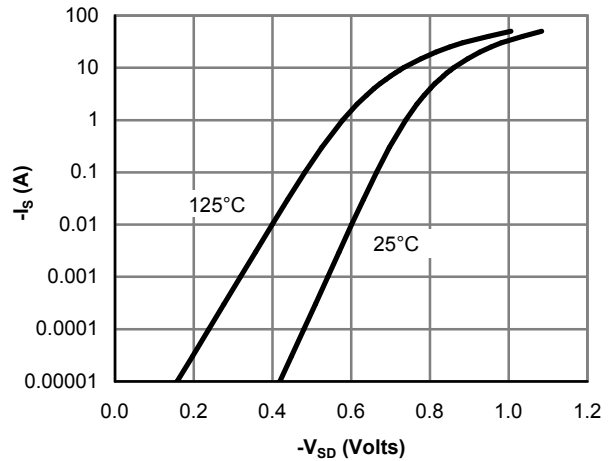


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

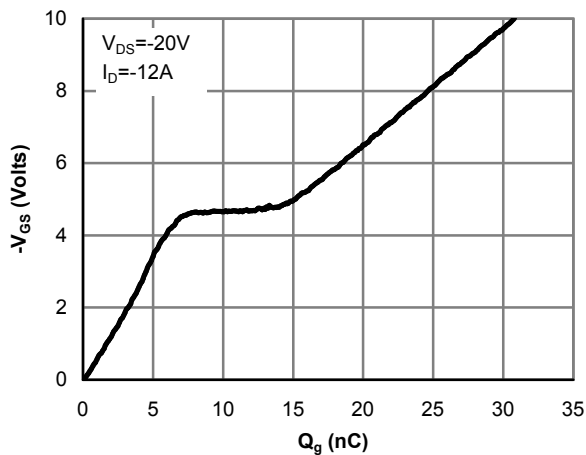


Figure 7: Gate-Charge Characteristics

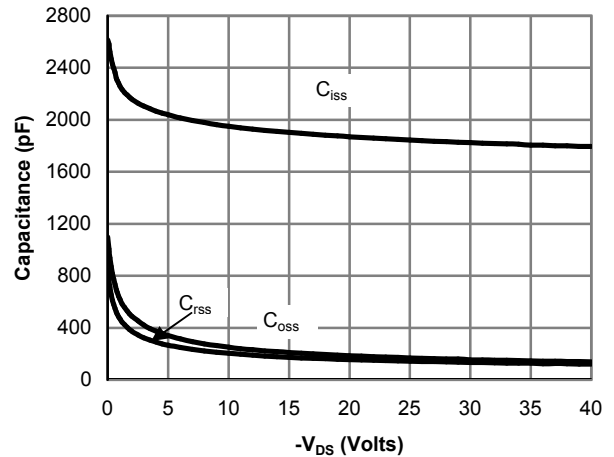


Figure 8: Capacitance Characteristics

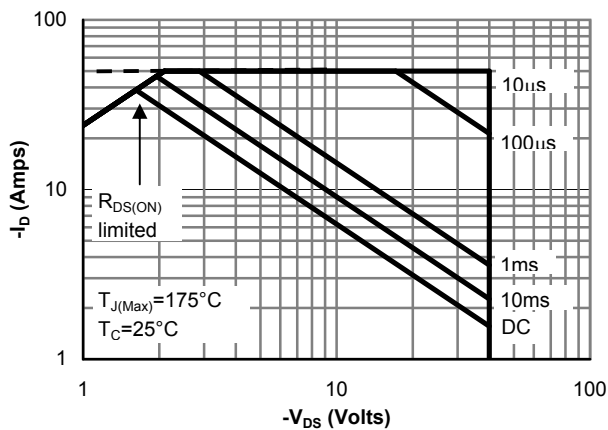


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

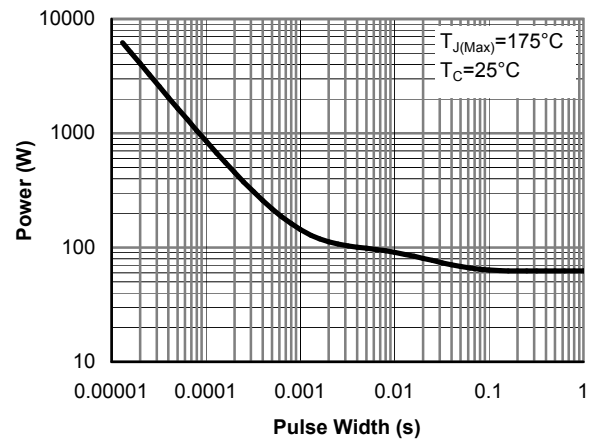


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

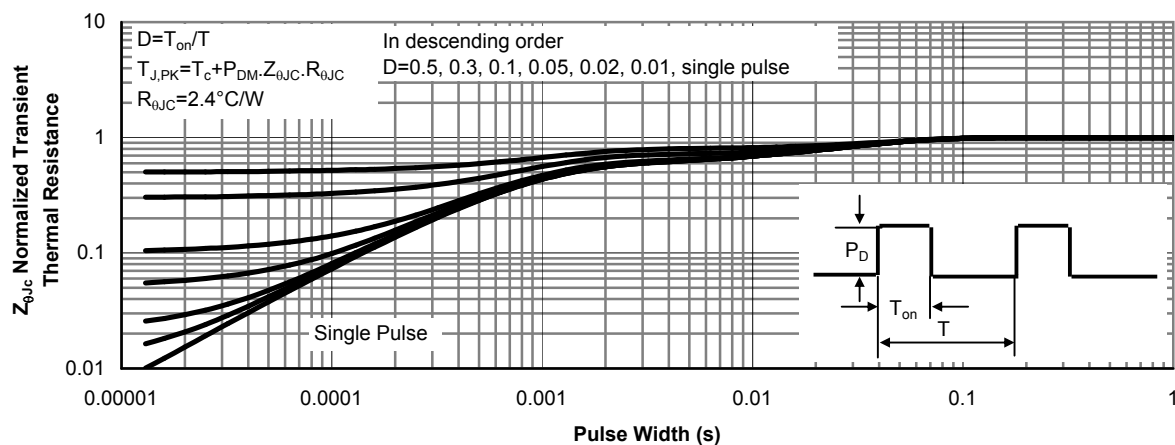


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

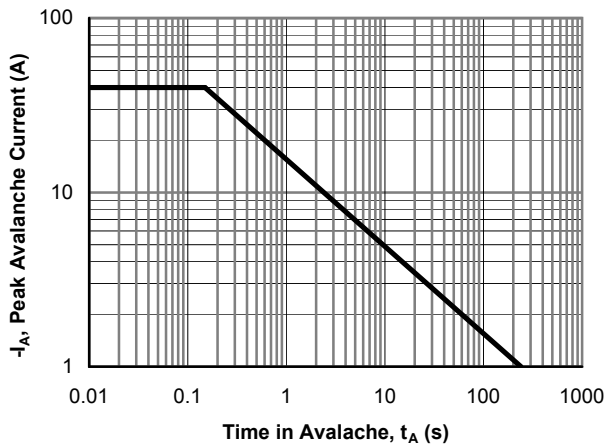


Figure 12: Single Pulse Avalanche Capability

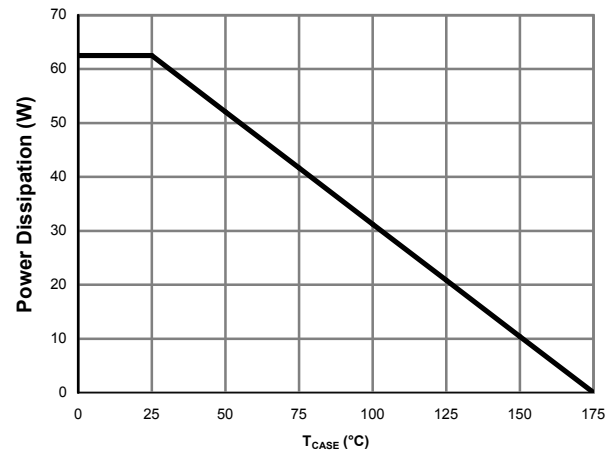


Figure 13: Power De-rating (Note B)

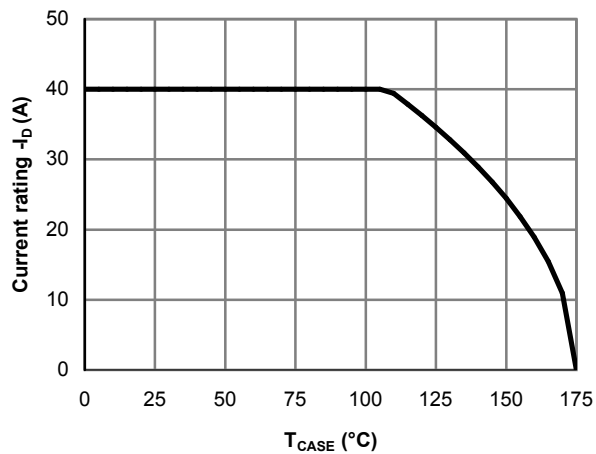


Figure 14: Current De-rating (Note B)

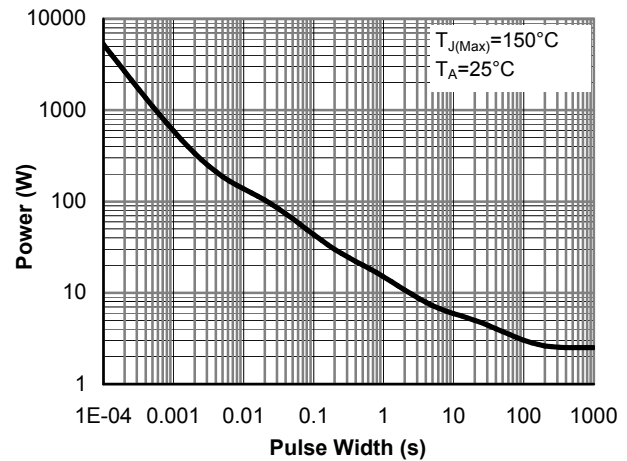


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

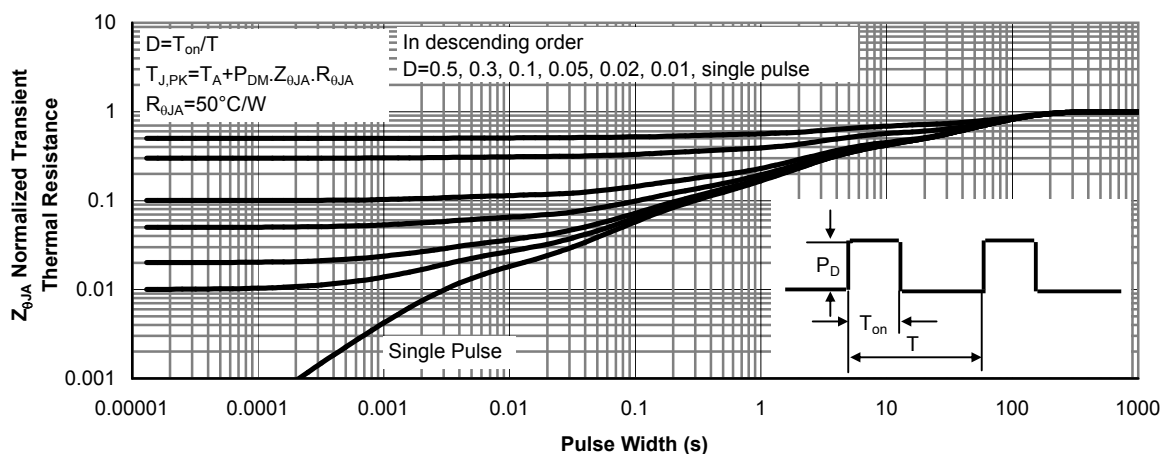
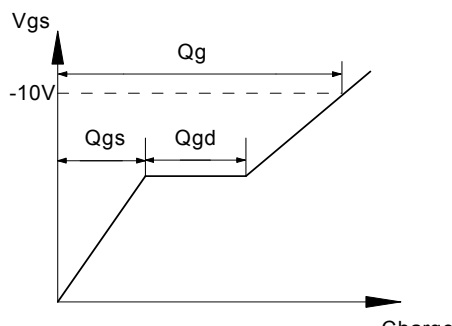
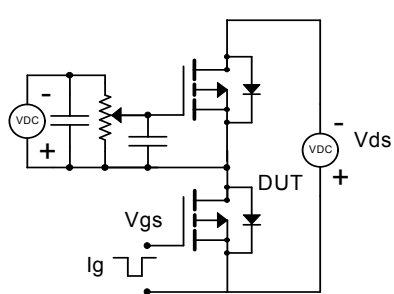
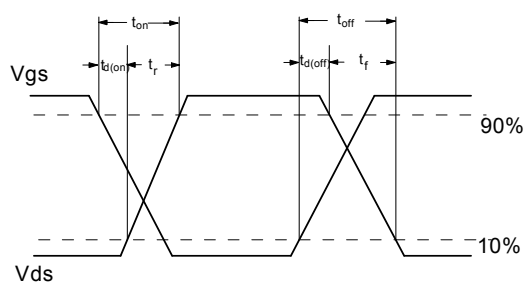
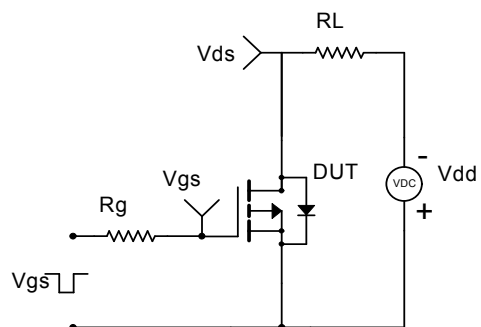


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

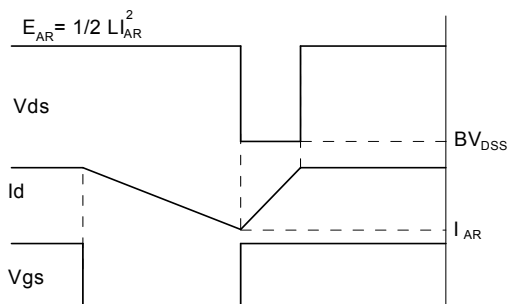
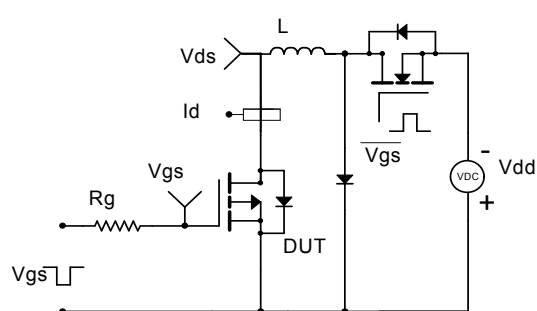
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

