TC74HC74P DUAL D FLIP FLOP WITH PRESET AND CLEAR

The TC74HC74 is a high speed CMOS DUAL D FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

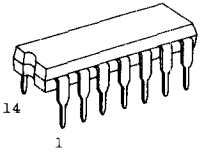
Signal given D INPUT is transferred to Q OUTPUT during the positive going transition of the clock pulse.

CLEAR and PRESENT are independent of the clock and accomplished by "L" level at the appropriate input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=40MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS74



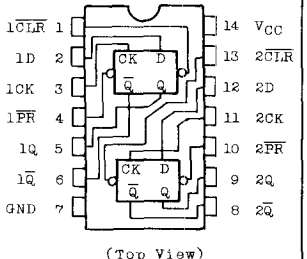
DIP (5-21F)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	*	*	L	H	CLEAR
H	L	*	*	H	L	PRESET
L	L	*	*	H	H	-
H	H	L	↓	L	H	-
H	H	H	↓	H	L	-
H	H	*	↑	Qn	$\overline{Qn}$	NO CHANGE

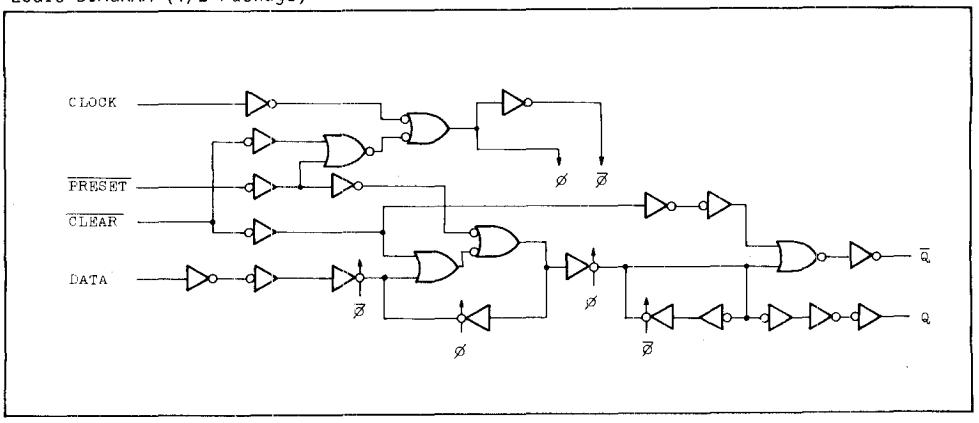
* Don't care

PIN ASSIGNMENT



(Top View)

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

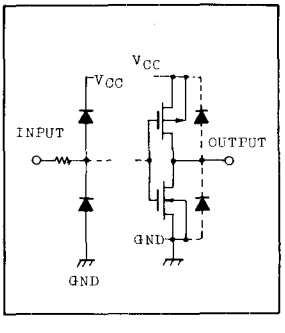
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.32	-	0.37	
			I_{OL}=5.2mA	6.0	-	0.18	0.32	-	0.37	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

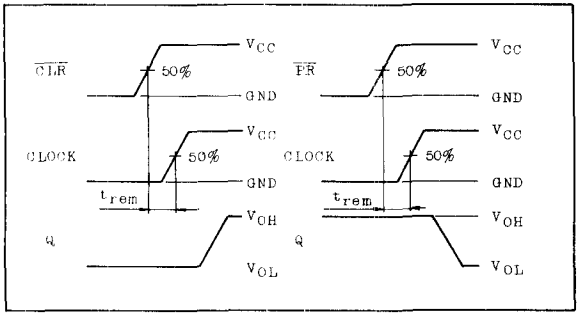
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	90	ns
			4.5	-	8	15	-	18	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	80	160	-	195	ns
			4.5	-	21	32	-	39	
			6.0	-	18	28	-	34	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	105	210	-	250	ns
			4.5	-	27	41	-	50	
			6.0	-	23	35	-	43	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

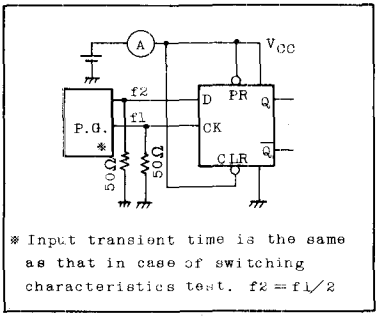
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	5	8	-	4	-	MHz
			4.5	25	40	-	20	-	
			6.0	29	45	-	23	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	35	75	-	90	ns
			4.5	-	8	15	-	18	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time	t_s		2.0	-	45	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	50	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	53	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per FF)

SWITCHING CHARACTERISTICS TEST WAVEFORM

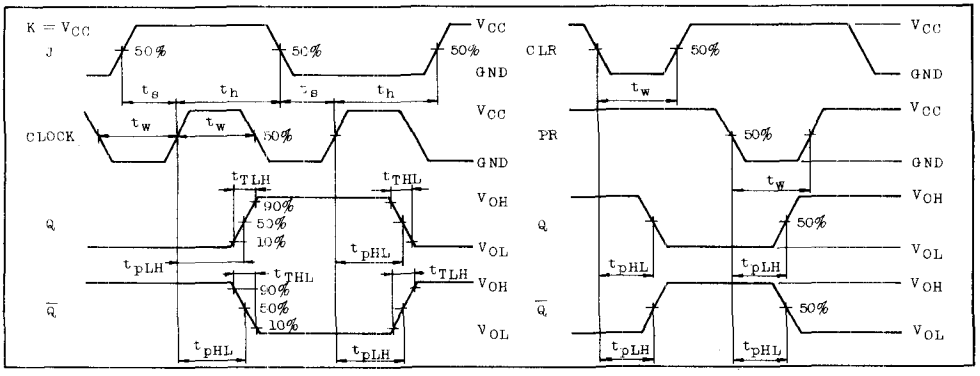


$I_{CC(opr)}$ TEST CIRCUIT

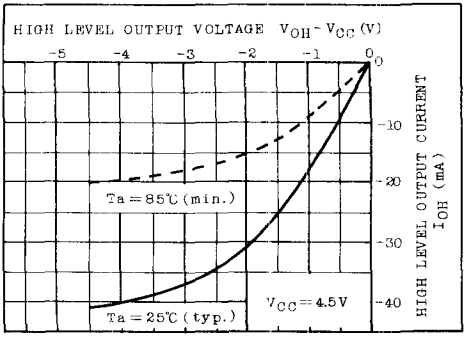


* Input transient time is the same as that in case of switching characteristics test. f2 = f1/2

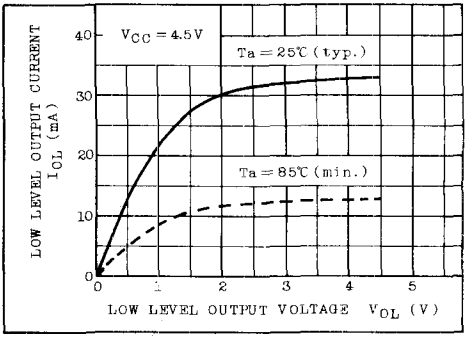
SWITCHING CHARACTERISTICS TEST WAVEFORM



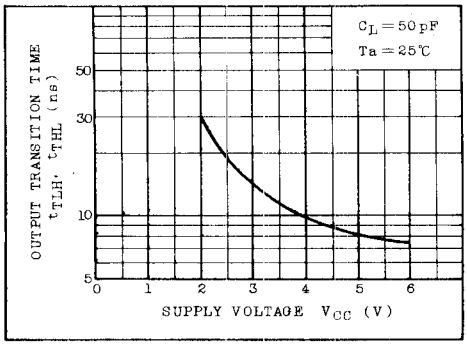
I_{OH} CHARACTERISTICS



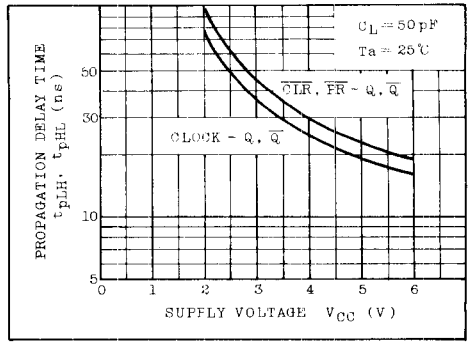
I_{OL} CHARACTERISTICS



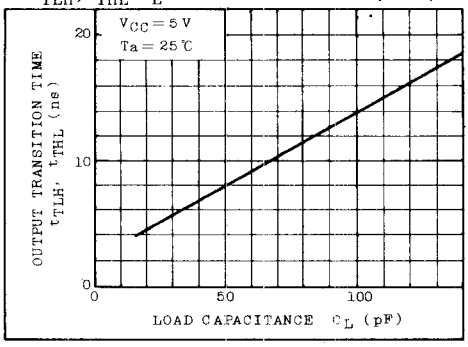
t_{TLH}, t_{THL}-V_{CC} CHARACTERISTICS (TYP.)



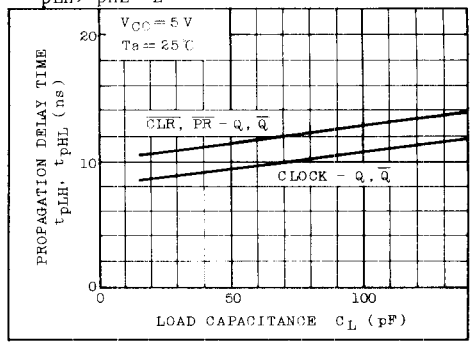
t_{pLH}, t_{pHL}-V_{CC} CHARACTERISTICS (TYP.)



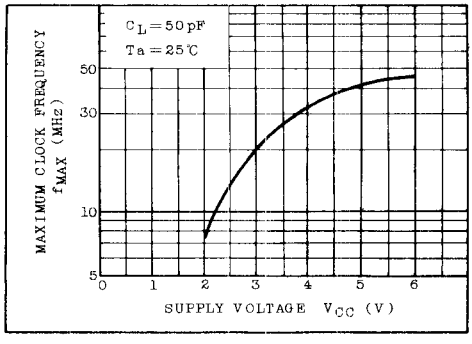
t_{TLH}, t_{THL}-C_L CHARACTERISTICS (TYP.)



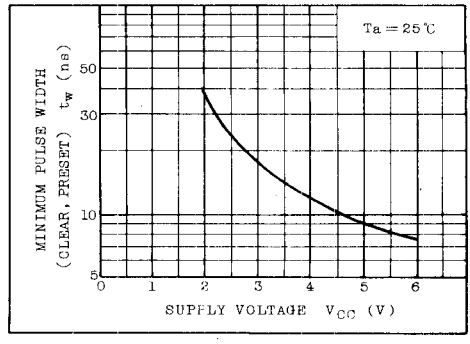
t_{pLH}, t_{pHL}-C_L CHARACTERISTICS (TYP.)



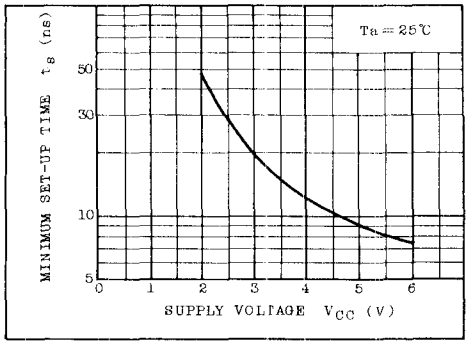
f_{MAX}-V_{CC} CHARACTERISTICS (TYP.)



$t_w(\overline{CL}, \overline{PR})$-$V_{CC}$ CHARACTERISTICS (TYP.)



t_s-V_{CC} CHARACTERISTICS (TYP.)



$t_{rem}(\overline{CL},\overline{PR})$-$V_{CC}$ CHARACTERISTICS (TYP.)