



CYPRESS

COMLINK™ SERIES

CY2CC1810

1:10 Clock Fanout Buffer with Output Enable

Features

- Low-voltage operation
- V_{DD} range from 2.5 to 3.3V
- 1:10 fanout
- Drives either a 50-ohm or 75-ohm transmission line
- Over voltage tolerant input hot swappable
- Low input capacitance
- Low output skew
- Low propagation delay
- Typical ($t_{pd} < 4$ ns)
- High-speed operation > 200 MHz
- LVTTL/LVCMOS-compatible input
 - Output disable to three-state
- Industrial versions available
- Packages available include: SOIC/SSOP

Description

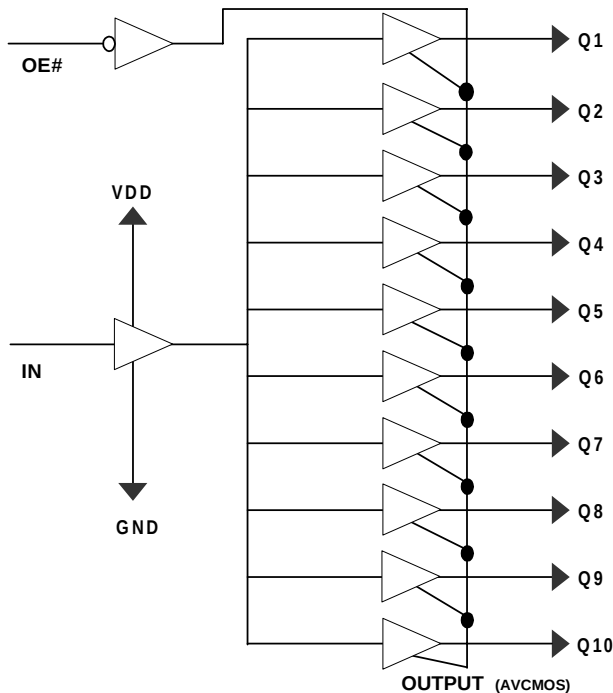
The Cypress series of network circuits is produced using advanced 0.35-micron CMOS technology, achieving the industries fastest logic and buffers.

The Cypress CY2CC1810 fanout buffer features one input and ten three-state outputs.

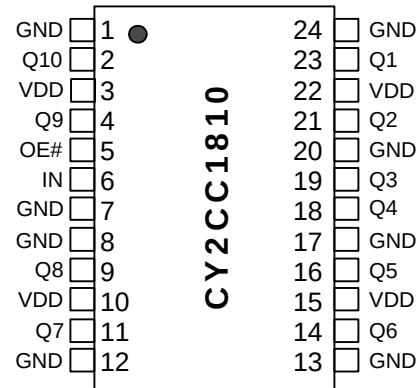
Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

AVCMOS-type outputs dynamically adjust for variable impedance-matching and eliminate the need for series-damping resistors; they also reduce noise overall.

Block Diagram



Pin Configuration



24 pin SOIC/SSOP

Pin Description

Pin Number	Pin Name	Pin Description	
1,7,8,12,13,17,20,24	G_{ND}	Ground	Power
3,10,15,22	V_{DD}	Power Supply	Power
5	OE#	Output Enable	LVTTL/LVCMOS
6	IN	Input	LVTTL/LVCMOS
2,4,9,11,14,16,18,19,21,23	Q10.....Q1	Output	AVCMOS

Maximum Ratings^{[1][2]}

Storage Temperature:	–65°C to + 150°C	Supply Voltage to Ground Potential	
Ambient Temperature:	–40°C to +85°C	(Outputs only)	–0.5V to $V_{DD} + 0.5V$
Supply Voltage to Ground Potential		DC Output Voltage	–0.5V to $V_{DD} + 0.5V$
V_{CC}	–0.5V to 4.6V	Power Dissipation	0.75W
Input	–0.5V to 5.8V		

DC Parameter @ 3.3V $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (see Figure 6)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12 \text{ mA}$	2.3	3.3		V
V_{OL}	Output Low Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12 \text{ mA}$		0.2	0.5	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2		5.8	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max.}$	$V_{IN} = 2.7V$			1	uA
I_{IL}	Input Low Current	$V_{DD} = \text{Max.}$	$V_{IN} = 0.5V$			–1	uA
I_I	Input High Current	$V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max})$				20	uA
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Min.}, I_{IN} = -18 \text{ mA}$			–0.7	–1.2	V
I_{OK}	Continuous Clamp Current	$V_{DD} = \text{Max.}, V_{OUT} = \text{GND}$				–50	mA
O_{OFF}	Power-down Disable	$V_{DD} = \text{GND}, V_{OUT} = < 4.5V$				100	uA
V_H	Input Hysteresis				80		mV

DC Parameter @ 2.5V $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (see Figure 1)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -7 \text{ mA}$	1.8			V
			$I_{OH} = 12 \text{ mA}$	1.6			V
V_{OL}	Output Low Voltage	$V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12 \text{ mA}$			0.65	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		1.6		5.0	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	$V_{DD} = \text{Max.}$	$V_{IN} = 2.4V$			1	uA
I_{IL}	Input Low Current	$V_{DD} = \text{Max.}$	$V_{IN} = 0.5V$			–1	uA
I_I	Input High Current	$V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max.})$				20	uA
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Min.}, I_{IN} = -18 \text{ mA}$			–0.7	–1.2	V
I_{OK}	Continuous Clamp Current	$V_{DD} = \text{Max.}, V_{OUT} = \text{GND}$				–50	mA
O_{OFF}	Power-down Disable	$V_{DD} = \text{GND}, V_{OUT} = < 4.5V$				100	uA
V_H	Input Hysteresis				80		mV

Capacitance

Symbol	Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	2.5		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	6.5		pF

Note:

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Power Supply Characteristics (See Figure 1)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
ΔI_{CC}	Delta I_{CC} Quiescent Power Supply Current	$(I_{DD} @ V_{DD} = \text{Max. and } V_{IN} = V_{DD}) - (I_{DD} @ V_{DD} = \text{Max. and } V_{IN} = V_{DD} - 0.6V)$			50	μA
I_{CCD}	Dynamic Power Supply Current	$V_{DD} = \text{Max.}$ Input toggling 50% Duty Cycle, Outputs Open			0.63	mA/MHz
I_C	Total Power Supply Current	$V_{DD} = \text{Max.}$ Input toggling 50% Duty Cycle, Outputs Open $f_L = 40 \text{ MHz}$			25	mA

High-frequency Parametrics

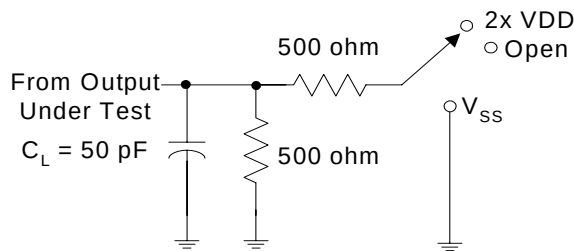
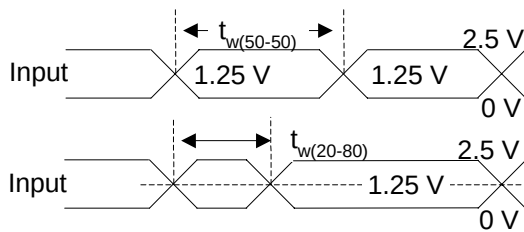
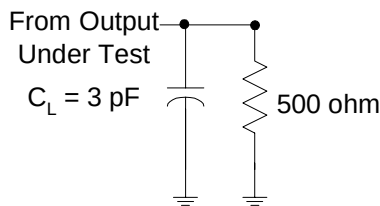
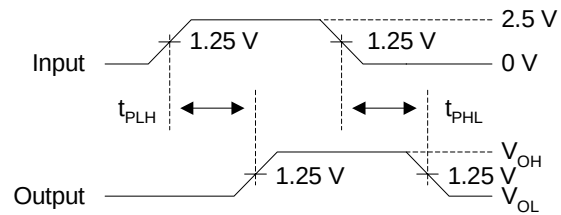
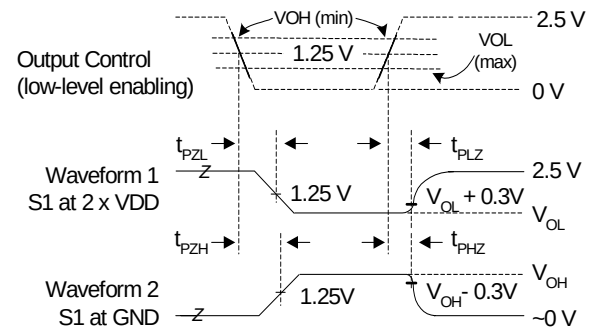
Parameter	Description	Test Conditions	Min.	Typ	Max	Unit
D_J	Jitter, Deterministic	50% duty cycle $t_W(50-50)$ The "point to point load circuit" Output Jitter – Input Jitter			20	ps
F_{max}	Maximum frequency $V_{DD} = 3.3V$	50% duty cycle $t_W(50-50)$ Standard Load Circuit.			160	MHz
		50% duty cycle $t_W(50-50)$ The "point to point load circuit"			200	
$F_{\text{max}(20)}$	Maximum frequency $V_{DD} = 3.3V$	20% duty cycle $t_W(20-80)$ The "point to point load circuit" $V_{IN} = 3.0V/0.0V$ $V_{OUT} = 2.3V/0.4V$			200	MHz
		Maximum frequency $V_{DD} = 2.5V$ The "point to point load circuit" $V_{IN} = 2.4V/0.0V$ $V_{OUT} = 1.7V/0.7V$			100	
t_W	Minimum pulse $V_{DD} = 3.3V$	The "point to point load circuit" $V_{IN} = 3.0V/0.0V$ $F = 100 \text{ MHz}$ $V_{OUT} = 2.0V/0.8V$	2			ns
	Minimum pulse $V_{DD} = 2.5V$	The "point to point load circuit" $V_{IN} = 2.4V/0.0V$ $F = 100 \text{ MHz}$ $V_{OUT} = 1.7V/0.7V$	1			

AC Switching Characteristics @ $3.3V$ $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ (See Figure 6)

Parameter	Description	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	1.5	3	3.9	nS
t_{PHL}	Propagation Delay – High to Low	1.5	3	3.9	nS
t_{PHZ}	Propagation Delay – High to High Z		4		nS
t_{PLZ}	Propagation Delay – Low to High Z		3		nS
t_R	Output Rise Time		0.8		V/nS
t_F	Output Fall Time		0.8		V/nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)			0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)			0.2	nS
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.			0.3	nS
t_{OFF}	Delay from OE to Driver Off			4.0	nS
t_{ON}	Delay from OE to Driver on			4.0	nS

AC Switching Characteristics @ 2.5V $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (See Figure 1)

Parameter	Description		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	See Figure 4	1.5	3.8	3.5	nS
t_{PHL}	Propagation Delay – High to Low		1.5	3.8	3.5	nS
t_{PHZ}	Propagation Delay – High to High Z	See Figure 5		5		nS
t_{PLZ}	Propagation Delay – Low to High Z			4		nS
t_R	Output Rise Time	See Figure 4		0.4		V/nS
t_F	Output Fall Time			0.6		V/nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 12			0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)	See Figure 11			0.2	nS
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 13			0.3	nS
t_{OFF}	Delay from OE to Driver Off				5.0	nS
t_{ON}	Delay from OE to Driver on				5.0	nS

Parameter Measurement Information: V_{DD} @ 2.5V^[3,5,6]

Figure 1. Load Circuit

Figure 2. Voltage Waveforms–Pulse Duration

Figure 3. Point-to-Point Load Circuit

Figure 4. Voltage Waveforms–Propagation Delay Times^[9]

Figure 5. Voltage Waveforms–Enable and Disable Times^[4,7,8]
Table 1.

Test	S1	
t_{PLH}/t_{PHL}	Open	See Figure 4
t_{PLZ}/t_{PZL}	$2 \times V_{DD}$	See Figure 5
t_{PHZ}/t_{PZH}	V_{SS}	

Notes:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz, $Z_o = 50\Omega$, $t_R < 2.5$ nS, $t_F < 2.5$ nS.
- Outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{DIS} .
- t_{PZL} and t_{PZH} are the same as t_{EN} .
- t_{PLH} and t_{PHL} are the same as t_{PD} .

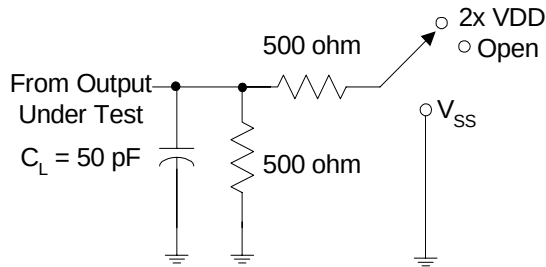
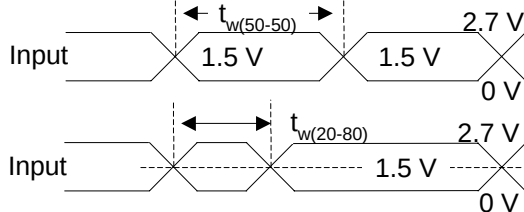
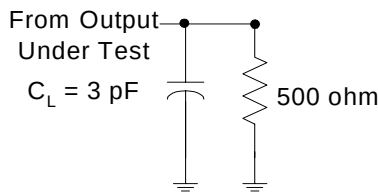
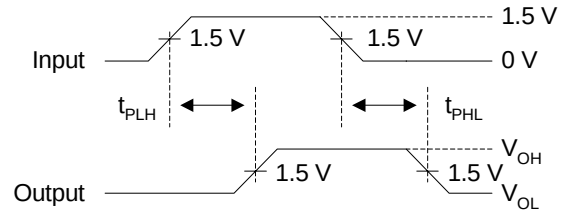
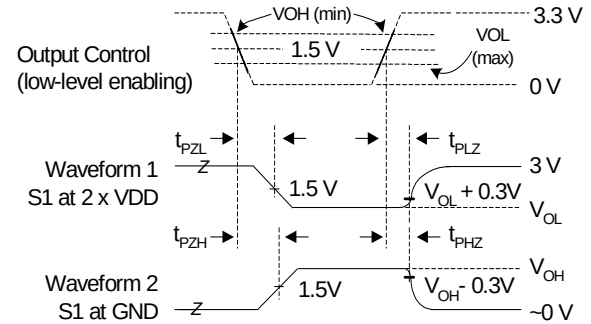
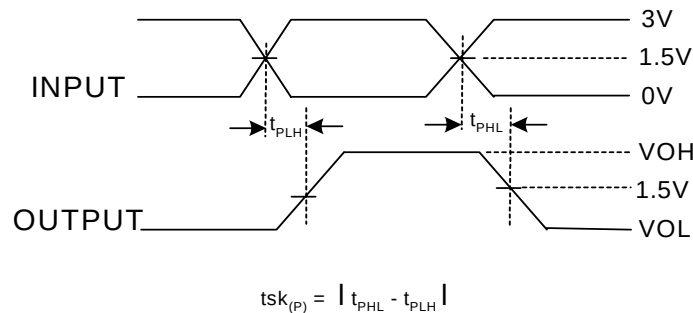
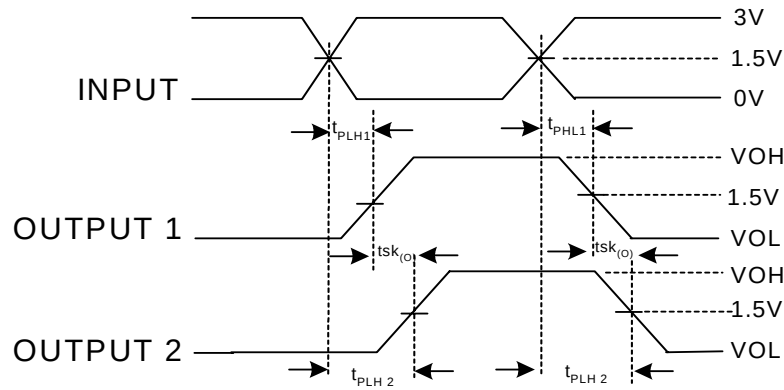
Parameter Measurement Information: V_{DD} @ 3.3V [10,12,13]

Figure 6. Load Circuit

Figure 7. Voltage Waveforms–Pulse Duration

Figure 8. Point-to-Point Load Circuit

Figure 9. Voltage Waveforms–Propagation Delay Times [16]

Figure 10. Voltage Waveforms–Enable and Disable Times [11,14,15]

Table 2.

Test	S1	
t_{PLH}/t_{PHL}	Open	See Figure 9
t_{PLZ}/t_{PZL}	2xVDD	See Figure 10
t_{PHZ}/t_{PZH}	VSS	

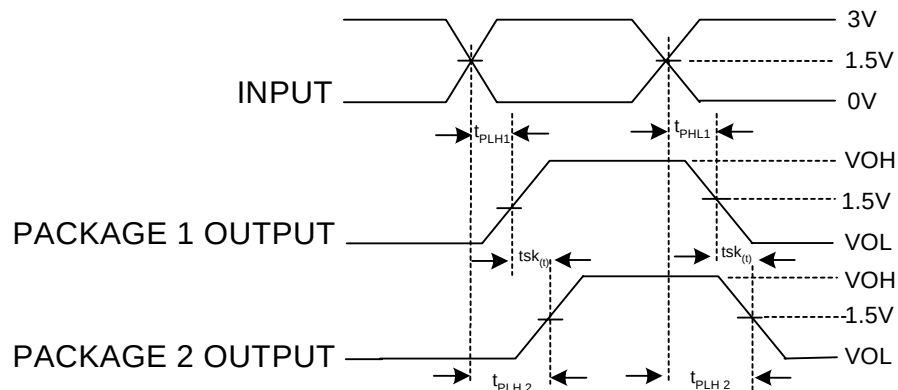

Figure 11. Pulse Skew– $tsk_{(p)}$
Notes:

10. C_L includes probe and jig capacitance
11. Waveform 1 is for an output with internal conditions such that the output is LOW, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH, except when disabled by the output control.
12. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz, $Z_o = 50\Omega$, $t_R < 2.5$ nS, $t_F < 2.5$ nS.
13. The outputs are measured one at a time with one transition per measurement.
14. t_{PLZ} and t_{PHZ} are the same as t_{DIS} .
15. t_{PZL} and t_{PZH} are the same as t_{EN} .
16. t_{PLH} and t_{PHL} are the same as t_{PD} .



$$tsk_{(P)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Figure 12. Output Skew- tsk_o



$$tsk_{(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

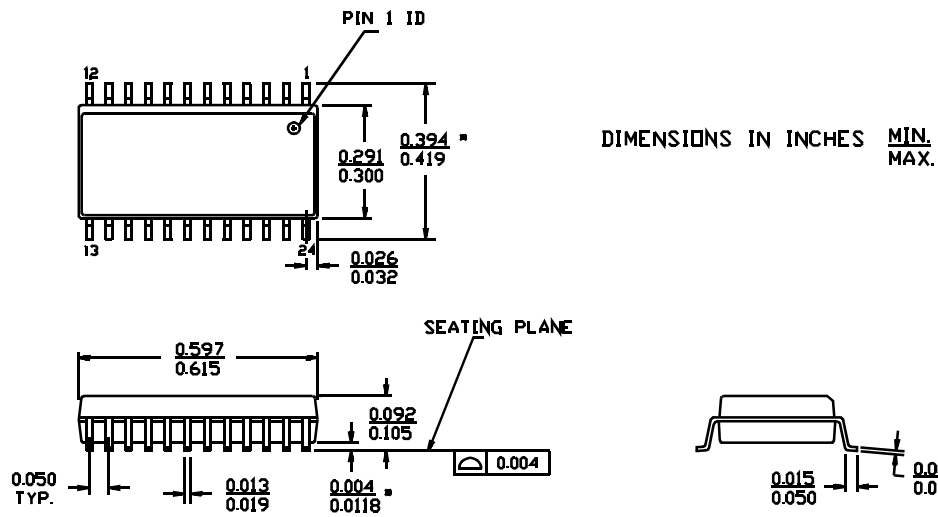
Figure 13. Package Skew - tsk_t

Ordering Information

Part Number	Package Type	Product Flow
CY2CC1810SI	24-pin SOIC	Industrial, -40° to 85°C
CY2CC1810SIT	24-pin SOIC-Tape and Reel	Industrial, -40° to 85°C
CY2CC1810OI	24-pin SSOP	Industrial, -40° to 85°C
CY2CC1810OIT	24-pin SSOP-Tape and Reel	Industrial, -40° to 85°C
CY2CC1810SC	24-pin SOIC	Commercial, 0°C to 70°C
CY2CC1810SCT	24-pin SOIC-Tape and Reel	Commercial, 0°C to 70°C
CY2CC1810OC	24-pin SSOP	Commercial, 0°C to 70°C
CY2CC1810OCT	24-pin SSOP-Tape and Reel	Commercial, 0°C to 70°C

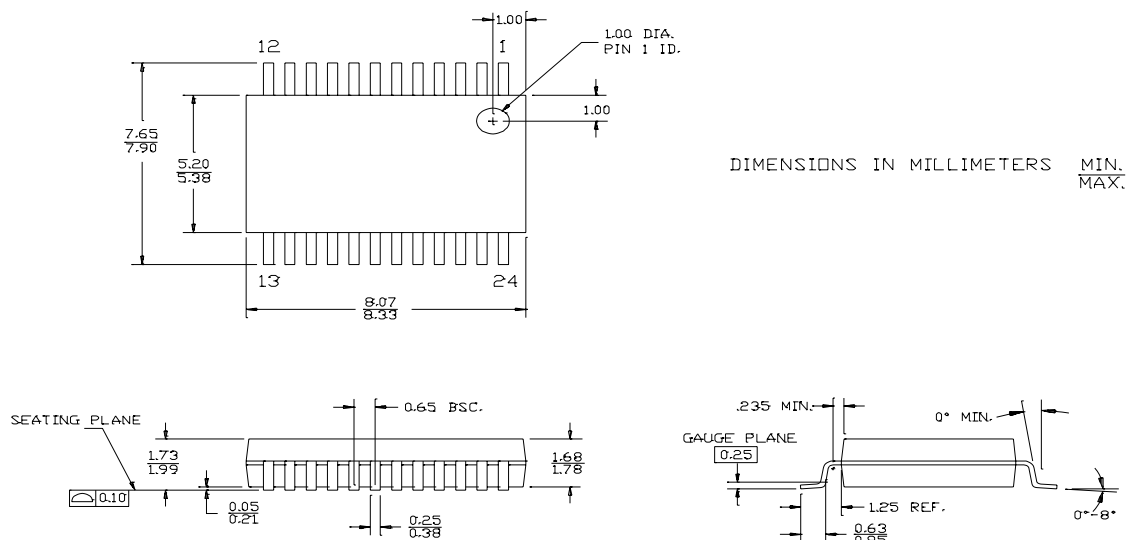
Package Drawing and Dimensions

24-lead (300-mil) Molded SOIC S13



51-85025-A

24-lead (5.3-mm) Shrunk Small Outline Package O24



51-85078-**

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Document History Page

Document Title: CY2CC1810 1:10 Clock Fanout Buffer with Output Enable Document #: 38-07055				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107080	06/07/01	IKA	Convert from IMI to Cypress format
*A	114316	05/08/02	TSM	ΔI_{DD} validation
*B	119147	10/07/02	RGL	Added 5.8 as the Max. value for VIH in the DC Parameters @3.3V table. Changed the Max. value of the VIH from 5.8 to 5.0 in the DC Parameters @2.5V table.
*C	122742	12/14/02	RBI	Added power up requirements to maximum ratings information.