CY7C1019CV33

1-Mbit (128 K × 8) Static RAM

Features

- Temperature Ranges
  - Industrial: –40 °C to 85 °C
  - Automotive-A: –40 °C to 85 °C
- Pin and Function compatible with CY7C1019BV33
- High Speed
  - t_{AA} = 10 ns
- CMOS for optimum Speed and Power
- Data Retention at 2.0 V
- Center Power/Ground Pinout
- Automatic Power Down when deselected
- Easy Memory Expansion with $\overline{CE}$ and $\overline{OE}$ Options
- Available in Pb-free 32-pin TSOP II package

Functional Description

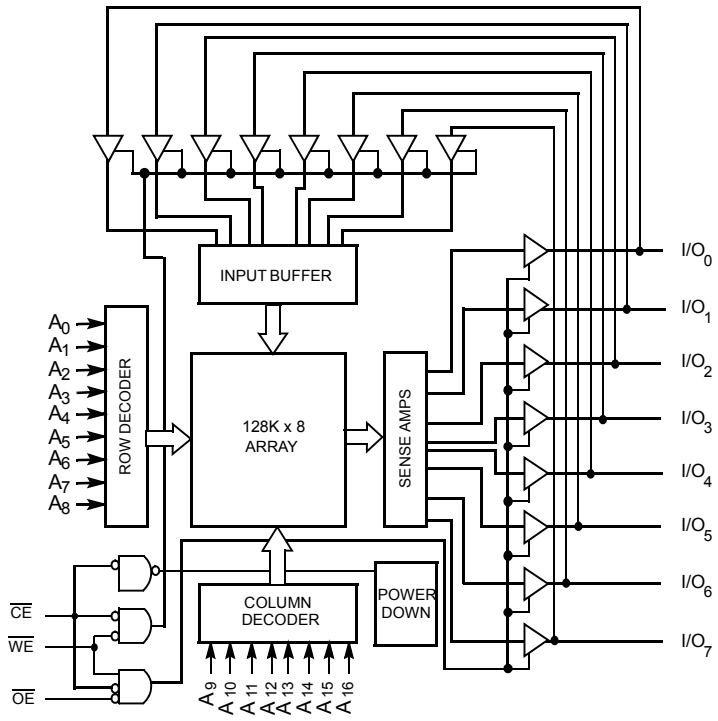
The CY7C1019CV33 is a high performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tristate drivers. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Logic Block Diagram



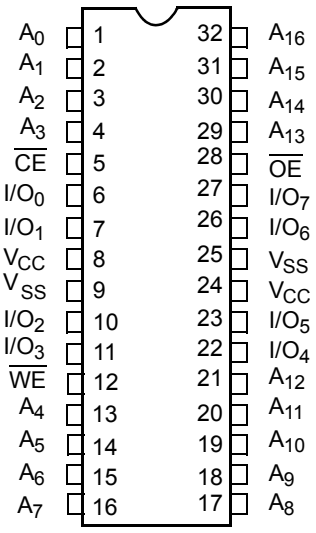
Contents

Selection Guide

Description	-10 (Industrial/ Automotive-A)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum Standby Current	5	mA

Pin Configuration

Figure 1. 32-pin TSOP II pinout (Top View) [1]



Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND [2] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [2] .....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] .....–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....>2001 V

Latch up Current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%
Industrial	–40 °C to +85 °C	3.3 V ± 10%
Automotive-A	–40 °C to +85 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial/Auto-A)		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]		–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	–	80	mA
I_{SB1}	Automatic CE Power down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	15	mA
I_{SB2}	Automatic CE Power down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	5	mA

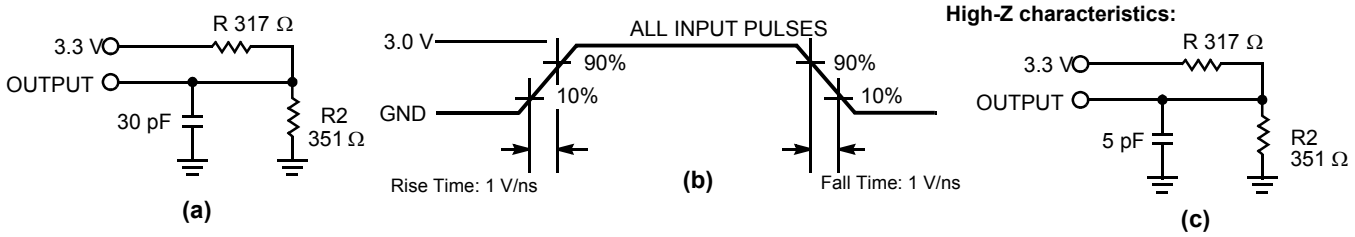
Capacitance

Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	pF

Notes
2. V_{IL} (min.) = –2.0 V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



Note

4. AC characteristics (except High Z) for all speeds are tested using the Thevenin load shown in section (a) in Figure 2. High Z characteristics are tested for all speeds using the test load shown in section (c) in Figure 2.

Switching Characteristics

Over the Operating Range

Parameter [5]	Description	-10 (Industrial/ Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	10	–	ns
t_{AA}	Address to Data Valid	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]	–	5	ns
t_{PU}[8]	$\overline{CE}$ LOW to Power Up	0	–	ns
t_{PD}[8]	$\overline{CE}$ HIGH to Power Down	–	10	ns
Write Cycle[9, 10]				
t_{WC}	Write Cycle Time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8	–	ns
t_{AW}	Address Setup to Write End	8	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	–	ns
t_{SD}	Data Setup to Write End	5	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]	–	5	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 2 on page 5. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. This parameter is guaranteed by design and is not tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 3. Read Cycle No. 1 [11, 12]

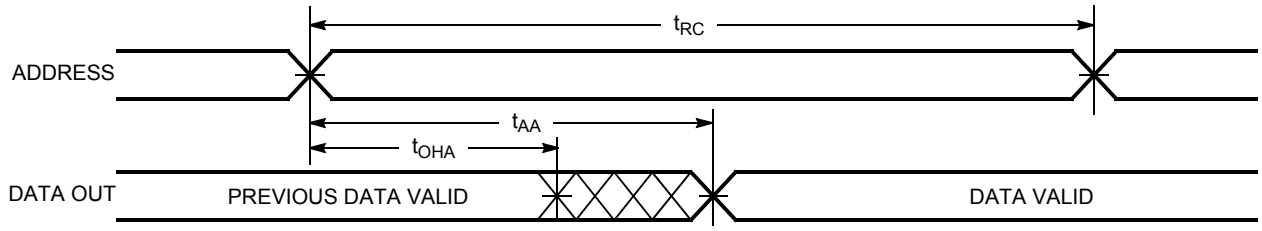


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]

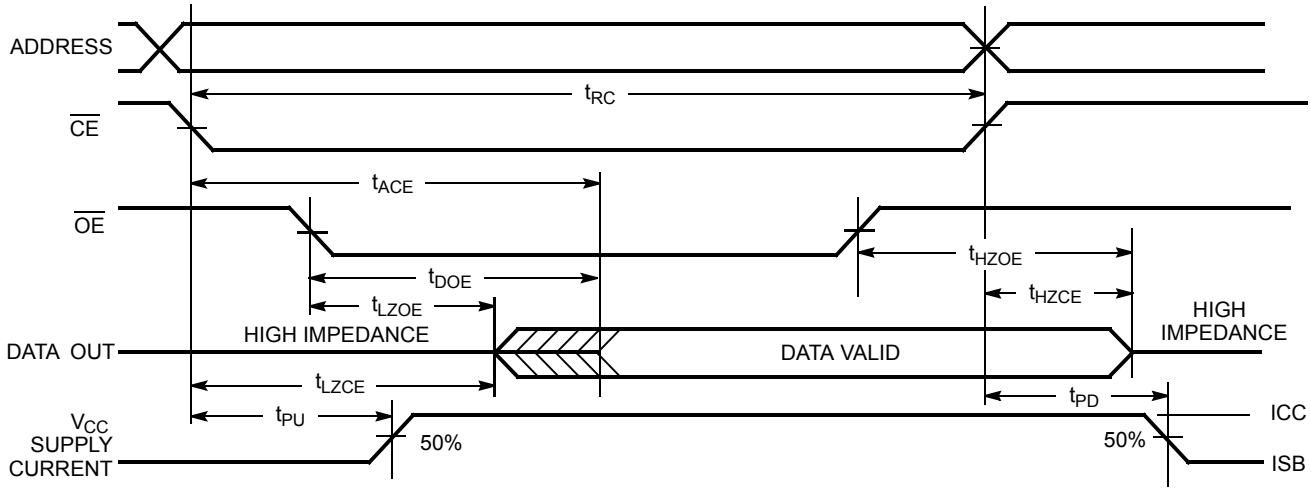
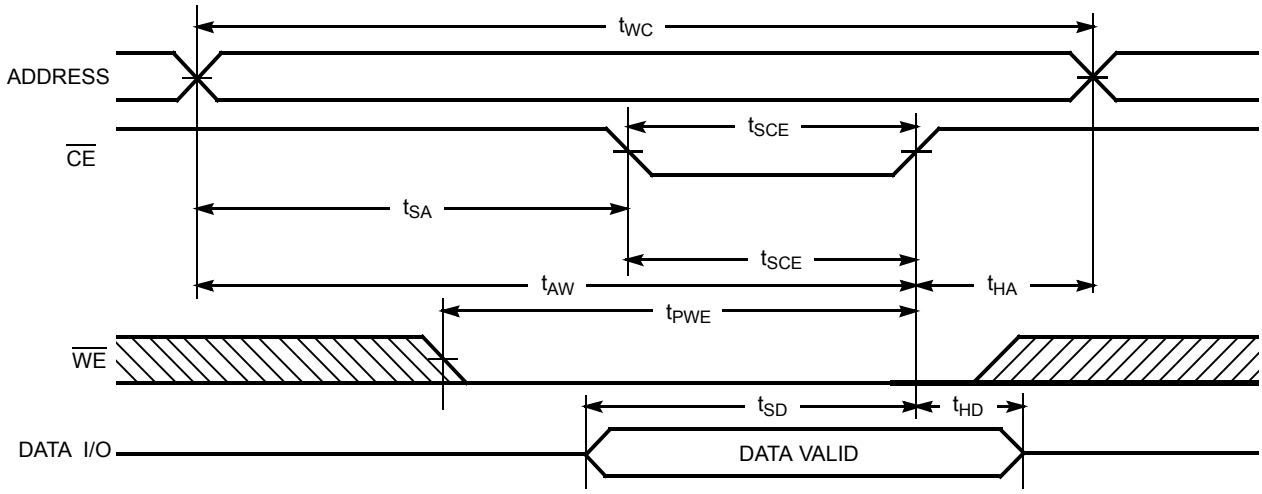


Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]



Notes
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [16, 17]

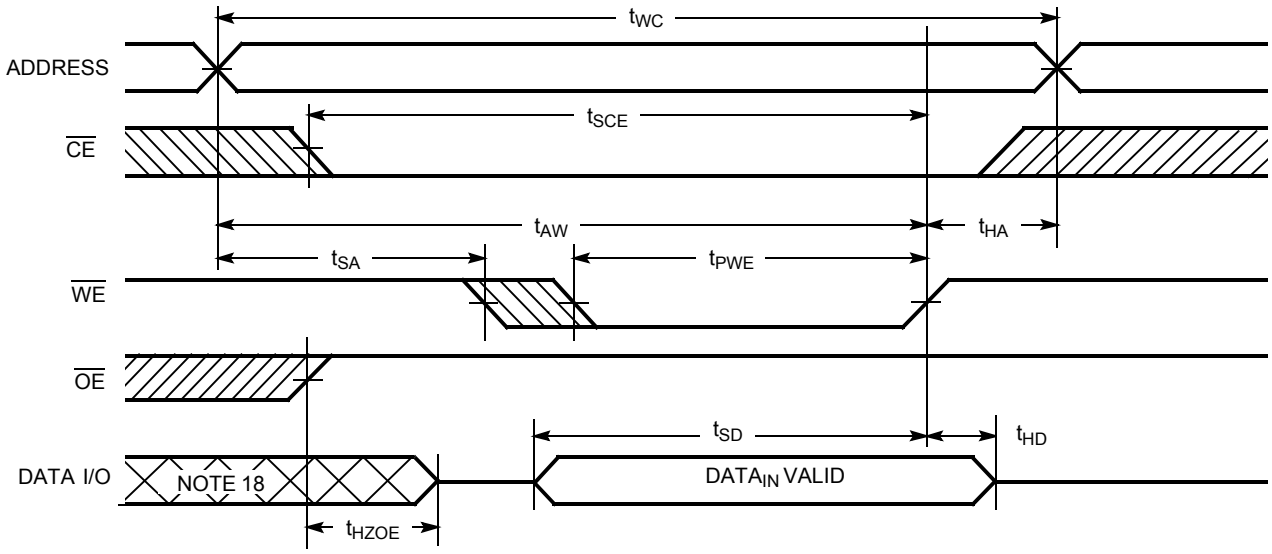
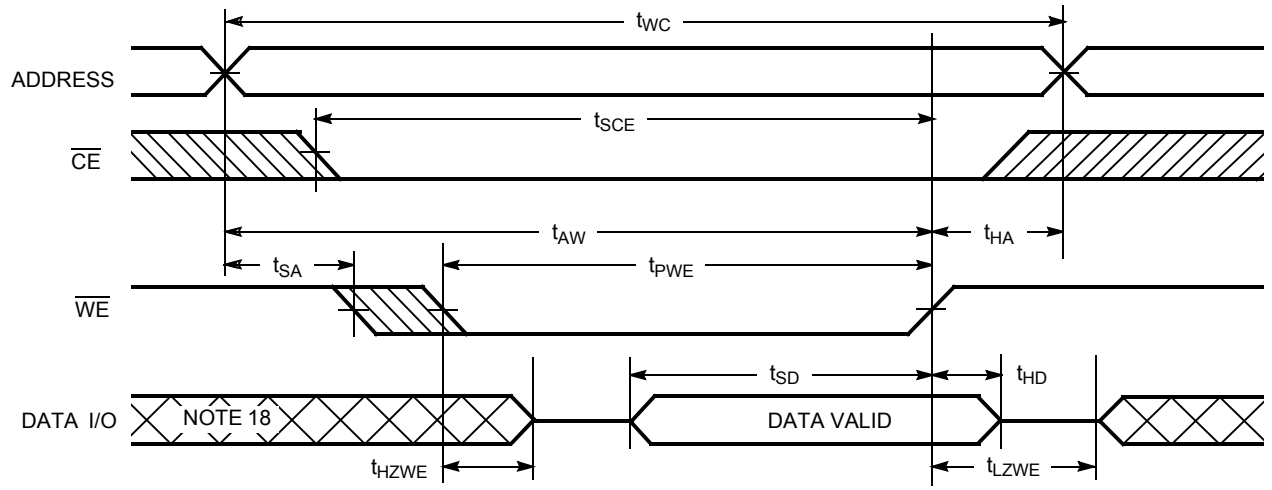


Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17]



Notes
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
18. During this period the I/Os are in the output state and input signals should not be applied.

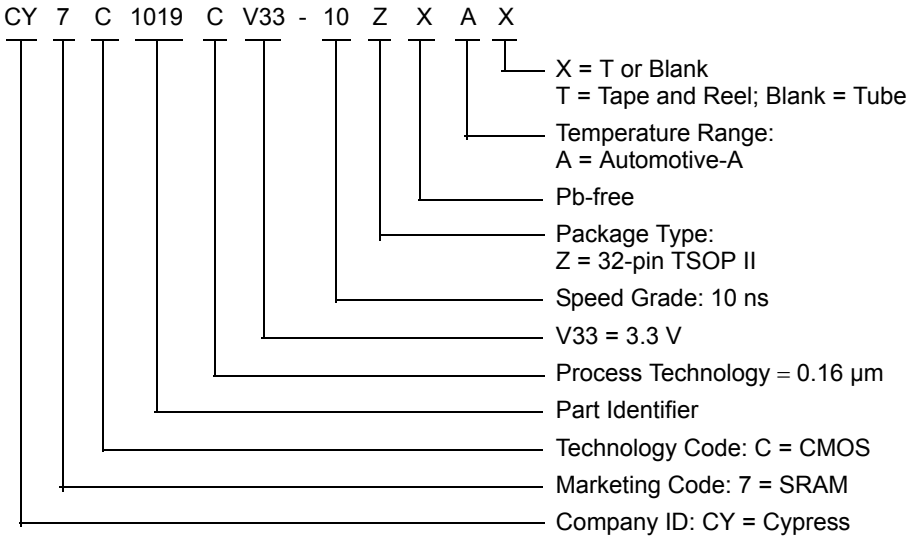
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

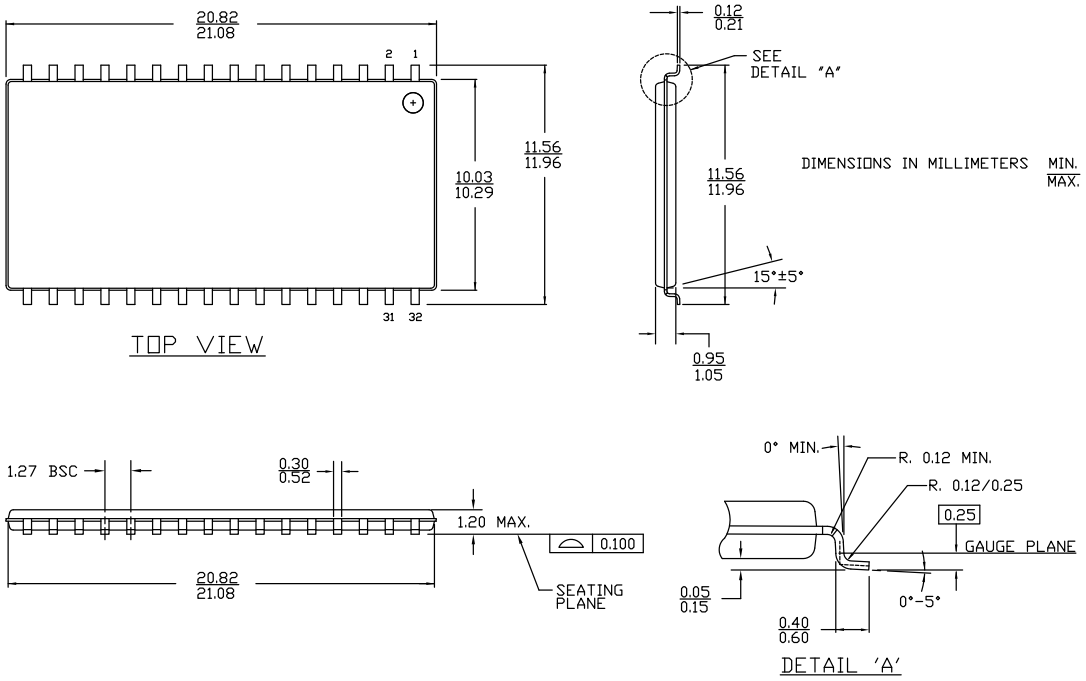
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1019CV33-10ZXA	51-85095	32-pin TSOP II (Pb-free)	Automotive-A
	CY7C1019CV33-10ZXAT	51-85095	32-pin TSOP II (Pb-free)	

Ordering Code Definitions



Package Diagram

Figure 8. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1019CV33, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05130				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	109245	12/16/01	HGK	New data sheet.
*A	113431	04/10/02	NSL	AC Test Loads split based on speed
*B	115047	08/01/02	HGK	Added TSOP II Package and I Temp. Improved I_{CC} limits
*C	119796	10/11/02	DFP	Updated standby current from 5 nA to 5 mA
*D	123030	12/17/02	DFP	Updated Truth Table to reflect single Chip Enable option
*E	419983	See ECN	NXR	Added 48-ball VFBGA Package Added lead-free parts in Ordering Information Table Replaced Package Name column with Package Diagram in the Ordering Information Table
*F	493543	See ECN	NXR	Removed 8 ns speed bin from Product offering Added note #1 on page #2 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information
*G	2761448	09/09/2009	VKN	Included Automotive-A information
*H	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagrams
*I	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions. Updated Package Diagram.
*J	3072834	11/11/2010	PRAS	Removed obsolete parts and package diagrams.
*K	3277371	06/08/2011	AJU	Updated Features. Updated Selection Guide (Removed -12 (Industrial) and -15 (Industrial) columns). Updated Electrical Characteristics (Removed -12 (Industrial) and -15 (Industrial) columns). Updated Switching Characteristics (Removed -12 (Industrial) and -15 (Industrial) columns). Updated Package Diagram. Updated in new template.
*L	4146968	10/04/2013	VINI	Updated in new template. Completing Sunset Review.

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