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FAIRCHILD SEMICONDUCTOR®

May, 2024

FAN5904
Multi-Mode Buck Converter for GSM/EDGE, 3G/3.5G and 4G PAs

Features

- 2.7 V to 5.5 V Input Voltage Range
- V_{OUT} Range from 0.40 V to 3.50 V (or V_{IN})
- Single 470 nH Small Form Factor Inductor
- 35 mΩ Integrated Bypass FET
- 100% Duty Cycle for Low Dropout Operation
- Input Under-Voltage Lockout / Thermal Shutdown
- 1.71 mm x 1.71 mm, 16-Bump, 0.4 mm Pitch WLCSP
- **High Power PWM Mode**
  - Up to 95% Efficient Synchronous Operation in High P_{OUT} Conditions
  - Output current up to 2.3 A
  - 10 µs Output Voltage Step Response for Early GSM Tx Power-Loop Settling
  - 3MHz PWM Mode
- **Low Power Auto Mode**
  - Up to 95% Efficient Synchronous Operation at Higher P_{OUT} Conditions
  - Output Current up to 1.2 A
  - 10 µs Output Voltage Step Response for Early Tx Power-Loop Settling
  - 6 MHz PWM Operation at High Power and PFM Operation at Low Power
- **Bypass Mode**
  - Up to 2 A Load Current

Applications

- Dynamic Supply Bias for Polar or Linear GSM/EDGE PAs and 3G/3.5G and 4G PAs
- Dynamic Supply Bias for GSM/EDGE Quad Band Amplifiers for Mobile Handsets and Data Cards

Description

The FAN5904 is a high-efficiency, low-noise, synchronous, step-down, DC-DC converter optimized for powering Radio Frequency (RF) Power Amplifiers (PAs) in handsets and other mobile applications. In High-Power Mode, GSM Tx power is enabled. In Low-Power Mode, up to 3.0 W is supported, enabling up to 29 dBm output power for 3G/3.5G and 4G platforms.

The output voltage may be dynamically adjusted from 0.40 V to 3.50 V, proportional to an analog input voltage VCON ranging from 0.16 V to 1.40 V, optimizing power-added efficiency. Fast transition times of less than 10 µs are achievable, allowing excellent inter-slot settling.

An integrated bypass FET is automatically enabled when the battery voltage and voltage drop across the DC-DC PMOS device are within a set voltage range of the desired output voltage ($V_{OUT} = V_{BAT} - V_{PMOS} - V_{BP_TH}$). This dynamic bypass feature enables the FAN5904 to support heavy load currents under the most stringent VSWR conditions while maintaining high efficiency and superior spectral performance. The bypass FET may also be enabled by providing a VCON voltage nominally greater than or equal to 1.5 V or by driving BPEN high.

The FAN5904 operates in PWM Mode with a 6 MHz switching frequency in Low-Power Mode and at 3 MHz in High-Power Mode, which limits high-frequency spur levels. It uses a single, small form factor inductor of 470 nH. In addition, PFM operation is allowed in Low-Power Mode to improve efficiency at low load currents.

The FAN5904UC00X option allows PFM Mode only when V_{OUT} is less than 1 V, while the FAN5904UC01X permits PFM Mode at higher voltages for applications that can tolerate larger output ripple and that demand optimal low-to-moderate load current efficiency.

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Ordering Information

Part Number	LPM Mode PFM	Output Voltage	Temperature Range	Package	Packing
FAN5904UC00X	V_{OUT} < 1 V	0.4 V to PVIN	-40°C to +85°C	1.71 mm x 1.71 mm, 16-Bump 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	Tape and Reel
FAN5904UC01X	All V_{OUT}				

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Block Diagrams

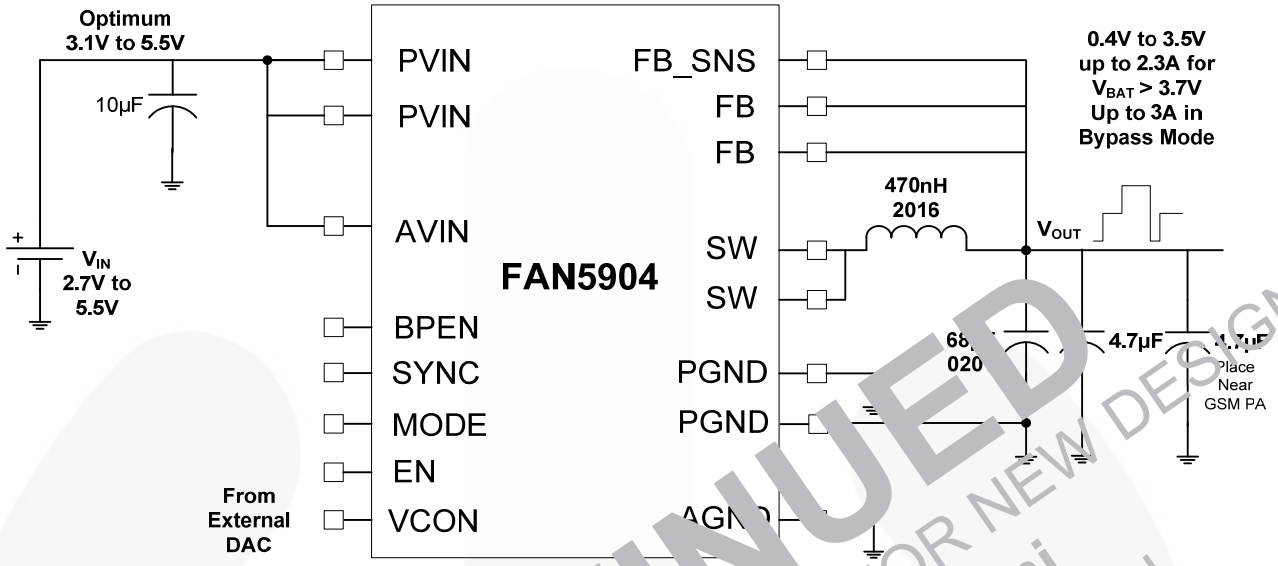

Figure 1. Typical Application

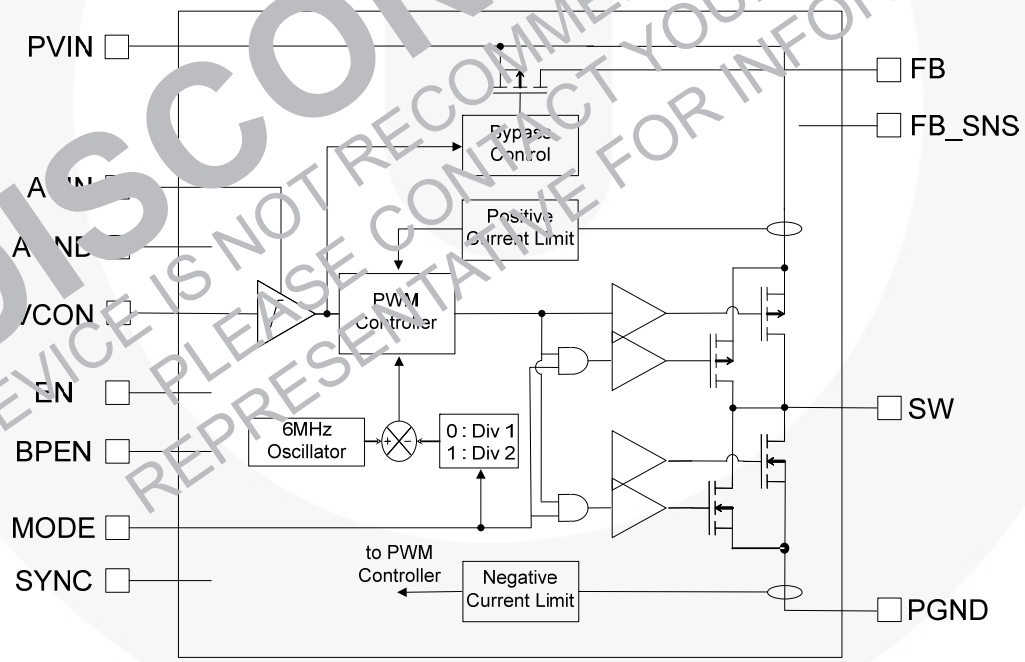

Figure 2. Simplified Block Diagram

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Pin Configuration

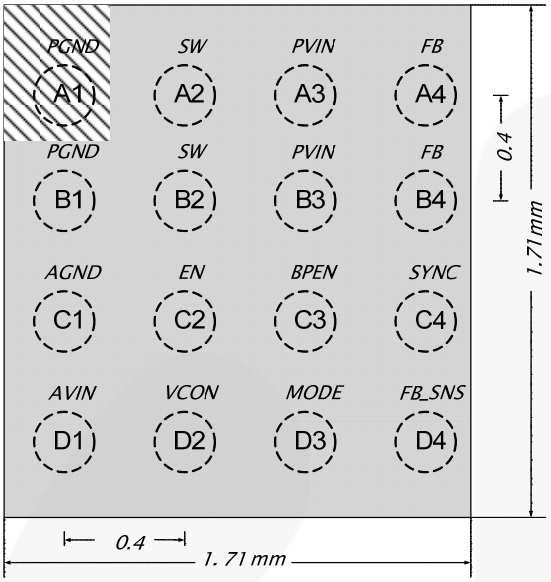

Figure 3. Bumps Face Down – Top-Through View

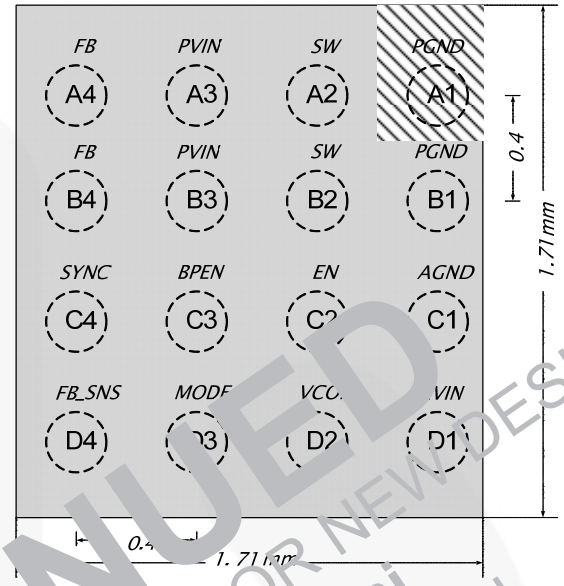

Figure 4. Bumps Face Up

Pin Definitions

Pin #	Name	Description
C1	AGND	Analog ground, reference ground for the IC. Follow PCB routing notes for connecting this pin.
A4, B4	FB	Output voltage sense pin. Connect to V_{OUT} to establish feedback path for regulation point. Connect together on PCB.
D4	FB_SNS	Feedback Sense pin. Connect to FB pins on PCB.
C2	EN	Enables switcher when HIGH; Shutdown Mode when LOW. This pin should not be left floating.
D2	VCON	Analog control pin. Shield signal routing against noise.
D1	AVIN	Analog supply voltage input. Connect to PVIN.
C3	BPEN	Force bypass when HIGH; Auto bypass when LOW. This pin should not be left floating.
C4	SYNC	External clock synchronization input. When SYNC is HIGH, the DC-DC does not allow PFM Mode. Tie SYNC to AGND if not used or in Auto-PFM Mode. This pin should not be left floating.
D3	MODE	Low-Power Auto Mode / High-Power PWM Mode select. When MODE = 1, the DC-DC is configured for 6MHz Low-Power Auto Mode. When MODE = 0, the DC-DC is configured for 3MHz High-Power PWM Mode. This pin should not be left floating.
A3, B3	PVIN	Supply voltage input to the internal MOSFET switches. Connect to input power source.
A2, B2	SW	Switching node of the internal MOSFET switches. Connect to output inductor.
A1, B1	PGND	Power ground of the internal MOSFET switches. Follow routing notes for connections between PGND and AGND.

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Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on AVIN, PVIN		-0.3	6.0	V
	Voltage on Any Other Pin		-0.3	AV_{IN} + 0.3	
T_J	Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature (10 Seconds)			+260	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101			

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the data sheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range	2.7		5.5	V
V_{OUT}	Output Voltage Range	0.35		<V_{IN}	V
I_{OUT_BYP}	Output Current (Bypass Mode)			3.0	A
$I_{OUT_LP_MODE}$	Output Current (Low Power Mode)			1.2	A
$I_{OUT_HP_MODE}$	Output Current (High-Power Mode)			2.3	A
L	Inductor for Smallest PCB Footprint		470		nH
	Inductor for Optimum Efficiency Performance		1.0		µH
C_{IN}	Input Capacitor[1]		10		µF
C_{OUT}	Output Capacitor		2 x 4.7		µF
T_A	Operating Ambient Temperature Range	-40		+85	°C
T_J	Operating Junction Temperature Range	-40		+125	°C

Note:

1. A large enough input capacitor value is required for limiting the input voltage drop during GSM bursts, bypass transitions, or during large output voltage transitions.

Dissipation Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance[2]		80		°C/W

Note:

2. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(MAX)}$ at a given ambient temperate T_A.

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Electrical Characteristics, All Power Modes

V_{IN} = V_{OUT} + 0.6 V, I_{OUT} = 200 mA, EN = V_{IN}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{IN} = 3.7 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
V_{IN}	Input Voltage range	I_{OUT} ≤ 2.3 A	3.0		5.5	V
I_{SD}	Shutdown Supply Current	EN = 0 V		1.0	3.0	µA
V_{UVLO}	Under Voltage Lockout Threshold	V_{IN} Rising	2.30	2.45	2.60	V
		Hysteresis		175		mV
Logic Control						
V_{IH}	Logic Threshold Voltage EN, BPEN, SYNC, MODE	Input HIGH Threshold	1.2			V
V_{IL}		Input LOW Threshold			0.4	
I_{CTRL}	Logic Control Input Bias Current EN, BPEN, SYNC, MODE	V_{IN} or GND		0.01	1.00	µA
Analog Control						
$V_{CON_BP_EN}$	V_{CON} Forced Bypass Enter	V_{CON} Voltage that Forces Bypass; V_{IN} = 2.70 V - 4.75 V	1.6			V
$V_{CON_BP_EX}$	V_{CON} Forced Bypass Exit	V_{CON} Voltage that Exits Forced Bypass; V_{IN} = 2.70 V - 4.75 V			1.4	V
Gain	Gain in Control Range: 0.16 V to 1.40 V			2.5		
V_{OUT_ACC}	V_{OUT} Accuracy	V_{OUT} = 2.5 x V_{CON}	-50		+50	mV
Bypass						
R_{FET}	Bypass FET Resistance[3]			35		mΩ
ΔV_{OUT_BP}	Bypass Mode Output Voltage Drop	I_{OUT} = 2 A		70		mV
Over Temperature Protection						
T_{OTP}	Over-Temperature Protection	Rising Temperature		+150		°C
		Hysteresis		+20		°C

Note

3. Bypass FET resistance does not include PFET R_{DSON} and inductor DCR in parallel with the bypass FET in Bypass Mode.

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Electrical Characteristics, Low-Power Auto Mode (MODE = 1)

V_{IN} = V_{OUT} + 0.6 V, I_{OUT} = 200 mA, EN = V_{IN}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{IN} = 3.7 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Oscillator / Synchronization						
f_{SW}	Average Oscillator Frequency		5.4	6.0	6.6	MHz
f_{SYNC}	Synchronization Frequency Range[4]		4.8	6.0	7.2	MHz
DC-DC						
R_{DSON}	PMOS On Resistance	V_{IN} = V_{GS} = 3.7 V		210		mΩ
	NMOS On Resistance	V_{IN} = V_{GS} = 3.7 V		125		mΩ
I_{LIMp}	P-Channel Current Limit		1.35	1.65	1.95	A
I_{LIMn}	N-Channel Current Limit		1.00	1.30	1.70	A
V_{OUT_MIN}	Minimum Output Voltage	V_{CON} = 0.16 V	0.35	0.40	0.45	V
V_{OUT_MAX}	Maximum Output Voltage	V_{CON} = 1.40 V	3.45	3.50	3.55	V
DC-DC Efficiency						
η_{Power}	Power Efficiency, Low-Power Auto Mode, V_{IN} = 3.7 V	V_{OUT} = 3.1 V, I_{LOAD} = 25 mA		95		%
		V_{OUT} = 1.8 V, I_{LOAD} = 25 mA		90		
		V_{OUT} = 1.5 V, I_{LOAD} = 10 mA		65		
Output Regulation						
V_{OUT_RLine}	V_{OUT} Line Regulation	3.2 V ≤ V_{IN} ≤ 4.7		+5		mV
V_{OUT_RLoad}	V_{OUT} Load Regulation	20 mA ≤ I_{OUT} ≤ 800 mA		+25		mV
$V_{BYPSLEW}$	V_{OUT} Slew Rate	During Bypass Enabling		0.25		V/µs
V_{BP_ThH}	Voltage Threshold to Enter Bypass	V_{IN} – V_{PMOS} – V_{OUT}	140	190	240	mV
V_{BP_ThL}	Voltage Threshold to Exit Bypass	V_{IN} – V_{OUT}	340	400	440	mV
V_{OUT_Ripple}	V_{OUT} Ripple[4]	PFM Mode, V_{IN} = 3.8 V, I_{OUT} < 100 mA		11		mV
		PWM Mode, V_{IN} = 3.8 V		4		
Timing						
t_{SS}	Start-up Time	V_{IN} = 3.7 V, V_{OUT} from 0 V to 3.1 V, C_{OUT} = 2 x 4.7 µF, 10 V, X5R		50	60	µs
$t_{DC\text{-}DC_TR}$	V_{OUT} Step Response Rise Time[5]	V_{OUT} from 5% to 95%, ΔV_{OUT} < 2 V (1.4 V – 3.4 V), R_{LOAD} ≤ 7 Ω			10	µs
$t_{DC\text{-}DC_TF}$	V_{OUT} Step Response Fall Time[5]	V_{OUT} from 95% to 5%, ΔV_{OUT} < 2 V (3.4 V – 1.4 V), R_{LOAD} ≤ 7 Ω			10	µs
$t_{DC\text{-}DC_CL}$	Maximum Allowed Time for Consecutive Current Limit[6]			40		µs
t_{DCDC_CLR}	Consecutive Current Limit Recovery Time[4]			180		µs

Notes:

4. Guaranteed by design; not tested in production.
5. Guaranteed by design; not tested in production. Voltage transient only. Maximum specified V_{OUT} transition step is 3.1 V. Assumes C_{OUT} = 2 x 4.7 µF.
6. Protects part under short-circuit conditions. After 40 µs nominally, operation halts and restarts after 180 µs nominally. Under heavy capacitive loads, V_{CON} slew rate should be reduced to avoid consecutive current limits. Under typical conditions for a 3 V change at the output, a capacitive only load of up to 40 µF is supported (assuming a step at the V_{CON} input).

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Electrical Characteristics, High-Power PWM Mode (MODE = 0)

V_{IN} = V_{OUT} + 0.6 V, I_{OUT} = 200 mA, EN = V_{IN}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{IN} = 3.7 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Oscillator / Synchronization						
f_{SW}	Average Oscillator Frequency		2.7	3.0	3.3	MHz
f_{SYNC}	Synchronization Frequency Range(7)		2.4	3.0	3.6	MHz
DC-DC						
R_{DSON}	PMOS On Resistance	V_{IN} = V_{GS} = 3.7 V		105		mΩ
	NMOS On Resistance	V_{IN} = V_{GS} = 3.7 V		[illegible]		mΩ
I_{LIMp}	P-Channel Current Limit		2.7	3.3	3.9	A
I_{LIMn}	N-Channel Current Limit		[illegible].0	1.3	1.7	A
V_{OUT_MIN}	Minimum Output Voltage	V_{CON} = 0.16 V	[illegible]	[illegible]40	0.45	V
V_{OUT_MAX}	Maximum Output Voltage	V_{CON} = 1.40 V	[illegible]45	3.50	3.55	V
DC-DC Efficiency						
η_{Power}	Power Efficiency, High-Power Auto Mode, V_{IN} = 3.7 V	V_{OUT} = 3.3 V, I_{L} = 1.[illegible]		92		%
		V_{OUT} = 2.0 V, [illegible]OAD = 0.2		8[illegible]		
Output Regulation						
V_{OUT_RLine}	V_{OUT} Line Regulation	1 ≤ V_{IN} 3.7		+5		mV
V_{OUT_RLoad}	V_{OUT} Load Regulation	20[illegible]A ≤ I_{OUT} ≤ 2000 mA		+25		mV
$V_{BYPSLEW}$	V_{OUT} Slew Rate	D[illegible] Bypass Enabling		0.25		V/µs
V_{BP_ThH}	Voltage Threshold to Enter Bypass	V_{IN} – V_{PMOS} – V_{OUT}	295	340	385	mV
V_{BP_ThL}	Voltage Threshold to Exit Bypass	V_{IN} – V_{OUT}	550	650	750	mV
V_{OUT_Ripple}	V_{OUT} Ripple(7)	PWM Mode, V_{IN} = 3.8 V		4		mV
Timing						
t_{SS}	Start-up Time	V_{IN} = 3.7 V, V_{OUT} from 0 V to 3.1 V, C_{OUT} = 2 x 4.7 µF, 10 V, X5R		50	60	µs
$t_{DC\text{-}DC_R}$	V_{OUT} Step Response Rise Time(8)	V_{OUT} from 5% to 95%, ΔV_{OUT} < 1.5 V (0.5 V – 2.0 V), R_{LOAD} ≤ 7 Ω			10	µs
$t_{DC\text{-}DC_TF}$	V_{OUT} Step Response Fall Time(8)	V_{OUT} from 95% to 5%, ΔV_{OUT} < 1.5 V (2.0 V – 0.5 V), R_{LOAD} ≤ 7 Ω			10	µs
$t_{DC\text{-}DC_TR}$	V_{OUT} Step Response Rise Time(8)	V_{OUT} from 5% to 95%, ΔV_{OUT} < 3.0 V (0.4 V – 3.4 V), R_{LOAD} ≤ 7 Ω			10	µs
$t_{DC\text{-}DC_TF}$	V_{OUT} Step Response Fall Time(8)	V_{OUT} from 95% to 5%, ΔV_{OUT} < 3.0 V (3.4 V – 0.4 V), R_{LOAD} ≤ 7 Ω			12	µs
$t_{DC\text{-}DC_CL}$	Maximum Allowed Time for Consecutive Current Limits(9)			40		µs
t_{DCDC_CLR}	Consecutive Current Limit Recovery Time(4)			180		µs

Notes:
7. Guaranteed by design; not tested in production.
8. Guaranteed by design; not tested in production. Voltage transient only. Maximum specified V_{OUT} transition step is 3.1 V. Assumes C_{OUT} = 2 x 4.7 µF.
9. Protects part under short-circuit conditions. Under heavy capacitive loads, V_{CON} slew rate may be adjusted to avoid consecutive current limits. Under typical conditions for a 3 V change at the output, a capacitive only load of up to 40 µF is supported (assuming a step at the V_{CON} input).

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Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{OUT} = 2 x 4.7 µF, and T_A = +25°C.

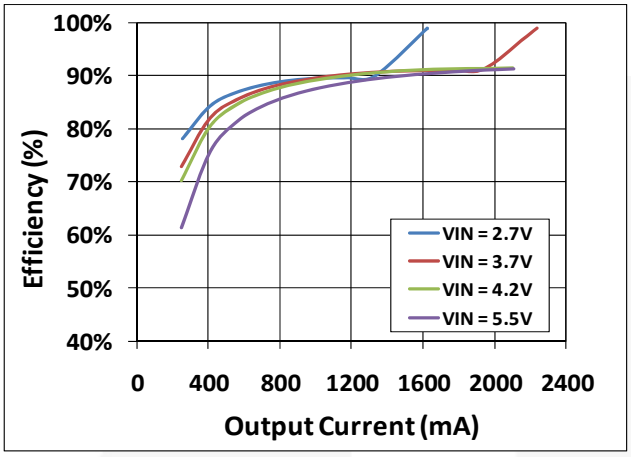

Figure 5. High-Power PWM Mode Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 1.5 Ω

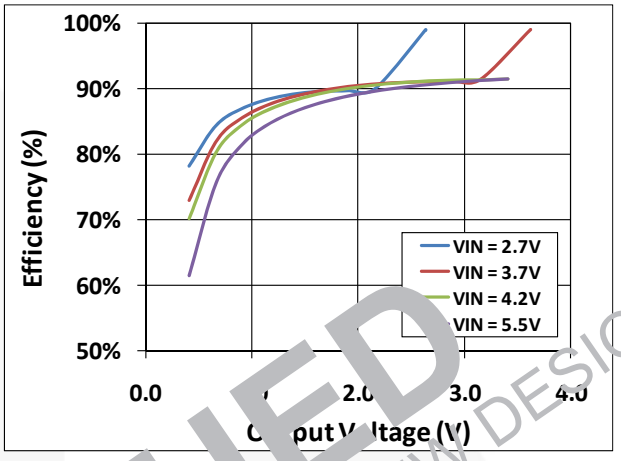

Figure 6. High-Power PWM Mode Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 1.5 Ω

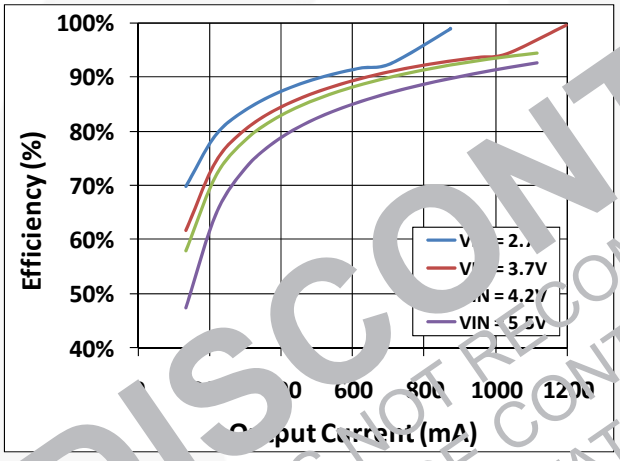

Figure 7. High-Power PWM Mode Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 3.0 Ω

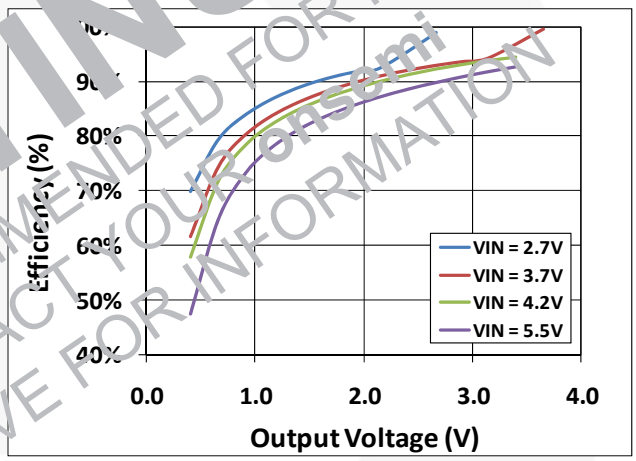

Figure 8. High-Power PWM Mode Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 3.0 Ω

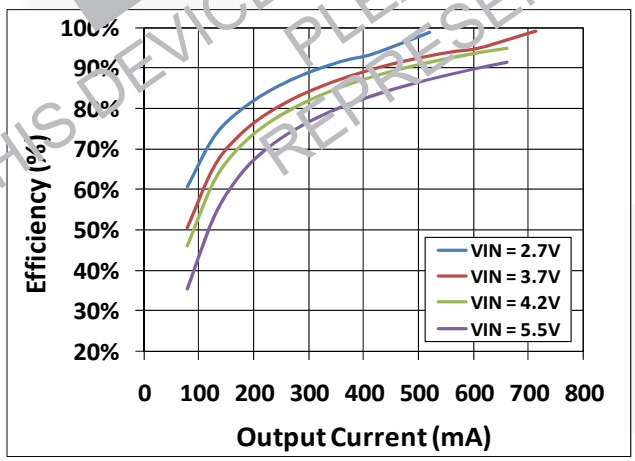

Figure 9. High-Power PWM Mode Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 5.0 Ω

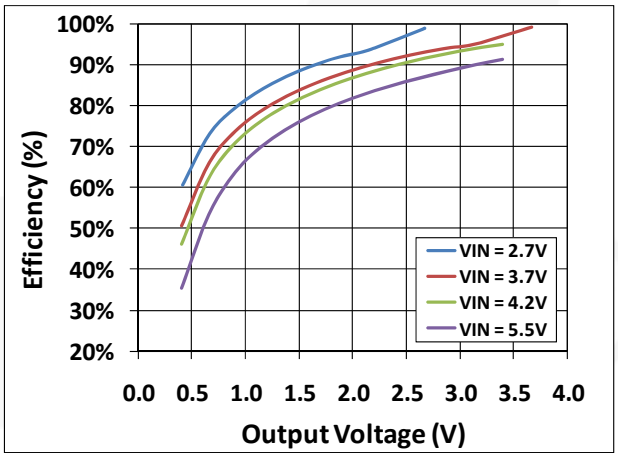

Figure 10. High-Power PWM Mode Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 5.0 Ω

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Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{OUT} = 2 x 4.7 µF, and T_A = +25°C.

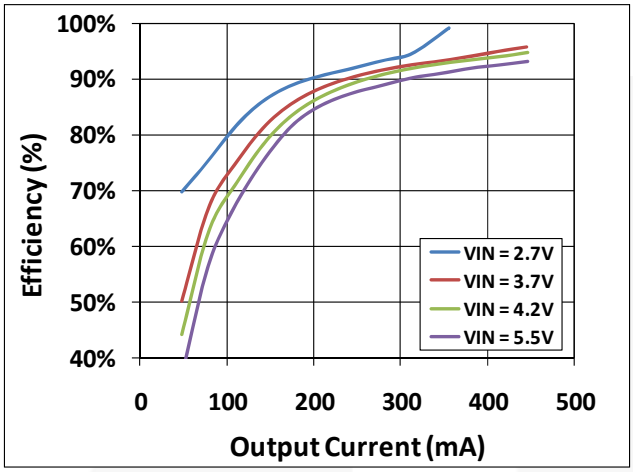

Figure 11. Low-Power Auto Mode Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 7.0 Ω

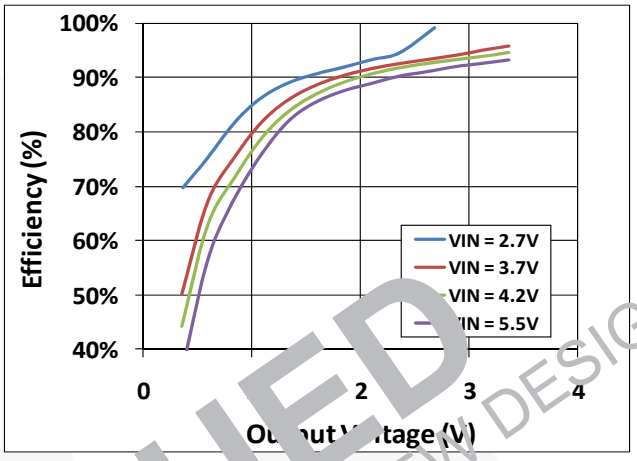

Figure 12. Low-Power Auto Mode Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 7.0 Ω

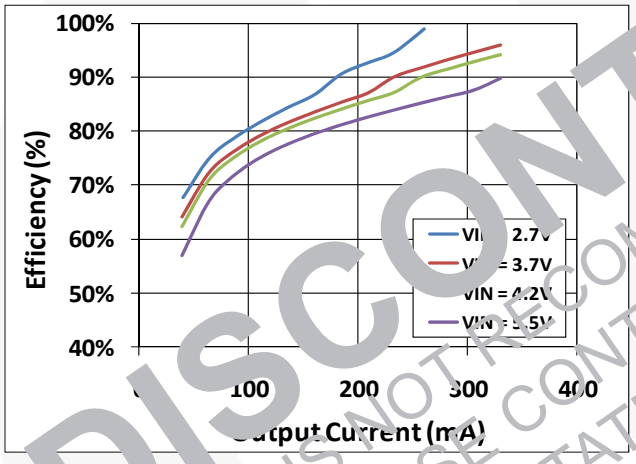

Figure 13. Low-Power Auto Mode Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 10.0 Ω

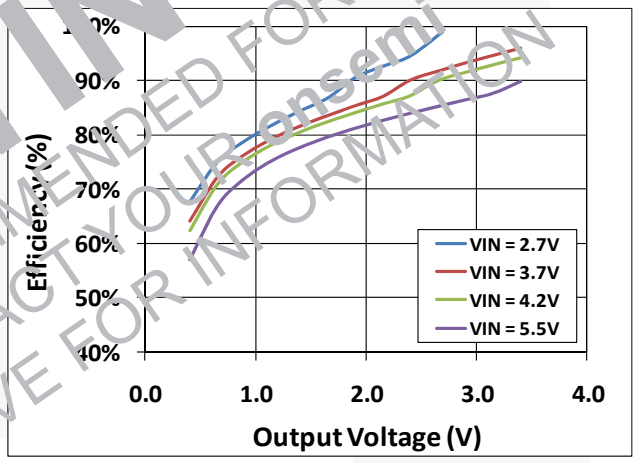

Figure 14. Low-Power Auto Mode Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 10.0 Ω

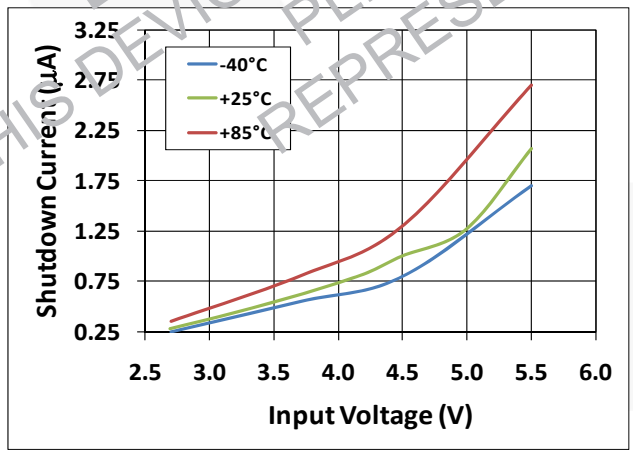

Figure 15. Shutdown Current vs. Input Voltage vs. Temperature

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Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{OUT} = 2 x 4.7 µF, and T_A = +25°C.

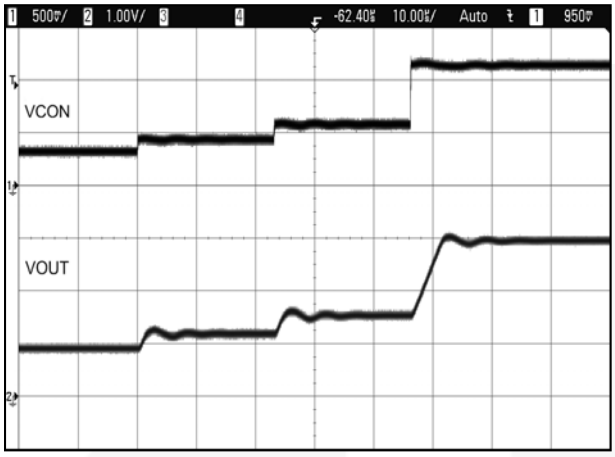

Figure 16. Rise Times for 300 mV, 500 mV, and 2 V ΔV_{OUT} (V_{IN} = 3.7 V)

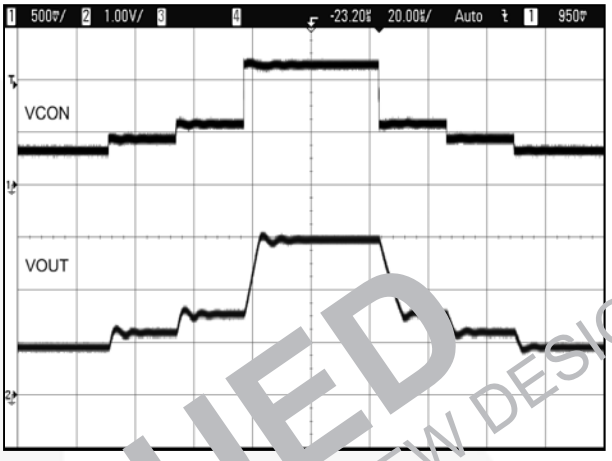

Figure 17. Rise Times for 300 mV, 500 mV, and 2 V ΔV_{OUT} (V_{IN} = 3.7 V)

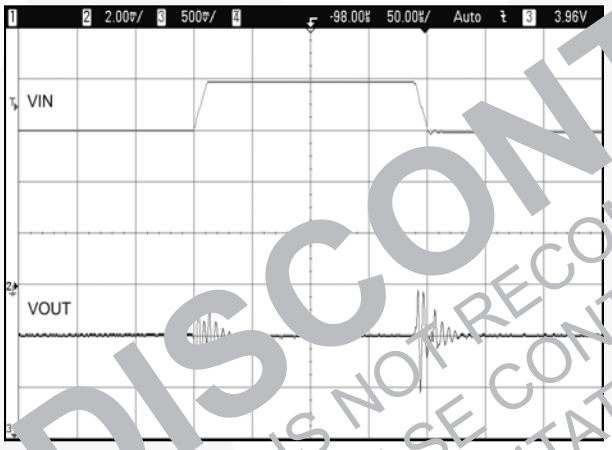

Figure 18. Line Transient V_{IN} = 3.7 V to 4.2 V, V_{OUT} = 1.0 V, 10 Ω Load, 50 µs/div.

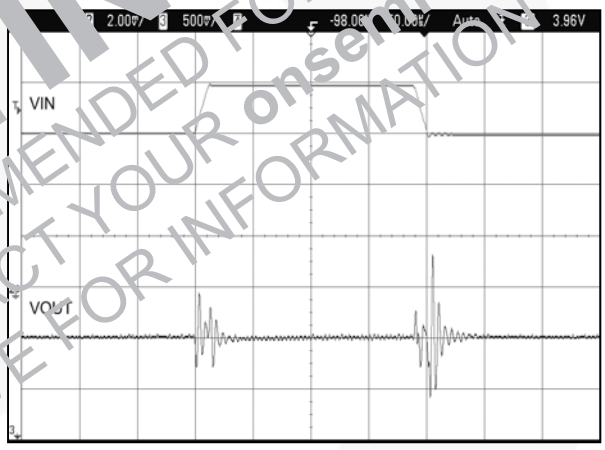

Figure 19. Line Transient V_{IN} = 3.7 V to 4.2 V, V_{OUT} = 2.5 V, 10 Ω Load, 50 µs/div.

Figure 20. Line Transient V_{IN} = 3.7 V to 4.2 V, V_{OUT} = 1.0 V, 5 Ω Load, 50 µs/div.

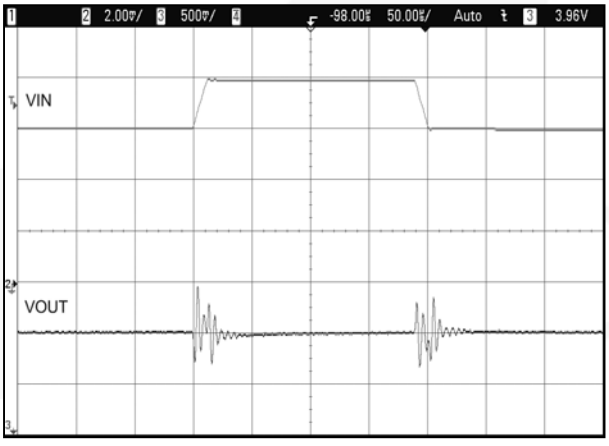

Figure 21. Line Transient V_{IN} = 3.7 V to 4.2 V, V_{OUT} = 2.5 V, 5 Ω Load, 50 µs/div.

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Typical Characteristics

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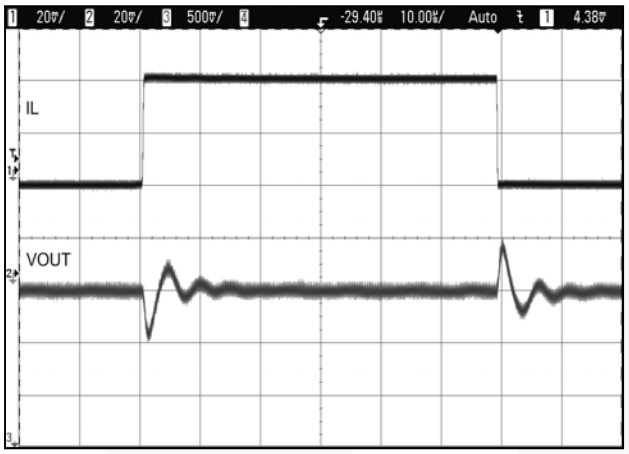

Figure 22. Load Transient, 0 mA to 400 mA, V_{OUT} = 1.0 V in High-Power Mode

Figure 23. Load Transient, 0 mA to 400 mA, V_{OUT} = 1.0 V in Low-Power Mode

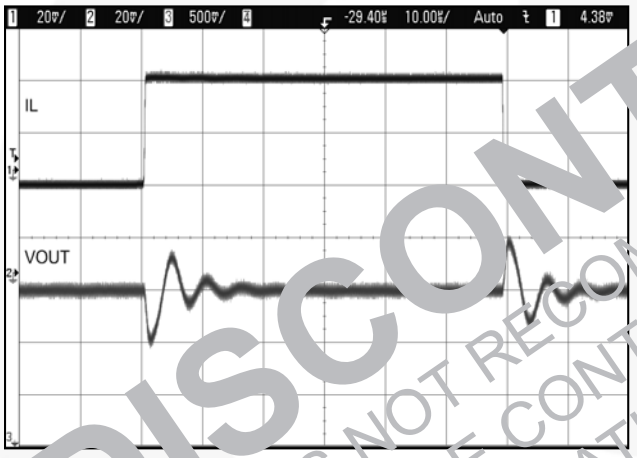

Figure 24. Load Transient, 0 mA to 400 mA, V_{OUT} = 2.5 V in High-Power Mode

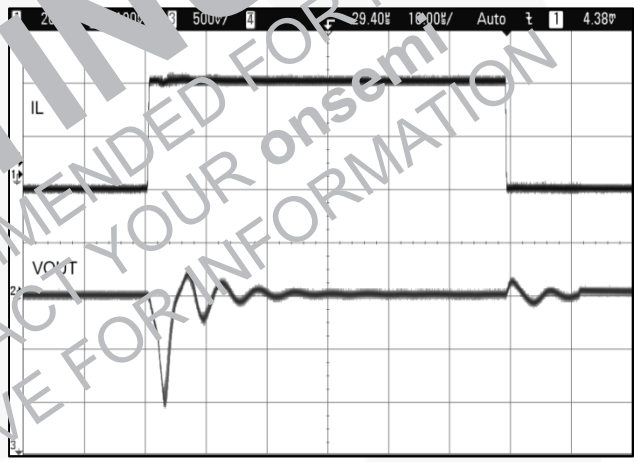

Figure 25. Load Transient, 0 mA to 400 mA, V_{OUT} = 2.5 V in Low-Power Mode

Figure 26. Load Transient, 200 mA to 800 mA, V_{OUT} = 1.0 V in High-Power Mode

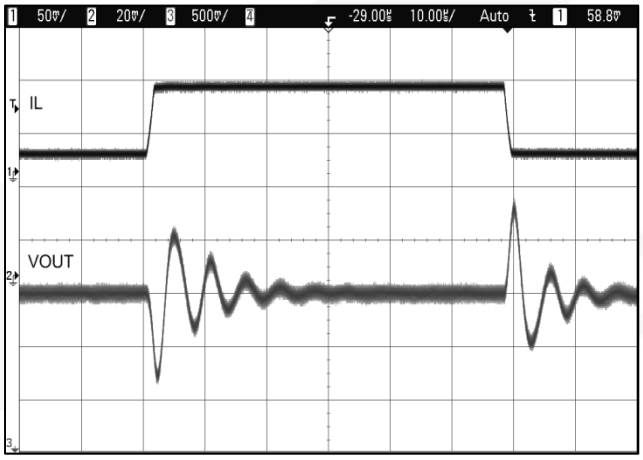

Figure 27. Load Transient, 200 mA to 800 mA, V_{OUT} = 1.0 V in Low-Power Mode

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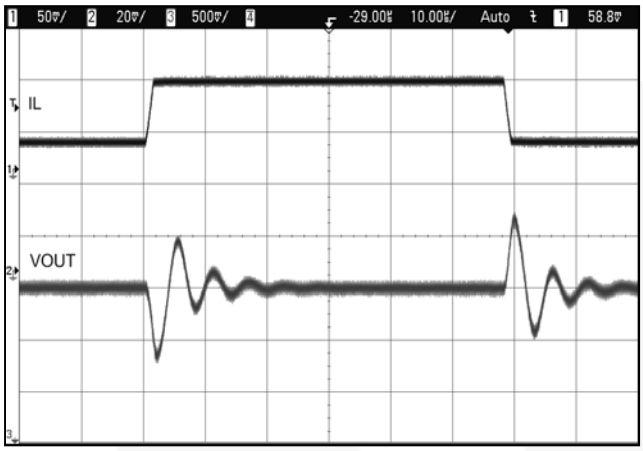

Figure 28. Load Transient, 200 mA to 800 mA, V_{OUT} = 2.5 V in High-Power Mode

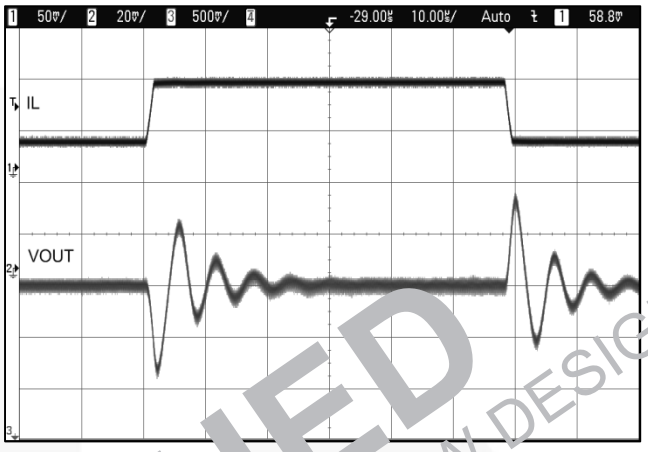

Figure 29. Load Transient, 200 mA to 800 mA, V_{OUT} = 2.5 V in Low-Power Mode

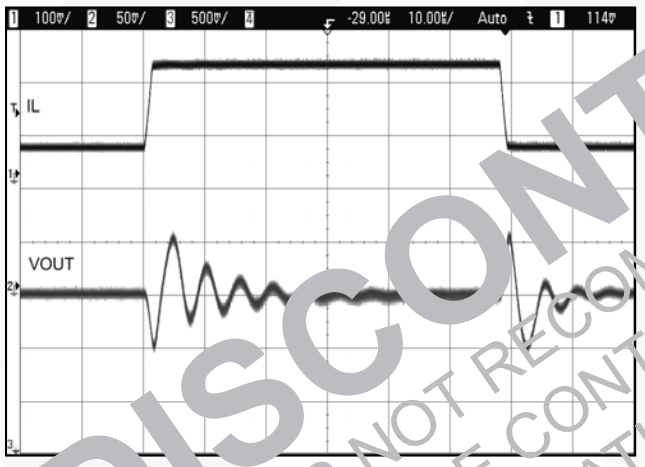

Figure 30. Load Transient, 400 mA to 2000 mA, V_{OUT} = 1.0 V in High-Power Mode

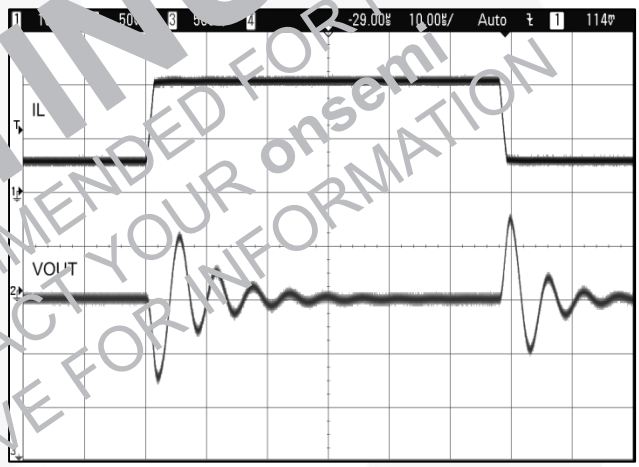

Figure 31. Load Transient, 400 mA to 2000 mA, V_{OUT} = 2.5 V in High-Power Mode

Figure 32. Switching Waveforms, PFM Mode, I_{LOAD} = 10 mA in Low-Power Mode

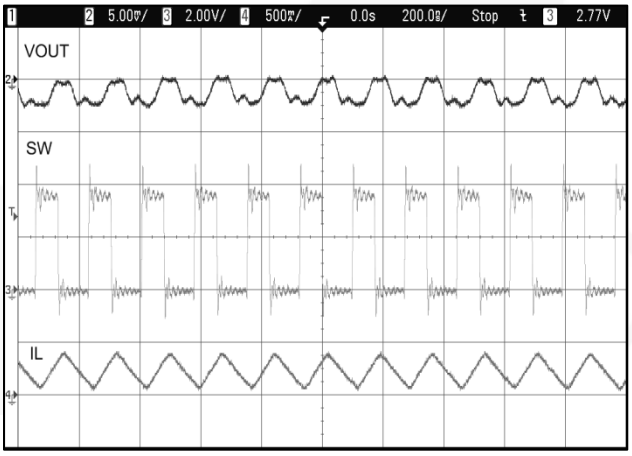

Figure 33. Switching Waveforms, PWM Mode, f_{SW} = 6 MHz, I_{LOAD} = 300 mA in Low-Power Mode

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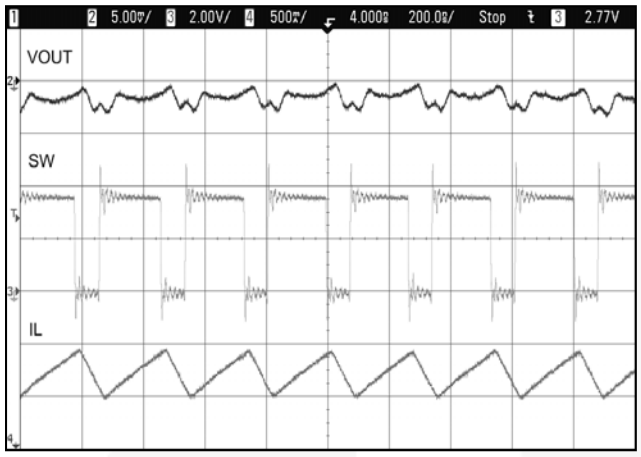

Figure 34. Switching Waveforms, PWM Mode, f_{SW} = 3 MHz, I_{LOAD} = 800 mA in High-Power Mode

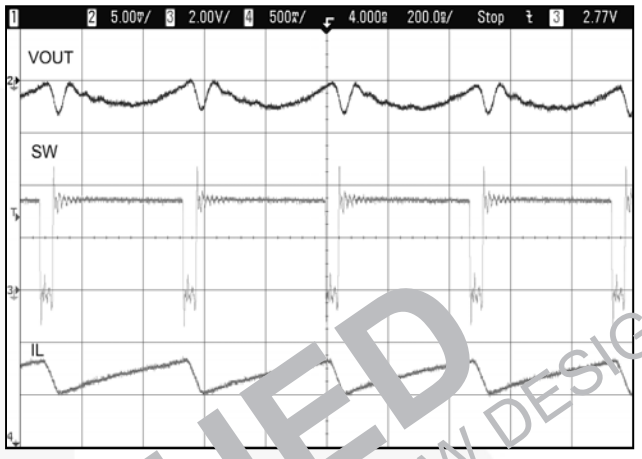

Figure 35. Switching Waveforms, PWM Mode, f_{SW} = 3 MHz, I_{LOAD} = 800 mA in High-Power Mode

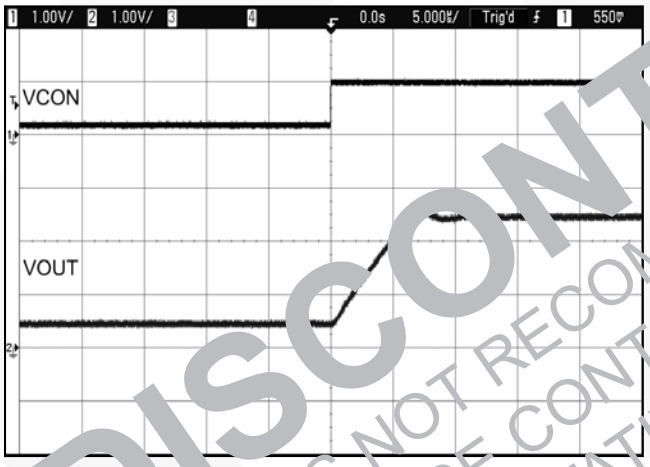

Figure 36. V_{OUT} Rising Transition 0.5 V to 2.5 V, V_{IN} = 3.7 V in Low-Power Mode

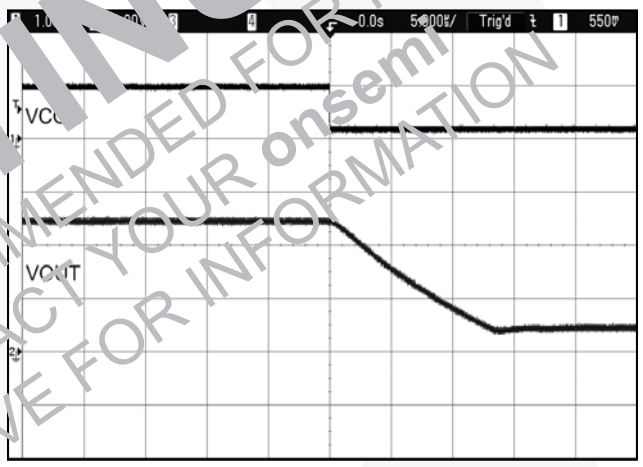

Figure 37. V_{OUT} Falling Transition 2.5 V to 0.5 V, V_{IN} = 3.7 V in Low-Power Mode

Figure 38. V_{OUT} Rising Transition 0.5 V to 3.0 V, V_{IN} = 3.7 V in High-Power Mode

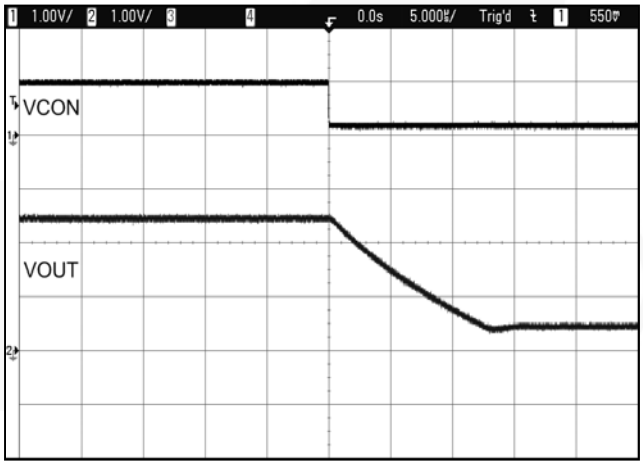

Figure 39. V_{OUT} Falling Transition 3.0 V to 0.5 V, V_{IN} = 3.7 V in High-Power Mode

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Typical Characteristics

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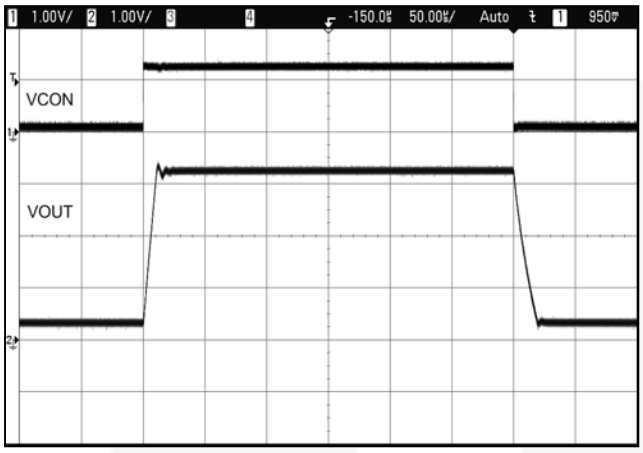

Figure 40. V_{OUT} Transient Response ΔV_{OUT} = 3 V in High-Power Mode

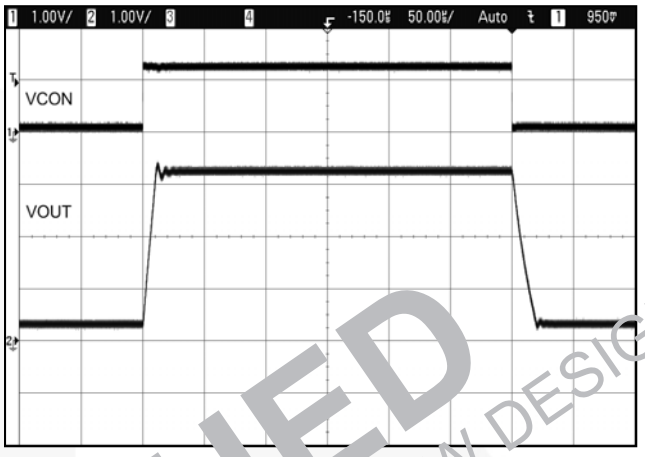

Figure 41. V_{OUT} Transient Response ΔV_{OUT} = 3 V in Low-Power Mode

Figure 42. V_{OUT} Transient and Bypass Response ΔV_{OUT} > 3 V, V_{CON} Stepped Above 1.5 V

Figure 43. V_{OUT} Transient and Bypass Response ΔV_{OUT} > 3 V, V_{CON} Stepped Above 1.5 V

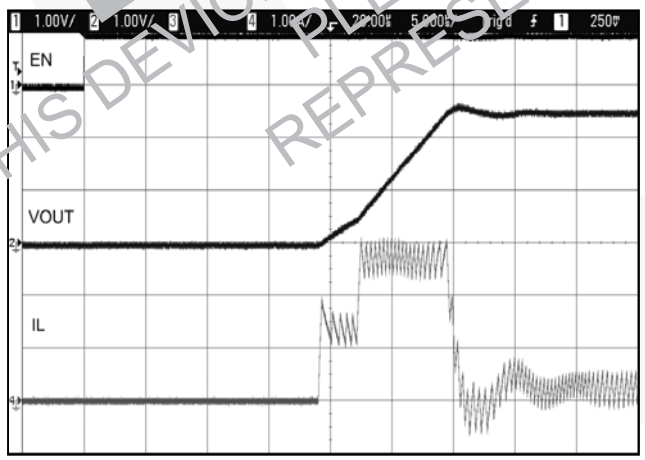

Figure 44. Soft-Start Transient Response from 0 mA to 100 mA in High-Power Mode

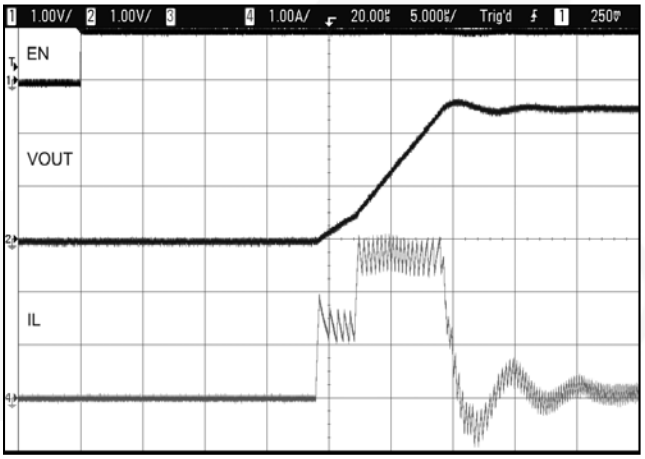

Figure 45. Soft-Start Transient Response from 0 mA to 100 mA in Low-Power Mode

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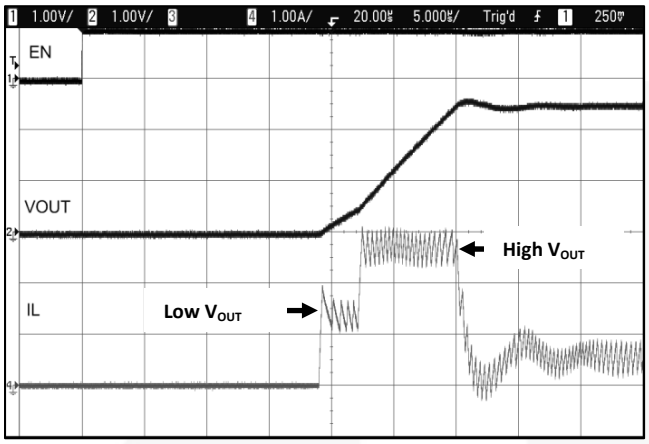

Figure 46. Soft-Start Transient Response from 0 mA to 800 mA in High-Power Mode

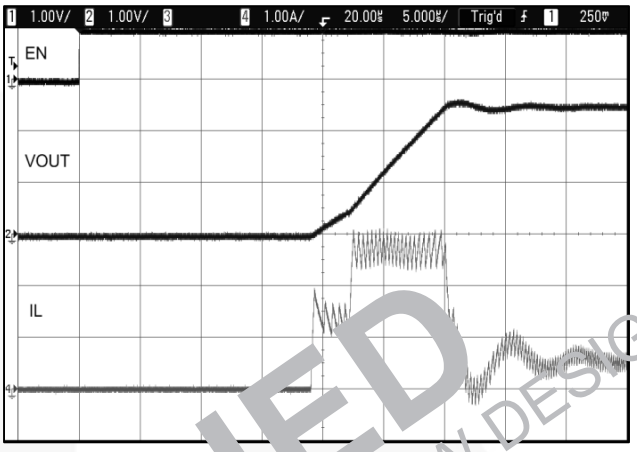

Figure 47. Soft-Start Transient Response from 0 mA to 800 mA in Low-Power Mode

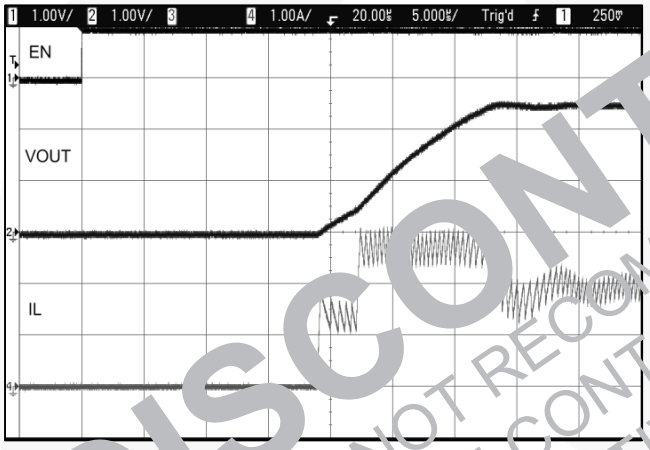

Figure 48. Soft-Start Transient Response from 0 mA to 2000 mA in High-Power Mode

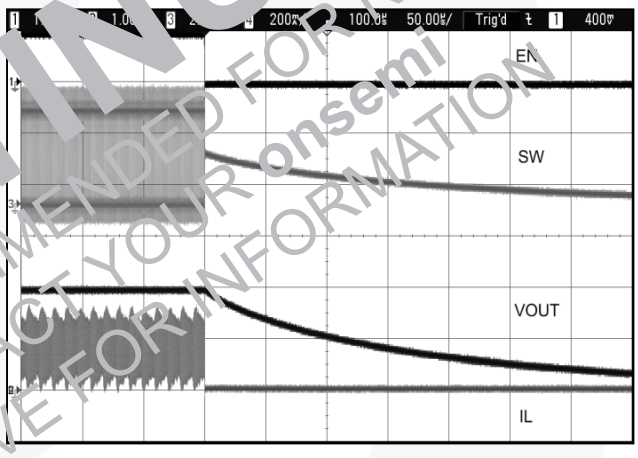

Figure 49. Shutdown Transient Response, No Load

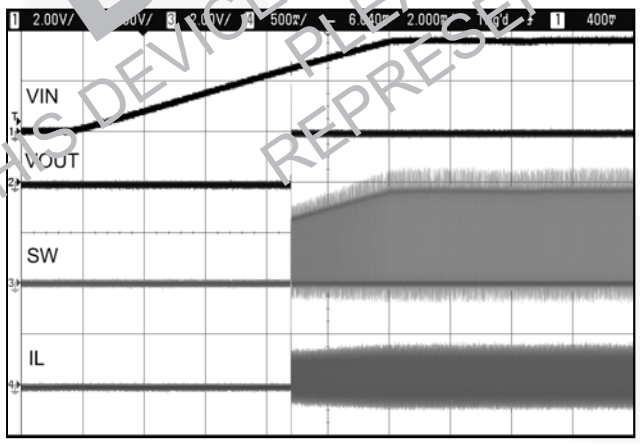

Figure 50. Cold-Start Transient Response from 0 mA to 100 mA in High-Power Mode

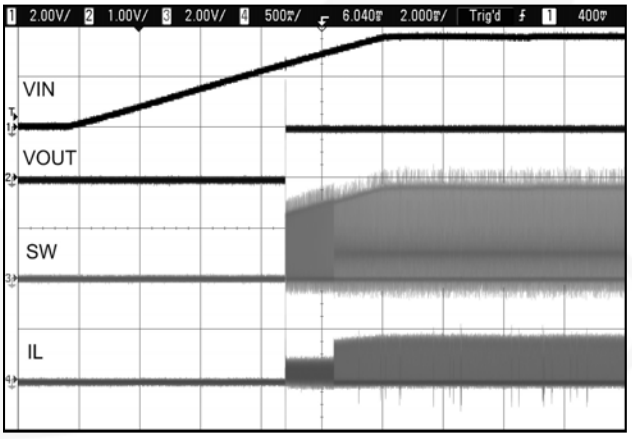

Figure 51. Cold-Start Transient Response from 0 mA to 100 mA in Low-Power Mode

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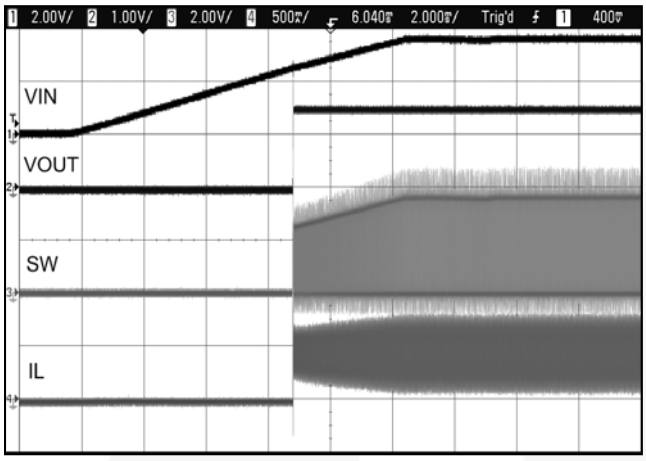

Figure 52. Cold-Start Transient Response from 0 mA to 500 mA in High-Power Mode

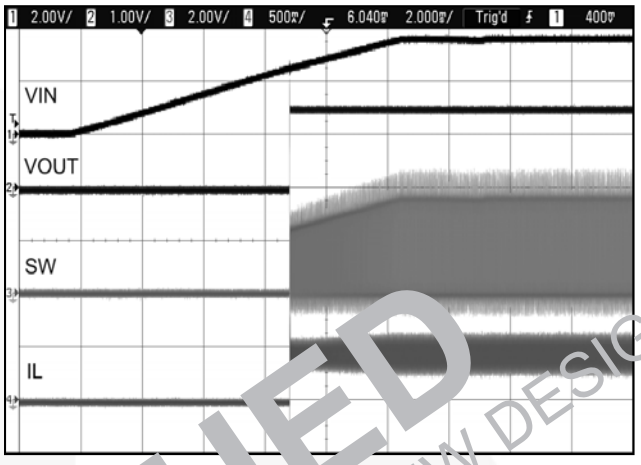

Figure 53. Cold-Start Transient Response from mA to 500 mA in Low-Power Mode

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Operating Description

The FAN5904 is a high-efficiency, synchronous, step-down converter operating with current-mode control. A wide range of load currents is supported. High-current applications, up to a DC output of 2.3 A demanded by GSM/EDGE applications, are allowed. Performance degradation due to spurs is mitigated by selection of a 3 MHz or 6 MHz switching rate. Moreover, the FAN5904 offers Bypass Mode, where the output is shorted to the battery input via a low on-state resistance bypass FET.

The output voltage V_{OUT} is regulated to 2.5 times the input control voltage, V_{CON}, set by an external DAC. The FAN5904 operates in either PWM or PFM Mode, depending on the output voltage and load current.

In Pulse Width Modulation (PWM) Mode, regulation begins with an on-state where a P-channel transistor is turned on and the inductor current is ramped up until the off-state begins. In off-state, the P-channel is switched off and an N-channel transistor is turned on. The inductor current decreases to maintain an average value equal to the DC load current. The inductor current is continuously monitored. A current sense detects when the P-channel transistor current exceeds the current limit and the switcher is turned back to off-state to decrease the inductor current and prevent magnetic saturation. Similarly, the current sense detects when the N-channel transistor current exceeds the current limit and redirects discharge current through the inductor back to the battery.

In Pulse Frequency Modulation (PFM) Mode, at low load currents, the FAN5904 operates in a constant on-time mode. During the on-state, the P-channel is turned on for a specified on-time before switching to off-state, during which the N-channel switch is enabled until the inductor current decreases to 0 A. The switcher output is then put in high-impedance state until a new regulation cycle starts.

PFM operation is allowed only in Low-Power Mode. At low load currents, PFM achieves higher efficiencies than PWM. To allow optimization of system performance, two versions of the FAN5904 are available. The FAN5904UC00X enables PFM only when V_{OUT} is less than approximately 1 V. The FAN5904UC01X allows PFM to be entered at higher output voltages.

PFM Mode is only enabled for output load currents nominally less than 100 mA. This realizes high efficiency down to 10mA load current. This is not supported in High-Power Mode (MODE = 0) and may be disabled in Low-Power Mode by tying the SYNC input HIGH.

Low-Power Auto Mode (MODE = 1)

Low-Power Auto Mode is ideal for 3G/3.5G and 4G applications. Current sense limits are nominally 1.65 Apk and power levels up to 29 dBm are supported.

High-Power PWM Mode (MODE = 0)

Due to the large current requirements in GSM/EDGE applications, only PWM Mode is supported when the FAN5904 is configured for High-Power Mode. Current-sense limits are increased to allow for large load currents up to a maximum of approximately 3.3 A.

Bypass Mode

In **Bypass Mode**, the DC-DC turns into 100% duty cycle and the bypass FET is turned on, which allows a very low voltage dropout and up to 3.0 A load current.

Table 4. Mode Definitions

Mode		Mode Description	Conditions			
			MODE	SYNC	BPEN	EN
1	Standby Mode	Whole IC disabled	X	X	X	0
2	Auto Mode Low Power	DC-DC in Auto Mode(10)	1	0	0	1
3	Forced PWM Mode Low Power	DC-DC in PWM Mode only	1	1	0	1
4	PWM Mode High Power	DC-DC in PWM High-Power Mode	0	0	0	1
5	Bypass Mode	Bypass FET and PFET forced to 100% duty-cycle	X	X	1	1

Note:

10. When V_{OUT} exceeds the bypass threshold, the bypass FET is enabled and the DC-DC goes to 100% duty cycle. When V_{OUT} is less than the exit threshold, the bypass FET is disabled and the DC-DC re-enters Auto Mode.

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DC Output Voltage

The output voltage of the FAN5904 is determined by V_{CON} provided by an external DAC or voltage reference:

$$V_{OUT} = 2.5 \times V_{CON} \quad (1)$$

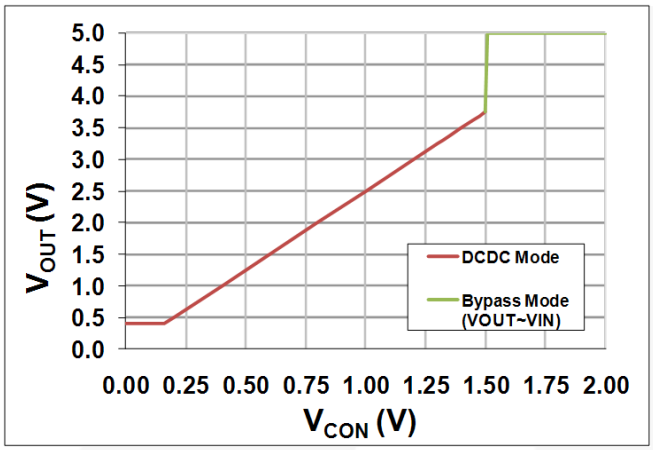

Figure 54. Output Voltage vs. Control Voltage

The FAN5904 is able to provide a regulated V_{OUT} only if V_{CON} falls within the typical range from 0.16 V to 1.40 V. This allows V_{OUT} to be adjusted between 0.4 V and 3.5 V. If V_{CON} is less than 0.16 V, V_{OUT} is clamped to 0.40 V.The part enters Bypass Mode for V_{CON} > 1.50 V. In Low-Power Mode (MODE = 1), the FAN5904 automatically switches between PFM, PWM, and Bypass Modes. In High-Power Mode (MODE = 0), the FAN5904 automatically switches between PWM and Bypass Modes and PFM operation is not available.

When V_{OUT} approaches the battery voltage, the DC-DC operates in a constant off-time mode and the frequency is adjusted to achieve high duty cycle. The system operates in this regulated mode until the bypass condition is satisfied.

Bypass Mode

As V_{OUT} and the battery voltage converge, the DC-DC begins to operate in constant off-time mode until eventually the DC-DC transitions to 100% duty cycle and the low R_{DSON} bypass FET is turned on. The battery voltage that results in 100% duty cycle operation depends on the output voltage, the voltage drop across the DC-DC converter, and the DC voltage drop across the inductor. In other words, the duty cycle is set by the ratio of the voltages across the inductor.

In many RF applications, it is undesirable for the DC-DC to reach 100% duty cycle since this would result in excessive output ripple. To minimize ripple, the FAN5904 implements a dynamic bypass threshold based on the voltage difference between the battery voltage (sensed through the AVIN pin), the voltage drop across the DC-DC PMOS device, and the internally generated reference voltage V_{REF}, as described in Figure 55. The Bypass Mode enter and exit thresholds are higher in High-Power Mode due to the higher load current capability. Bypass Mode is also entered when V_{CON} exceeds 1.5 V and exited when V_{CON} is less than 1.4 V.

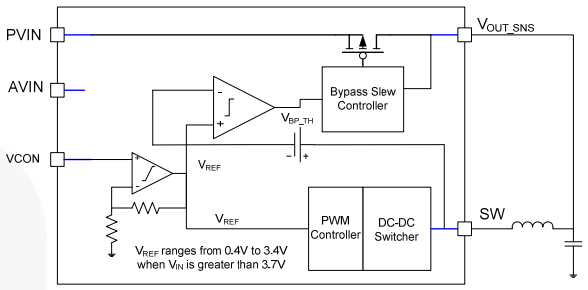

Figure 55. Enabling Bypass Transistor Circuit

The bypass FET is turned on progressively using a slew rate controller to limit the inrush current since Bypass Mode effectively shorts the input supply rails to a capacitive load.

The resulting inrush current can be expressed as a function of the specified slew rate as follows:

$$I_{INRUSH} \approx C_{OUT} \frac{\Delta V_{OUT}}{\Delta t} = C_{OUT} \bullet V_{BP_SLEW} \quad (2)$$

PFM Lockout Mode and Synchronization

It may be desirable to prevent the DC-DC converter from operating in PFM Mode. For example, the low PFM switching frequency may interfere with audio circuitry and using PWM may eliminate the interference. When configured for Low-Power Mode (MODE = 1) a logic 1 on the SYNC pin forces the IC to avoid PFM Mode. Logic 0 allows the IC to automatically switch to PFM Mode during light loads.

In Low-Power or High-Power Modes, toggling the SYNC pin forces the converter to synchronize its switching frequency to the frequency on the SYNC pin (f_{SYNC}). The signal must be within the oscillator synchronization frequency range and meet the threshold voltage requirements.

Dynamic Output Voltage Transitions

FAN5904 has a complex voltage transition controller that realizes 10µs transition times with a large output capacitor and output voltage ranges.

The transition controller manages five transitions:

- ΔV_{OUT} positive step
- ΔV_{OUT} negative step
- ΔV_{OUT} transition from or to Bypass Mode
- ΔV_{OUT} transition at startup
- ΔV_{OUT} transition after BPEN

In all cases, it is recommended that sharp V_{CON} transitions be applied, letting the transition controller optimize the output voltage slew rate.

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ΔV_{OUT} Positive Step
After a V_{CON} positive step, the FAN5904 goes into a current limit mode, where V_{OUT} ramps with a constant slew rate dictated by the output capacitor and the current limit I_{LIMp}

ΔV_{OUT} Negative Step
After a V_{CON} negative step, the FAN5904 enters a current limit mode where V_{OUT} is reduced with a constant slew rate dictated by the output capacitor and the current limit I_{LIMn}.

V_{OUT} Transition to or from Bypass Mode
The transition to or from Bypass Mode requires that the bypass conditions be met. The FAN5904 performs detection of the bypass conditions 2 µs after V_{CON} transition and enables the required charging / discharging circuit to realize a transition time of 20 µs.

V_{OUT} Transition at Startup
At startup, after EN rising edge is detected, the system requires 25 µs to allow all internal voltage references and amplifiers to start before enabling the DC-DC function.

V_{OUT} Transition after BPEN
When BPEN goes HIGH, the controller dismisses the internal bypass flags and sensors and enables Bypass Mode. However, the transition is managed with the same current limits and slew rate used during regular transitions.

Thermal Protection
When the junction temperature exceeds the maximum specified junction temperature, the FAN5904 enters Power-Down Mode (except the thermal detection circuit).

Application Information
Figure 56 illustrates an application of the FAN5904 in a GSM/EDGE/WCDMA transmitter configuration. The FAN5904 is ideal for driving multiple GSM/EDGE and 3G/3.5G and 4G PAs. Figure 57 presents a timing diagram designed to meet GSM specifications. The FAN5904 is designed to support voltage transients of 10 µs when configured for GSM/EDGE applications (MODE = 0) and driving a load capacitance of approximately 10 µF. Figure 58 shows a timing diagram for WCDMA applications.

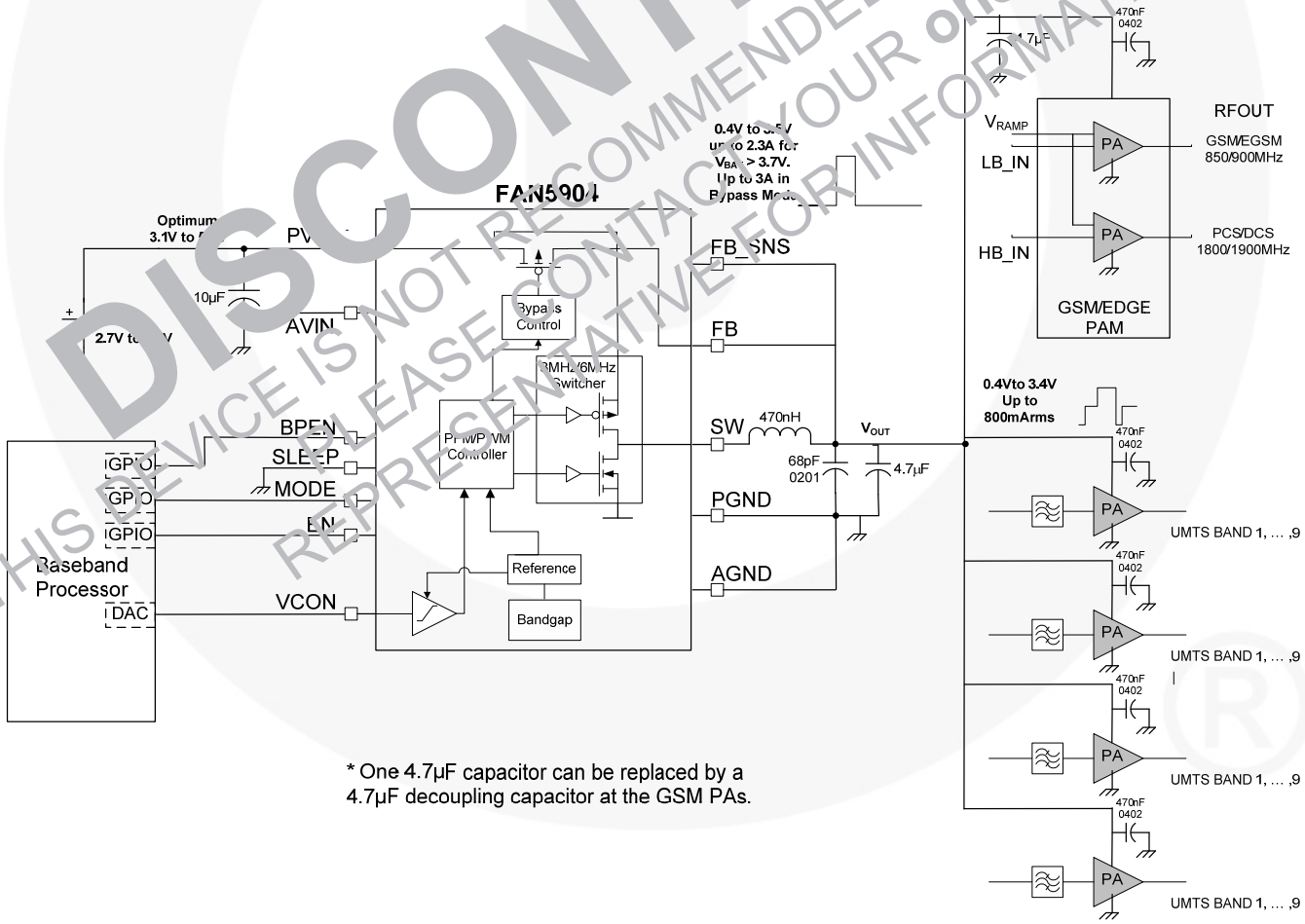

Figure 56. Typical Application Diagram with GSM/EDGE/WCDMA Transmitters

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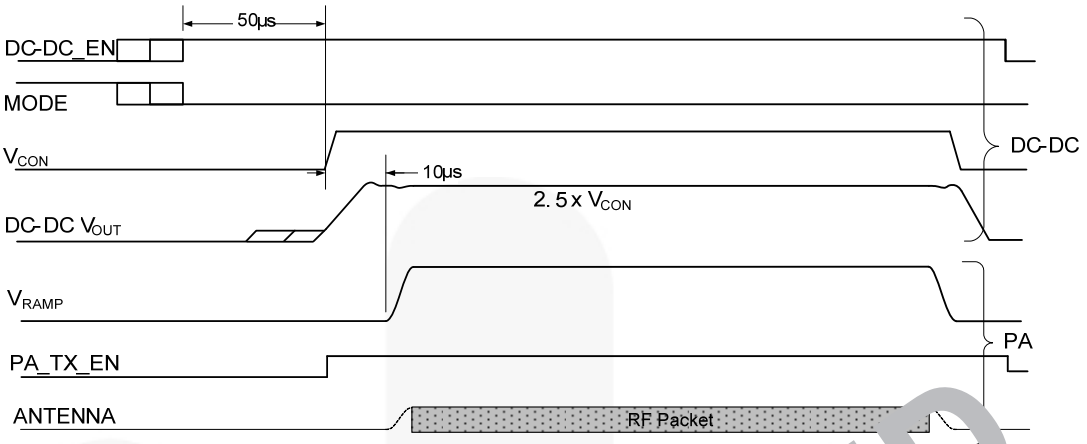

Figure 57. Timing Diagram for GSM/EDGE Transmitters

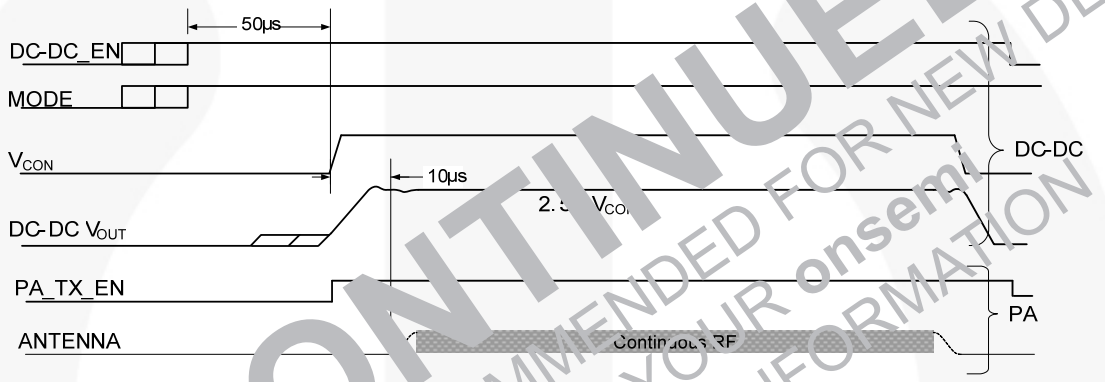

Figure 58. Timing Diagram for WCDMA Transmitters

Application Information

Inductor Selection

The FAN5904 operates at 3.6 MHz switching frequency in Low-Power Mode and 3 MHz in High-Power Mode and, as such, 470 nH – 1.0 µH inductors can be used, respectively. For applications requiring the smallest possible PCB area, use a 470 nH 2016 inductor; or a 1.0 µH 3020 inductor for optimum efficiency performance.

Table 2. Recommended Inductors

Inductor	Description
L	470 nH, ±30%, 2.3 A, 2016 (metric) TDK: VLS201610MT-R47N
	470 nH, ±30%, 2.8 A, 2520 (metric) TDK: VLS252010T-R47N
	470 nH, ±20%, 2.3 A, 2520 (metric) Samsung: CIG22HR47MNE
	470 nH, ±20%, 1.8 A, 2520 (metric) Taiyo-Yuden: CKP2520R47M
	1.0 µH, ±20%, 2.4 A, 3030 (metric) Coilcraft: XFL3010-102ME

Capacitor Selection

The minimum required output capacitor C_{OUT} should be two (2) 4.7 µF, 10 V, X5R with an ESR of 10 mΩ or lower, and an ESL of 0.3 nH or lower placed in parallel after inductor L1. Larger case sizes result in increased loop parasitic inductance and higher noise. One of the 4.7 µF capacitors should be used as a decoupling capacitor at the GSM/EDGE PA V_{CC} pin.

A 0.1 µF capacitor may be added in parallel with C_{OUT} to reduce the capacitor's parasitic inductance.

Table 3. Recommended Capacitor Values

Capacitor	Description
C_{IN}	10 µF, ±20%, X5R, 10 V
C_{OUT}	(2) 4.7 µF, ±20%, X5R, 6.3 V
C for V_{CON}	470 pF, ±20%, X5R, 25 V

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Filter VCON

VCON is the analog control pin of the DC-DC and should be connected to an external Digital-to-Analog Converter (DAC). It is recommended to add up to 470 pF decoupling capacitance between VCON and AGND to filter DAC noise. This capacitor also helps protect the DAC from the DC-DC high-frequency switching noise inherently coupled through the VCON pin. The value of the capacitor must be selected according to the DAC performance since it could limit the DAC output voltage slew rate. 470 pF is typically used.

Any noise on the V_{CON} input is transferred to V_{OUT} with a gain of two and a half (2.5). If the DAC output is noisy, a series resistor may be inserted between the DAC output and the capacitor to form an RC filter.

Follow these guidelines:

- Use a low noise source or a driver with good PSRR to generate V_{CON}.
- The V_{CON} driver must be referenced to AGND.
- V_{CON} routing must be protected against PVIN, SW, and PGND signals, as well as other noisy signals. Use AGND shielding for better isolation.
- Be sure the DAC output can drive the capacitor VCON. It may be necessary to insert a low-value resistor to ensure DAC stability while not slowing V_{CON} fast transition times.

No Floating Inputs

The FAN5904 does not have internal pull-down resistors on its inputs. Therefore, unused inputs should not be left floating and should be pulled HIGH or LOW.

PCB Layout and Component Placement

- The key consideration is the placement of the power ground PGND connection shared between the FAN5904, C1, and C2. This minimizes the parasitic inductance of the switching loop paths.
- Place the inductor away from the feedback pins to prevent unpredictable loop behavior.
- Ensure the traces are wide enough to handle the maximum current value, especially in Bypass mode.
- Ensure the vias are able to handle the current density. Use filled vias if available.
- *Refer to Fairchild's application note: AN9726 — The Importance of PCB Design for FAN5903 and FAN5904.*

Assembly

- Use lead-free solder reflow temperature profile.
- Use metal-filled or solder-filled vias, if available.
- Poor soldering can cause low DC-DC conversion efficiency. If the efficiency is low, X-ray the solder connections to verify their integrity.
- PVIN and PGND must be routed with the widest and shortest traces possible. It is acceptable for the traces connecting the inductor to be long rather than having long PVIN or PGND traces.
- Ensure that the routing loop, PVIN – PGND – VOUT is as short as possible.
- Place PGND on the top layer and connect it to the AGND ground plane next to C2 using several vias.
- The SW node is a source of electrical switching noise. Do not route it near the VCON pin.
- Two small vias are used to connect the SW node to the inductor L1. Use solder-filled vias, if available.
- The connection from C_{OUT} to FB should be wide to minimize the Bypass Mode voltage drop and the series inductance. Even if the current in Bypass Mode is small, keep this trace short and at least 5 mm wide.

  The AGND ground plane should not be broken into pieces. Ground currents must have a direct, wide path from input to output.
- Each capacitor should have at least two dedicated ground vias. Place vias within 0.1 mm of the capacitors.

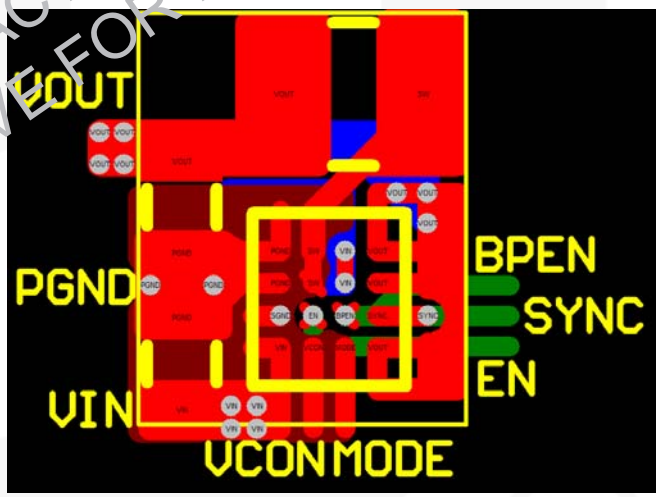

Figure 59. Example PCB Layout of FAN5904

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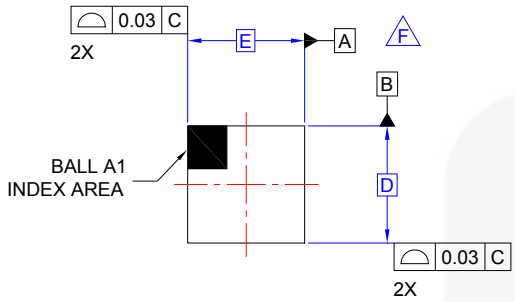
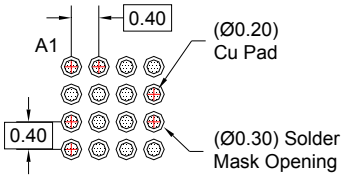
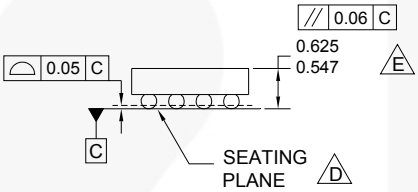
Physical Dimensions



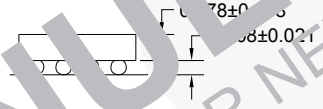
TOP VIEW

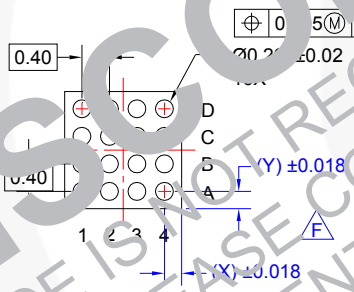


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS





BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

Product	D	E	X	Y	Unit
FAN5904UC00X	1.710 ±0.030	1.710 ±0.030	0.255	0.255	mm
FAN5904UC01X	1.710 ±0.030	1.710 ±0.030	0.255	0.255	mm

Figure 60. 1.71x1.71 mm Square, 16 Bumps, 0.4 mm Pitch, WLCSP

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