



N-CHANNEL MOSFET

Qualified per MIL-PRF-19500/556

Qualified Levels:
JAN, JANTX, and
JANTXV

DESCRIPTION

This family of 2N6782U, 2N6784U and 2N6786U switching transistors are military qualified up to the JANTXV level for high-reliability applications. These devices are also available in thru hole TO-205AF package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website <http://www.microsemi.com>.

FEATURES

- Surface mount equivalent of JEDEC registered 2N6782, 2N6784 and 2N6786 number series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/556.
(See [part nomenclature](#) for all available options.)
- RoHS compliant by design.

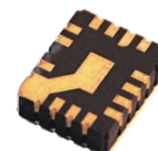
APPLICATIONS / BENEFITS

- Lightweight surface mount design enables mounting in a crowded area.
- Military and other high-reliability applications.

MAXIMUM RATINGS @ $T_A = +25^\circ\text{C}$ unless otherwise stated

Parameters / Test Conditions	Symbol	Value	Unit
Operating & Storage Junction Temperature Range	T_J & T_{stg}	-55 to +150	$^\circ\text{C}$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	8.33	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = +25^\circ\text{C}$ @ $T_C = +25^\circ\text{C}$ ⁽¹⁾	P_T	0.8 15	W
Drain-Source Voltage, dc 2N6782U 2N6784U 2N6786U	V_{DS}	100 200 400	V
Gate-Source Voltage, dc	V_{GS}	± 20	V
Drain Current, dc @ $T_C = +25^\circ\text{C}$ ⁽²⁾ 2N6782U 2N6784U 2N6786U	I_{D1}	3.50 2.25 1.25	A
Drain Current, dc @ $T_C = +100^\circ\text{C}$ ⁽²⁾ 2N6782U 2N6784U 2N6786U	I_{D2}	2.25 1.50 0.80	A
Off-State Current (Peak Total Value) ⁽³⁾ 2N6782U 2N6784U 2N6786U	I_{DM}	14.0 9.0 5.5	A (pk)
Source Current 2N6782U 2N6784U 2N6786U	I_S	3.50 2.25 1.25	A

See notes on next page.



**U-18 LCC
Package**

Also available in:

**TO-205AF (TO-39)
package**

(leadless)
2N6782 & 2N6786

MSC – Lawrence

6 Lake Street,
Lawrence, MA 01841
Tel: 1-800-446-1158 or
(978) 620-2600
Fax: (978) 689-0803

MSC – Ireland

Gort Road Business Park,
Ennis, Co. Clare, Ireland
Tel: +353 (0) 65 6840044
Fax: +353 (0) 65 6822298

Website:

www.microsemi.com

- Notes:**
1. Derate linearly 0.12 W/°C for $T_C > +25\text{ }^{\circ}\text{C}$.
 2. The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

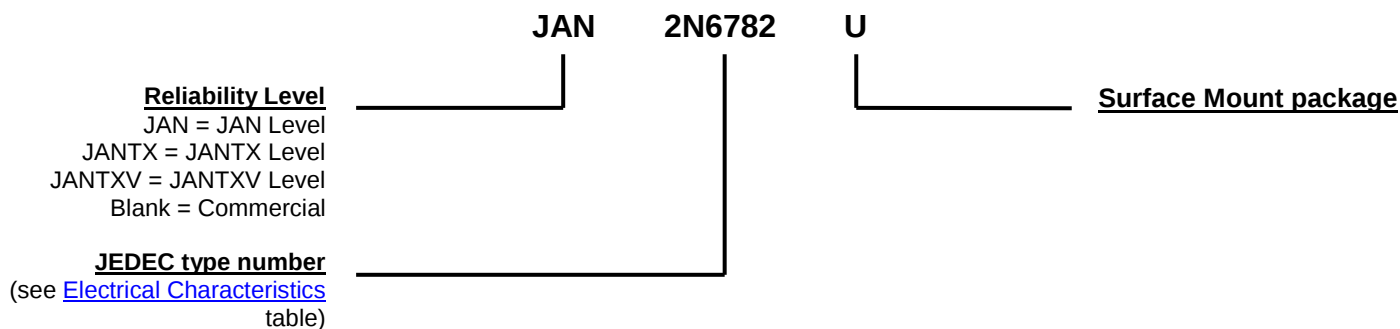
$$I_D = \sqrt{\frac{T_J(\text{max}) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(\text{max})}}$$

3. $I_{DM} = 4 \times I_{D1}$ as calculated in note 1.

MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at Pin 1 location.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See [Package Dimensions](#) on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I_F	Forward current
R_G	Gate drive impedance
V_{DD}	Drain supply voltage
V_{DS}	Drain source voltage, dc
V_{GS}	Gate source voltage, dc

ELECTRICAL CHARACTERISTICS @ $T_A = +25^\circ\text{C}$, unless otherwise noted

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$ 2N6782U 2N6784U 2N6786U	$V_{(BR)DSS}$	100 200 400		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_J = +125^\circ\text{C}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_J = -55^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0	4.0 5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}, T_J = +125^\circ\text{C}$	I_{GSS1} I_{GSS2}		± 100 ± 200	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}$ 2N6782U 2N6784U 2N6786U	I_{DSS1}		25	μA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}, T_J = +125^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}, T_J = +125^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}, T_J = +125^\circ\text{C}$ 2N6782U 2N6784U 2N6786U	I_{DSS2}		0.25	mA
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 1.50\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 0.80\text{ A pulsed}$ 2N6782U 2N6784U 2N6786U	$r_{DS(on)1}$		0.60 1.50 3.60	Ω
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 3.50\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 1.25\text{ A pulsed}$ 2N6782U 2N6784U 2N6786U	$r_{DS(on)2}$		0.61 1.60 3.70	Ω
Static Drain-Source On-State Resistance $T_J = +125^\circ\text{C}$ $V_{GS} = 10\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 1.50\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 0.80\text{ A pulsed}$ 2N6782U 2N6784U 2N6786U	$r_{DS(on)3}$		1.08 2.81 7.92	Ω
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = 3.50\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 1.25\text{ A pulsed}$ 2N6782U 2N6784U 2N6786U	V_{SD}		1.5 1.5 1.4	V

ELECTRICAL CHARACTERISTICS @ $T_A = +25^\circ\text{C}$, unless otherwise noted (continued)
DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Gate Charge:				
On-State Gate Charge $V_{GS} = 10\text{ V}$, $I_D = 3.50\text{ A}$, $V_{DS} = 50\text{ V}$ 2N6782U $V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$, $V_{DS} = 100\text{ V}$ 2N6784U $V_{GS} = 10\text{ V}$, $I_D = 1.25\text{ A}$, $V_{DS} = 200\text{ V}$ 2N6786U	$Q_{g(on)}$		8.1 8.6 12	nC
Gate to Source Charge $V_{GS} = 10\text{ V}$, $I_D = 3.50\text{ A}$, $V_{DS} = 50\text{ V}$ 2N6782U $V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$, $V_{DS} = 100\text{ V}$ 2N6784U $V_{GS} = 10\text{ V}$, $I_D = 1.25\text{ A}$, $V_{DS} = 200\text{ V}$ 2N6786U	Q_{gs}		1.7 1.5 1.8	nC
Gate to Drain Charge $V_{GS} = 10\text{ V}$, $I_D = 3.50\text{ A}$, $V_{DS} = 50\text{ V}$ 2N6782U $V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$, $V_{DS} = 100\text{ V}$ 2N6784U $V_{GS} = 10\text{ V}$, $I_D = 1.25\text{ A}$, $V_{DS} = 200\text{ V}$ 2N6786U	Q_{gd}		4.5 5.5 7.6	nC

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-on delay time $I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 50\text{ V}$ 2N6782U $I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 100\text{ V}$ 2N6784U $I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 200\text{ V}$ 2N6786U	$t_{d(on)}$		15	ns
Rinse time $I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 50\text{ V}$ 2N6782U $I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 100\text{ V}$ 2N6784U $I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 200\text{ V}$ 2N6786U	t_r		25 20 20	ns
Turn-off delay time $I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 50\text{ V}$ 2N6782U $I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 100\text{ V}$ 2N6784U $I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 200\text{ V}$ 2N6786U	$t_{d(off)}$		25 30 35	ns
Fall time $I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 50\text{ V}$ 2N6782U $I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 100\text{ V}$ 2N6784U $I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\ \Omega$, $V_{DD} = 200\text{ V}$ 2N6786U	t_f		20 20 30	ns
Diode Reverse Recovery Time $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 50\text{ V}$, $I_F = 3.50\text{ A}$ 2N6782U $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 50\text{ V}$, $I_F = 2.25\text{ A}$ 2N6784U $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 50\text{ V}$, $I_F = 1.25\text{ A}$ 2N6786U	t_{rr}		180 350 540	ns

GRAPHS

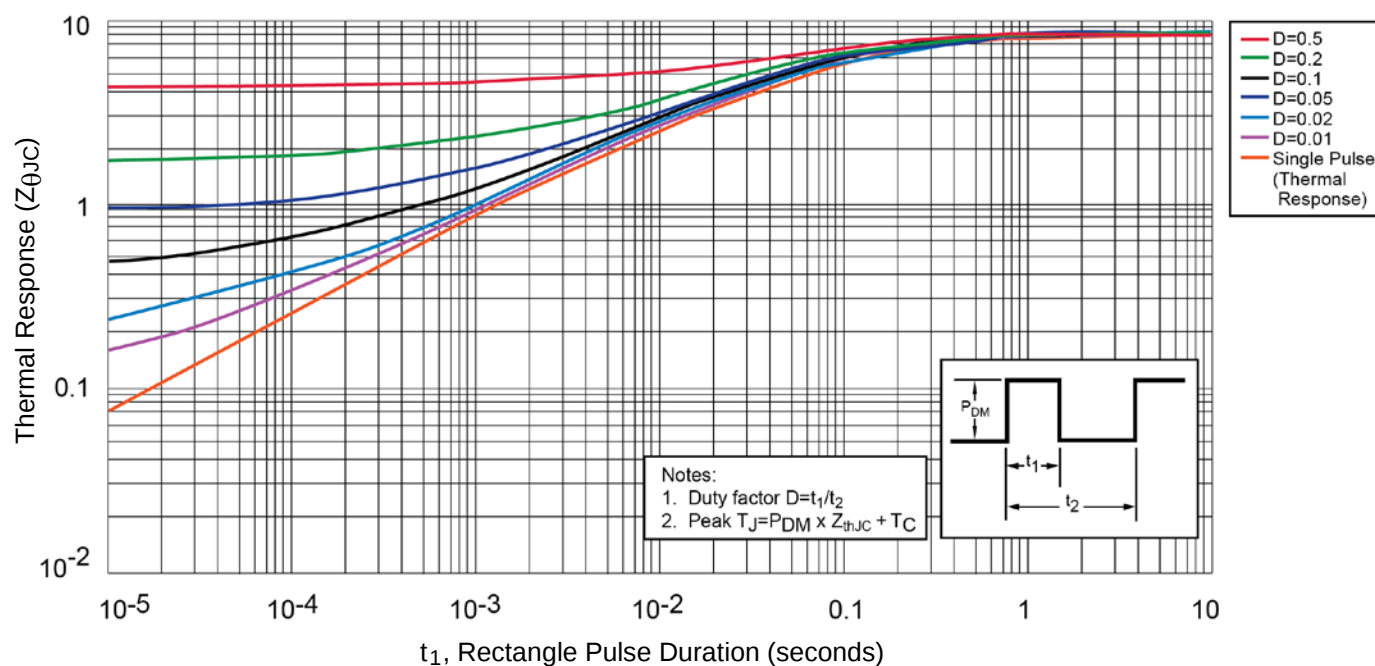
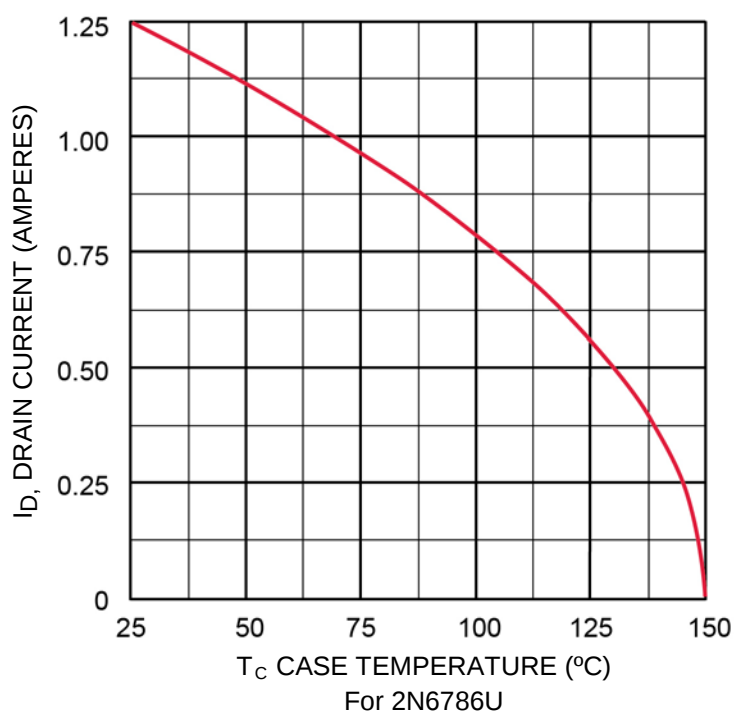
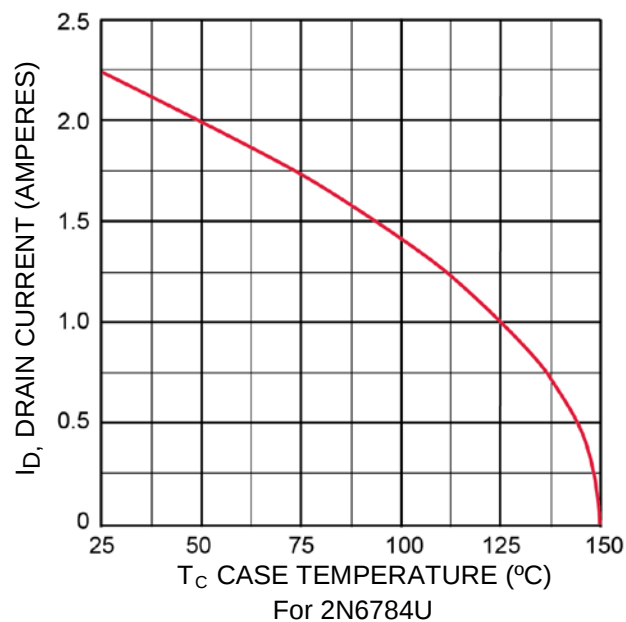
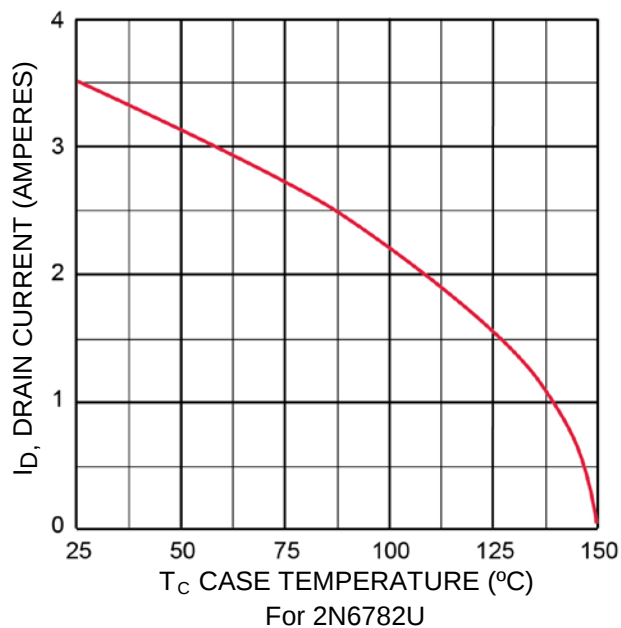
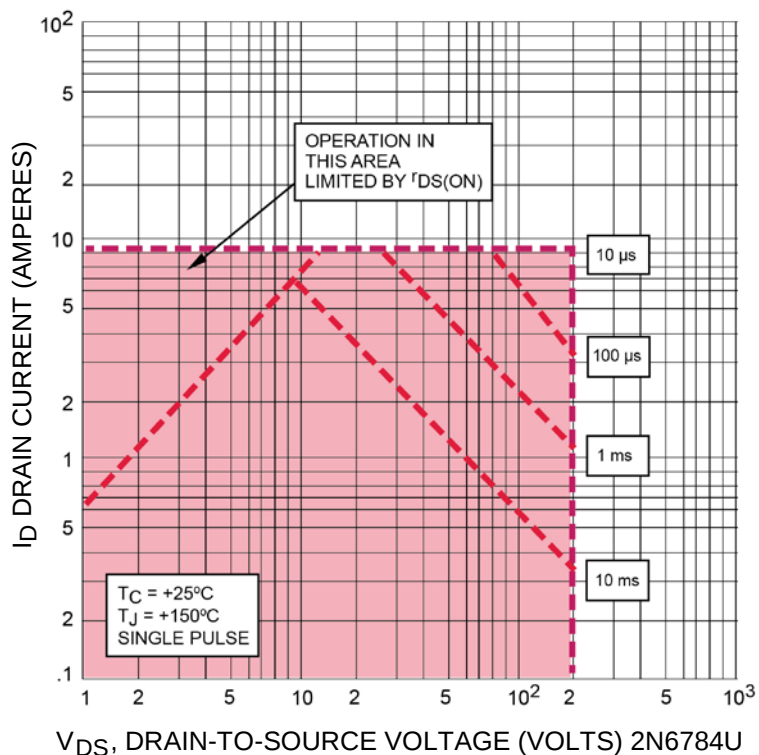
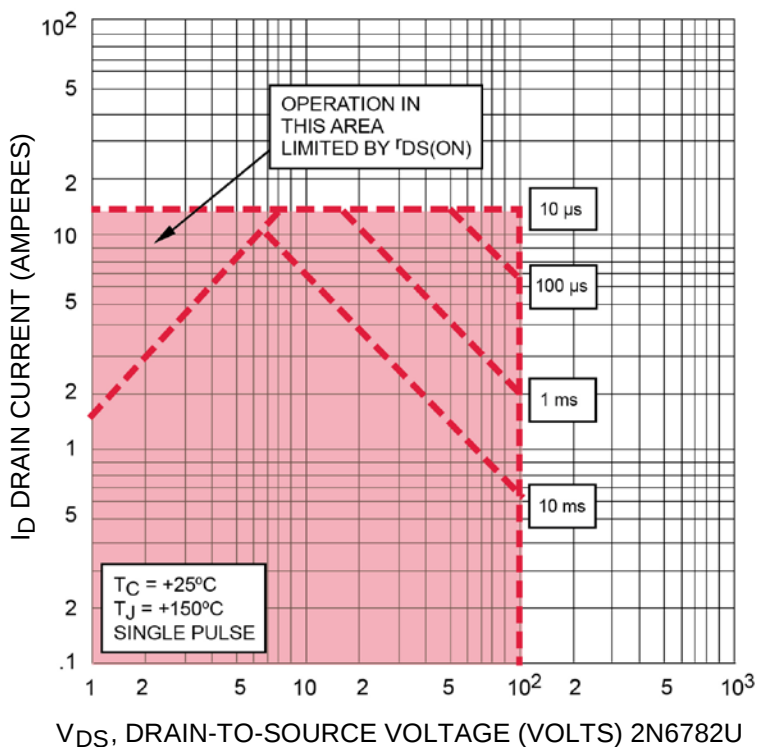


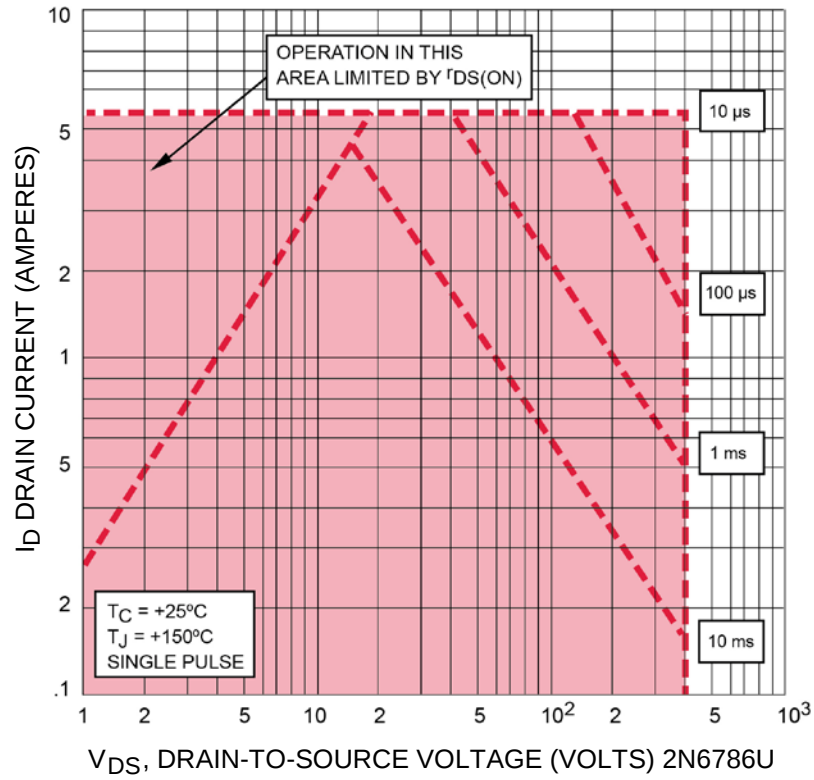
FIGURE 1
Thermal Response Curves

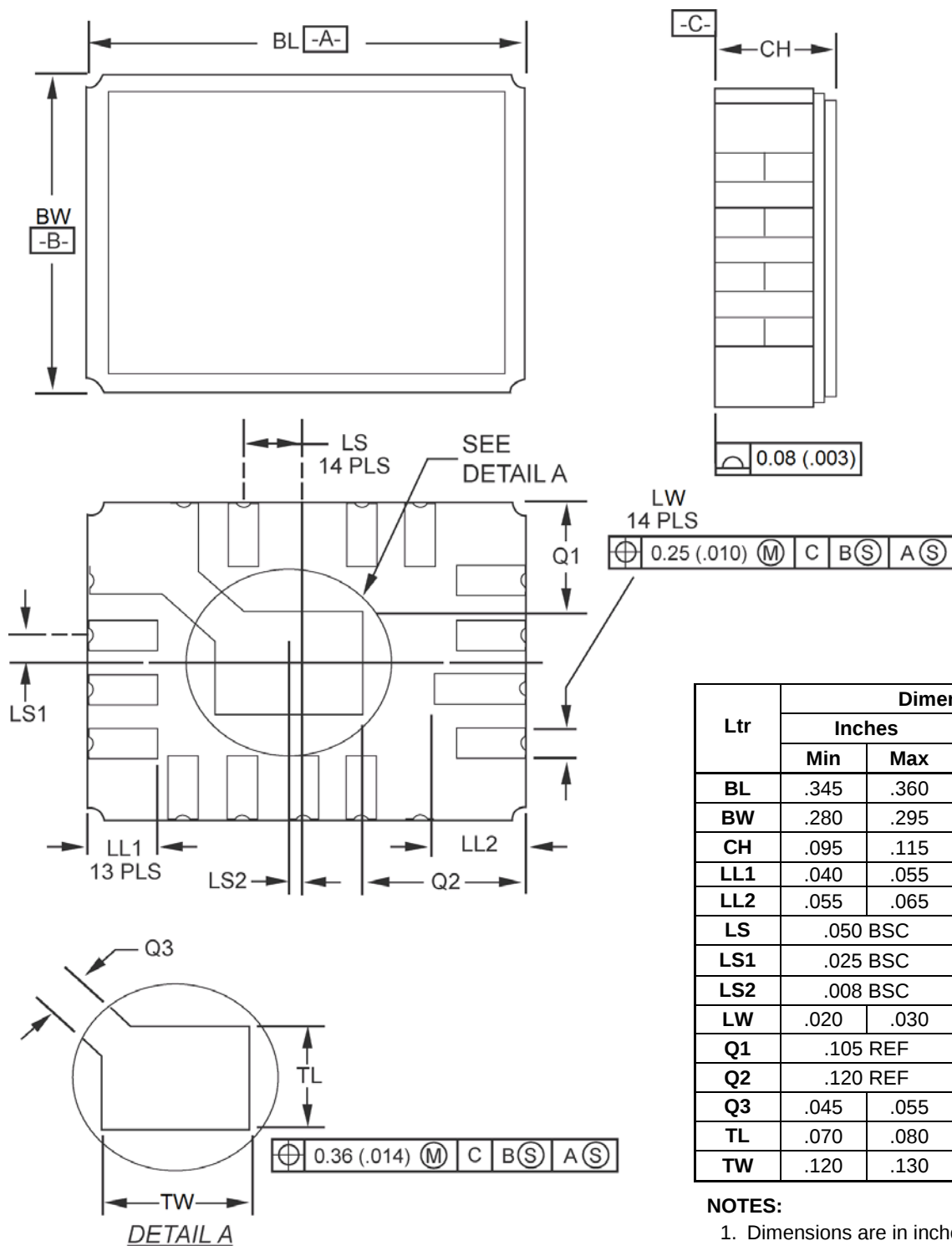
GRAPHS (continued)
FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs


GRAPHS (continued)
FIGURE 3 – Maximum Safe Operating Area


GRAPHS (continued)

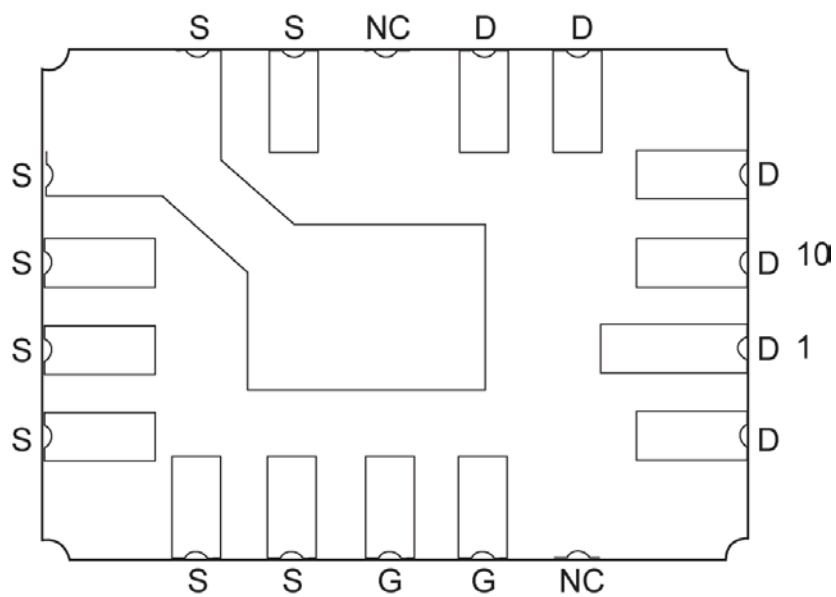
FIGURE 3 – Maximum Safe Operating Area



PACKAGE DIMENSIONS

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φ x symbology.
4. Ceramic package only.

PAD LAYOUT



PAD ASSIGNMENTS