CRD4525-Q1

2 x 15 W CS4525 Digital Amplifier Reference Design

Features

- Output Filters Optimized for 8 Ω Loads
- Delivers 15 W/Ch into 8 Ω at 0.5 % THD+N
- Single-Ended 2 V_{RMS} Stereo Analog Inputs
- Optical and Coaxial S/PDIF Inputs
- Demonstrates EMI Compliant Design per FCC Class B Part 15 and CISPR 22 Standards
- Flexible I/O Headers Provided
  - PCM Input Signal Interface
  - Auxiliary Serial Port Signal Interface
  - Delay Port Signal Interface
  - PWM Logic Level Signal Interface
- Optional CRD4412A Daughter-Card for Subwoofer Channel
  - Implements a 2.1 Configuration
- Demonstrates Recommended 4-Layer Layout and Grounding Arrangements
- +18 V Switching Mode Power Supply Included
- Can be operated by On-Board Controls or with Windows® Compatible Graphical User Interface

Description

The CRD4525-Q1 demonstrates the CS4525 digital PWM controller with integrated power stages. This reference design implements a two-channel amplifier that delivers 15 W per full-bridge channel into 8 Ω loads using a single +18 V supply. The CRD4525-Q1 is powered by an included 80 W switching mode power supply.

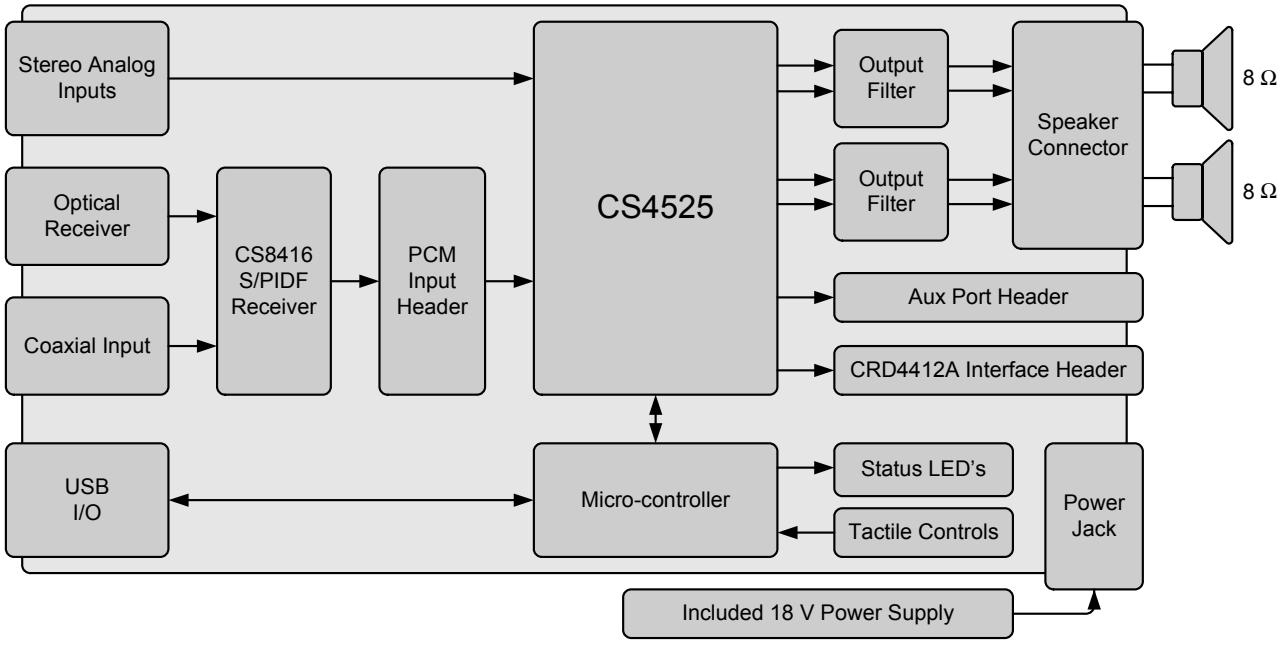
Standard RCA phono jacks are provided to easily interface analog input signals with the evaluation board. Optical and coaxial inputs are provided to interface with S/PDIF digital audio input signals.

The PWM audio power outputs are routed through an inductor/capacitor 2nd order low-pass filter (LPF) to remove high-frequency components from the output signal, effectively converting it from digital to analog.

The Windows software provides a GUI to make configuration of the CRD4525-Q1 easy. The software communicates through the PC's USB port to configure the control port registers so that all features of the CS4525 can be evaluated. Additionally, control over basic functions is possible via on-board hardware controls without the need to attach the CRD4525-Q1 to a PC.

ORDERING INFORMATION

CRD4525-Q1	CS4525 Reference Design



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1. SYSTEM OVERVIEW

The CRD4525-Q1 reference design is an excellent means for evaluating the CS4525 30 W digital amplifier with integrated ADC. Analog and digital audio input signal interfaces are provided; an on-board microcontroller and USB PC interface is used for easily configuring the CS4525's internal registers, and stand-alone mode is supported through on-board tactile controls.

The CRD4525-Q1 schematic set is shown in Figure 6 through Figure 8.

1.1 Power

A 80 W OEM switching-mode power supply is included to power the CRD4525-Q1. The power supply provides +18 V to the CS4525 power stages, and an on-board buck-converter and regulator provide power to the logic-level digital circuitry.

Power may be supplied from the included power supply or any 12-18 VDC power supply capable of delivering sufficient current for the intended power output. Connection for the power supply is provided in J3 (see the System Connections table on page 14).

1.2 CS4525 Digital Amplifier

A complete description of the CS4525 is included in the CS4525 product data sheet.

Optional user configuration settings of the CS4525 are provided through its control port registers, accessible through the CS4525 tab of the Cirrus Logic FlexGUI software. A register-level configuration interface is provided on the Register Maps tab. See the "PC Software Control" section on page 7 for more information.

1.3 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 8 on page 17) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data and clocks for the CS4525. The CS8416 operates in master mode and can provide PCM data in Left-Justified, I²S, Right-Justified 16-bit, and Right-Justified 24-bit interface formats.

The most common operations of the CS8416 may be controlled via the S/PDIF Input Controls tab in the GUI software application. Advanced options are accessible through the CS8416 sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software.

1.4 System Clocking

A 24.576 MHz parallel resonant crystal, Y1, is available to provide a clock source to the CS4525. The crystal is mounted in pin sockets, allowing easy removal or replacement. Alternatively, an input SYS_CLK signal can be provided on pin 3 of the serial audio input header (J2).

1.5 External Data Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J2, J4, and J11. Figure 6 shows the headers' electrical connections.

The 12-pin, 3 column header, J2, provides access to the CS4525's serial audio input and SYS_CLK input signals. Place shunts across the SCLK, LRCK, and SDIN pins located in the columns labeled "S/PDIF" to connect to the on-board S/PDIF digital interface receiver circuitry. To use an external digital audio source, simply remove the shunts and connect a ribbon across the SCLK, LRCK, and SDIN pins located in the col-

umns labeled “EXT SAI”. A single ground column for the ribbon cable’s ground connection is provided to maintain signal integrity.

The 8-pin, 2 column header, J11, provides access to the CS4525’s auxiliary serial audio port output signals, as well as the SYS_CLK output signal. A single ground column is provided to maintain signal integrity.

The 20-pin, 2 column header, J4, is included to interface with a CRD4412A card. Various signals, power, and ground are presented on this header. Notably, this header includes the DLY_SDOUT and DLY_SDIN signals which can be used to interface with an external delay device or DSP. See Figure 6 for complete connectivity information.

1.6 Analog Inputs

RCA connectors supply the CS4525 analog inputs through single-ended passive circuits with one pole of input filtering. A resistive attenuation network is implemented to allow 2 V_{RMS} input levels to be supplied to the CRD4525-Q1. Refer to the CS4525 data sheet for the maximum input signal level at the analog input pins.

1.7 Speaker Outputs

The CS4525 power outputs are configured for stereo full-bridge operation. The outputs are routed through a 2nd order low-pass filter to remove high-frequency content from the output signals and then presented at the speaker wire crimp terminals (J5). The output filters are optimized for 8 Ω speaker loads. The speaker terminal connections are shown below.

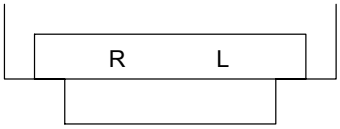


Figure 1. Speaker Terminal Configuration

1.8 PC Control

A USB connection is provided to facilitate software control of the CS4525’s internal registers.

A graphical user interface is available for the CRD4525-Q1 to allow easy manipulation of the CS4525’s internal registers. See the CS4525 data sheet for complete internal register descriptions.

To enable the CRD4525-Q1, simply connect the supplied USB cable from an available USB port on a PC to the USB connector (J37) and launch the Cirrus Logic FlexGUI software.

A visual indicator is provided by an on-board LED (D12) that illuminates when the board is being operated under PC control. When operating under PC Control, the stand-alone controls on the board should not be manipulated.

Refer to “PC Software Control” on page 7 for a description of the Graphical User Interface (GUI).

1.9 Stand-Alone Control

A volume control knob (S1), reset button (S2), and mute button (S3) are included for stand-alone operation of the CRD4525-Q1. These controls were not supported by early versions of firmware running on the CRD4525-Q1, so it may be necessary to upgrade older firmware versions to enable their functionality.

The on-board firmware can be upgraded by downloading and running the most recent version of the Cirrus Logic FlexGUI application. If necessary, this application (downloadable at www.cirrus.com/msasoftware) will automatically upgrade the firmware for an attached CRD4525-Q1 upon start-up.

1.10 External Power Stage Interface

A keyed connector (J4) is included to interface with the CRD4412A. The CRD4525-Q1 can be used with or without a CRD4412A attached.

Without the CRD4412A attached, the CRD4525-Q1 configures itself for 2-channel stereo full-bridge operation. When the CRD4412A is attached, the CS4525 enables its bass manager and routes the LFE channel to the CRD4412A which amplifies the signal in mono parallel full-bridge mode. Together, the CRD4525-Q1 and CRD4412A implement a 2.1 configuration.

The CRD4412A must be inserted and removed while power is not applied to the CRD4525-Q1.

2. PC SOFTWARE CONTROL

The CRD4525-Q1 is designed for use with the Microsoft® Windows-based FlexGUI graphical user interface. This interface provides comprehensive control over the CS4525's internal registers via a PC's USB port.

The FlexGUI software may be downloaded and installed from www.cirrus.com/msasoftware.

Step-by-step instructions for using the FlexGUI are provided as follows:

1. Download and install the FlexGUI software from www.cirrus.com/msasoftware.
2. Connect the CRD4525-Q1 to a host PC using the supplied USB cable.
3. Connect load speakers to the speaker output terminals.
4. Connect an input source to the S/PDIF or analog input connectors.
5. Plug the input to the included +18 V power supply into an available power outlet.
6. Plug the output of the included +18 V power supply into the power input connector on the CRD4525-Q1.
7. Launch the FlexGUI software. *The GUI will load and be displayed.*
8. Un-check the "Power Down CS4525" checkbox to power-up the device. *In this state, the CRD*4525-Q1 *will convert and amplify the content present on the optical S/PDIF input.*

2.1 CS4525 Main Controls Tab

The CS4525 Main Controls tab provides a high-level, intuitive interface to many of the basic configuration options of the CS4525. Use this tab to access functions such as power-down, input source, and volume control.

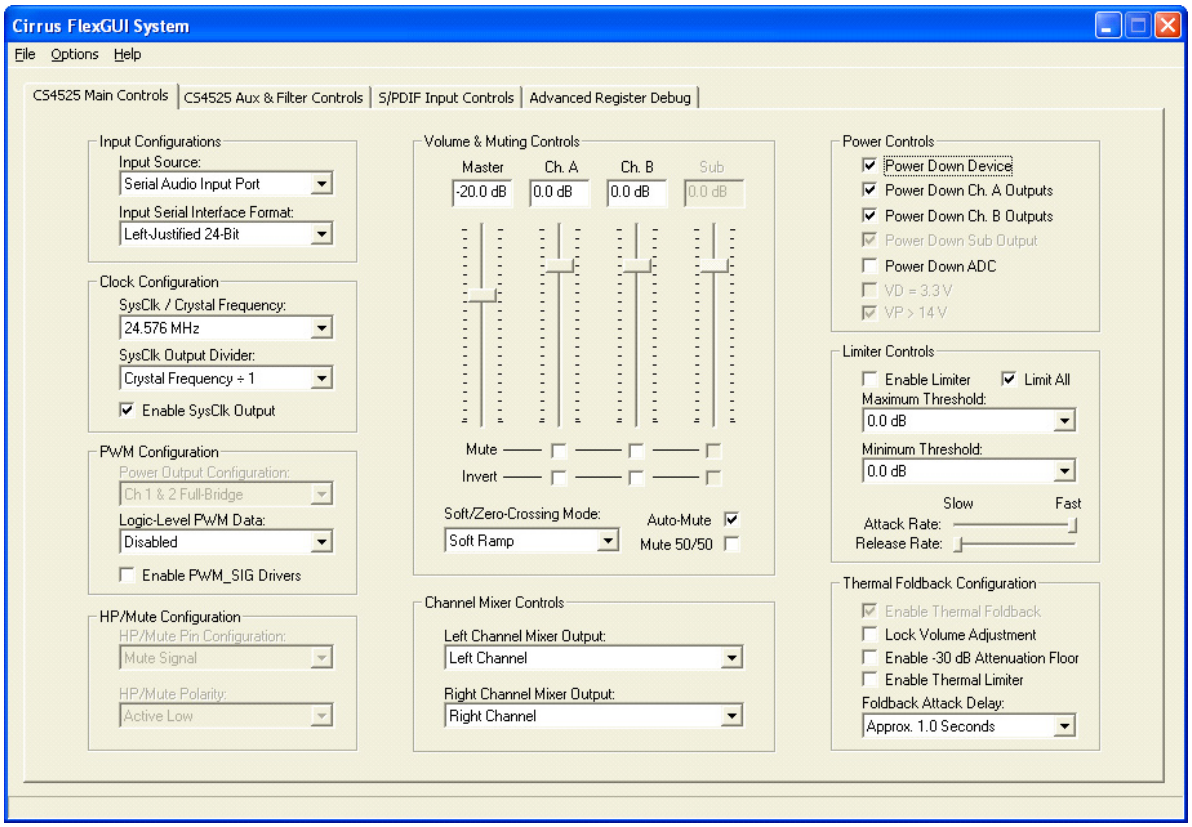


Figure 2. CS4525 Main Controls Tab

2.2 CS4525 Aux & Filter Controls Tab

The CS4525 Aux & Filter Controls tab provides a high-level, intuitive interface to many of the advanced configuration options of the CS4525. Use this tab to configure the auxiliary port, the internal filters, and advanced PWM adjustments. Control over device and board resets is also provided.

The CS4525 Parametric EQ Filter Wizard, available for download from the CS4525 product page at www.cirrus.com, provides a graphical interface to the Parametric Equalization, Bass Manager, and Tone Control features of the CS4525. Using this utility, the user can graphically configure any or all of the five on-chip bi-quad filters, the Bass Manager crossover frequency, and the bass/treble shelving filters available in the CS4525.

This utility creates a script file which can be loaded into the CS4525 utilizing the FlexGUI interface. Please refer to Cirrus Logic application note AN303 for more information regarding this valuable tool.

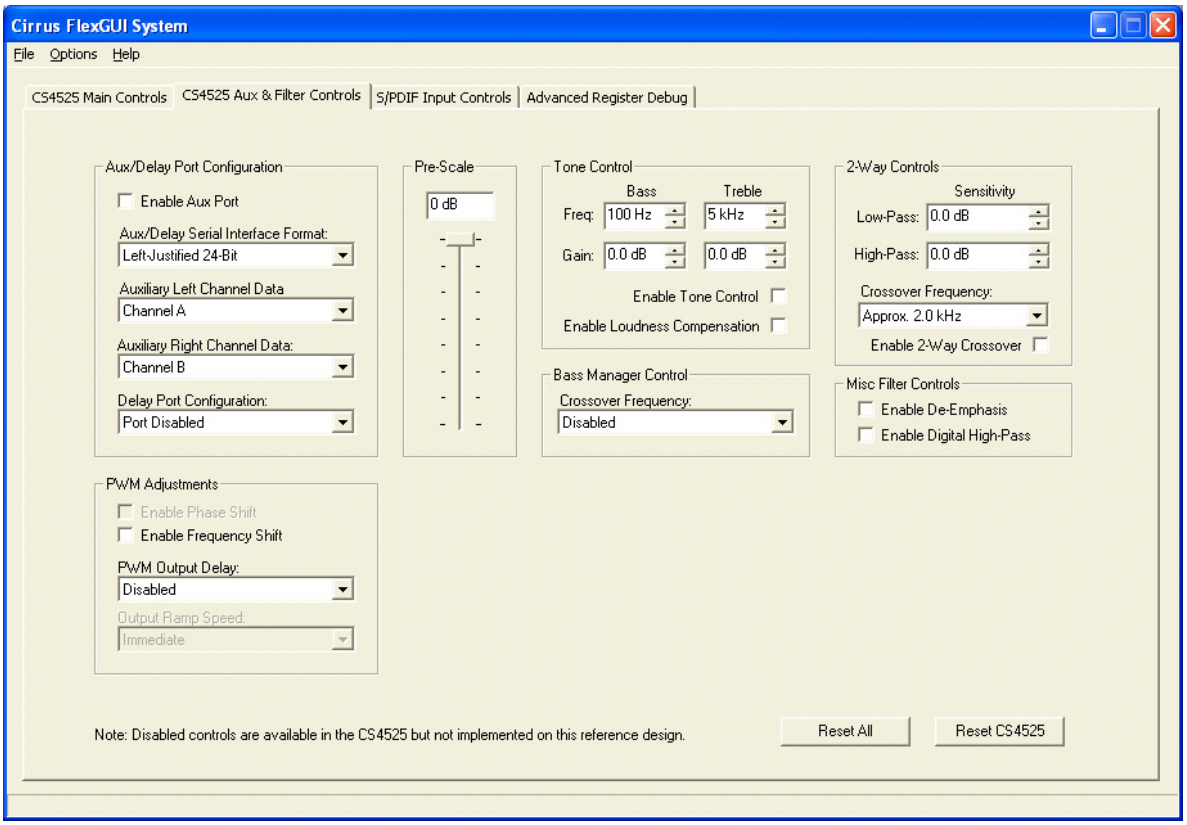


Figure 3. CS4525 Aux & Filter Controls Tab

2.3 S/PDIF Input Controls Tab

When the CRD4525-Q1 is configured to make use of the CS8416 S/PDIF receiver, the devices must be configured for proper operation. The S/PDIF Input Controls tab provides a high-level, intuitive interface to the most common configuration options of the CS8416.

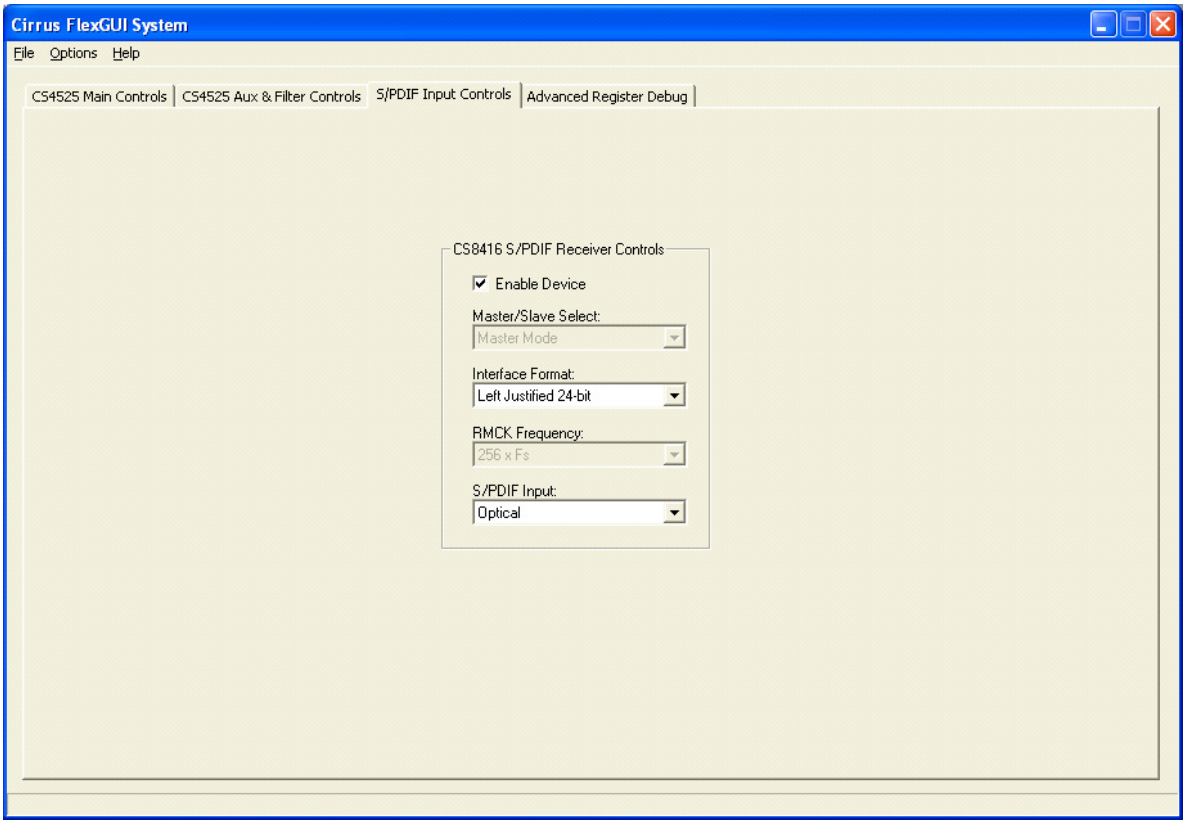
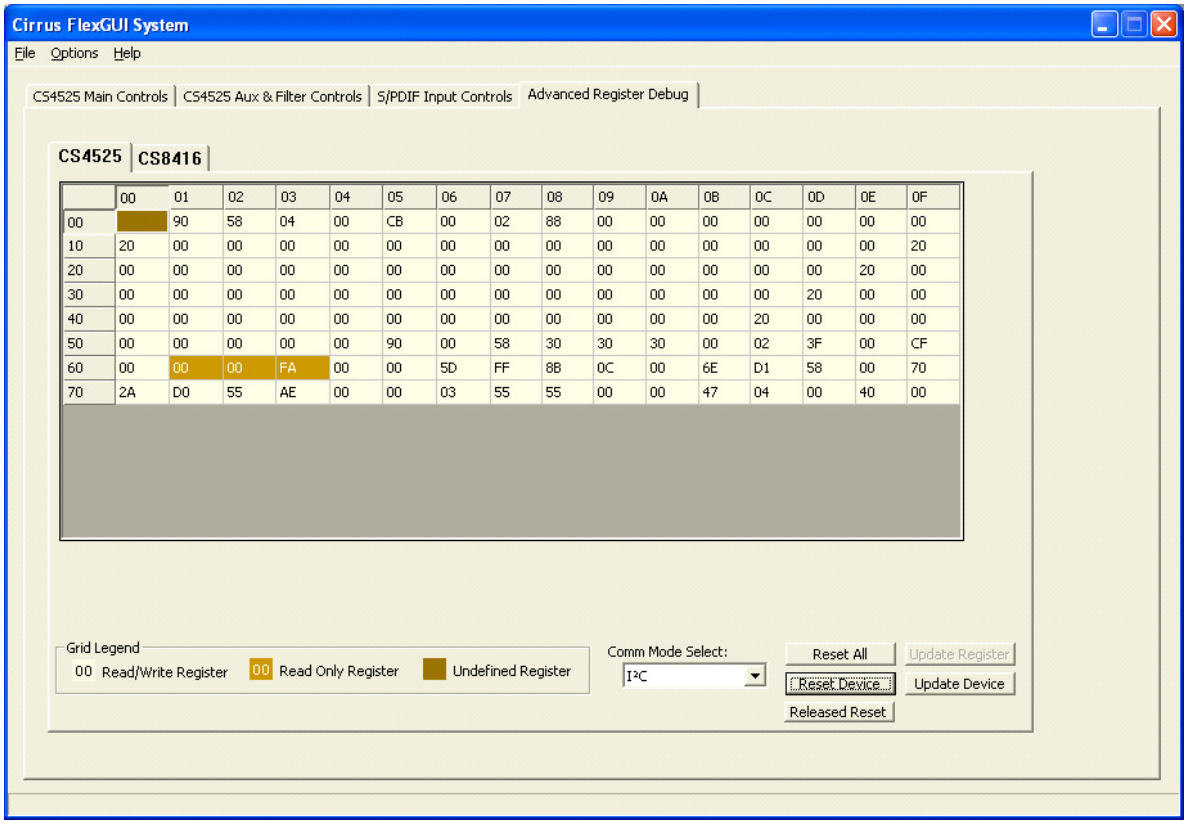


Figure 4. S/PDIF Input Controls Tab

2.4 Register Maps Tab

The Register Maps tab provides an easy register-level interface to the on-board devices. Register values can be modified on a bit-wise or byte-wise basis. To modify a single bit, first select the register by clicking its position in the register matrix; then click the appropriate push-button for the desired bit. To modify an entire register, simply enter the register's new value directly into the register matrix.

Within the Register Maps tab, the CS4525 tab is used to access the CS4525's internal registers, and the CS8416 tab is used to access the CS8416's internal registers.



	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00		90	58	04	00	CB	00	02	88	00	00	00	00	00	00	00
10	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	20
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	20	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	20	00	00
40	00	00	00	00	00	00	00	00	00	00	00	00	20	00	00	00
50	00	00	00	00	00	90	00	58	30	30	30	00	02	3F	00	CF
60	00	00	00	FA	00	00	5D	FF	8B	0C	00	6E	D1	58	00	70
70	2A	D0	55	AE	00	00	03	55	55	00	00	47	04	00	40	00

Figure 5. Register Maps Tab

2.5 Pre-Configured Script Files

Pre-configured script files are provided with the CRD4525-Q1 to allow easy initial board bring-up. The board configurations stored within these files are described in Sections 2.5.1 - 2.5.3.

2.5.1 Analog In

Using the pre-configured script file named “Analog In.fgs”, an analog input signal applied to the analog inputs of the CRD4525-Q1 will be used as the CS4525’s input source. The device will be powered up with no internal processing active and the master volume control set to -20 dB.

2.5.2 Optical SPDIF In

Using the pre-configured script file named “Optical SPDIF In.fgs”, the optical S/PDIF input signal will be received by the CS8416 S/PDIF receiver. The CS8416 PCM output signals will be used as the CS4525’s input source. The device will be powered up with no internal processing active and the master volume control set to -20 dB.

2.5.3 Coaxial SPDIF In

Using the pre-configured script file named “Coaxial SPDIF In.fgs”, the coaxial S/PDIF input signal will be received by the CS8416 S/PDIF receiver. The CS8416 PCM output signals will be used as the CS4525’s input source. The device will be powered up with no internal processing active and the master volume control set to -20 dB.

3. STAND-ALONE MODE CONTROL

The CRD4525-Q1 is capable of operation without being connected to a computer by operating in stand-alone mode. When in this mode, the board is controlled by on-board hardware controls detailed in Table 2 on page 14.The rotary volume control on the edge of the board controls the volume. Tapping the mute button mutes/un-mutes the PWM outputs of the CS4525.

When a valid SPDIF signal is not present, the CS4525 is automatically configured to amplify the audio signal present on the RCA analog input connectors. When a valid SPDIF signal is present, the CS4525 is automatically configured to amplify the audio signal present in the SPDIF stream. Holding down the mute button for three seconds switches between optical SPDIF input and coaxial SPDIF input.

4. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4525 requires careful attention to power supply and grounding arrangements to optimize performance and heat dissipation and minimize radiated emissions. Figure 9 on page 18 shows the component placement. Figure 11 on page 20 shows the top layout. Figure 13 on page 22 shows the bottom layout. The decoupling capacitors are located as close to the CS4525 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

4.1 Power Supply Decoupling

Proper power supply decoupling is one key to maximizing the performance of a Class-D amplifier. Because the design uses an open loop output stage, noise on the power supply rail will be coupled to the output. Careful decoupling of the power stage supply rails is essential. Figure 9 on page 18 demonstrates good decoupling capacitor placement. Notice that the small value decoupling capacitors are placed as close as physically possible to the power pins of the CS4525. The ground side of the capacitors is connected directly to top side ground plane, which is also used by the power supply return pins. This keeps the high frequency current loop small to minimize power supply variations and EMI. 470 µF electrolytic capacitors are also located in close proximity to the power supply pins to supply the current locally for each channel. These are not required to be expensive low-ESR capacitors. General-purpose electrolytic capacitors that are specified to handle the ripple current can be used.

4.2 Electromagnetic Interference (EMI)

The EMI challenges that face a maker of Class-D amplifiers are largely the same challenges that have been faced by the switch mode power supply industry for many years. The numerous EMI consulting firms that have arisen and the many books that have been written on the subject indicate the scope of potential problems and available solutions. They should be considered a resource - most makers of switch mode equipment would benefit from developing a working relationship with a qualified EMI lab and from bringing their experience to bear on design issues, preferably early in the design process.

This reference design is a board-level solution which is meant to control emissions by minimizing and suppressing them at the source, in contrast to containing them in an enclosure.

The EMI requirements for an amplifier have added dimensions beyond those imposed on power supplies. Audio amplifiers are usually located in close proximity to radio receivers, particularly AM receivers which are notoriously sensitive to interference. Amplifiers also need to operate with speaker leads of unpredictable length and construction which makes it possible for any high-frequency currents that appear on the outputs to generate nuisance emissions.

For more detailed information regarding the EMI performance of the CRD4525-Q1, please refer to Section 10. “Electromagnetic Compliance” on page 30.

4.2.1 Suppression of EMI at the Source

Several techniques are used in the circuit design and board layout to minimize high frequency fields in the immediate vicinity of the high power components. Specific techniques include the following:

- As mentioned in Section 4.1, effective power supply decoupling of high-frequency currents and minimizing the loop area of the decoupling loop is one aspect of minimizing EMI.
- Each output of the CS4525 includes “snubbing” components. For example, OUT1 includes snubber components R24 (5.62 Ω) and C23 (680 pF). These components serve to damp ringing on the switching outputs in the 30-50 MHz range. The snubbing components should be as close as practical to the output pins to maximize their effectiveness.
- A separate ground plane with a solid electrical connection to the chassis, and which surrounds the speaker output connector, should be implemented. This allows the speaker outputs to be RF decoupled to the chassis just before they exit the chassis from the speaker connector.
- Make use of source termination resistors on all digital signals whose traces are longer than about 25 mm.

5. SYSTEM CONNECTIONS & JUMPERS

Connector Name	Reference Designator	Signal Direction	Connector Function
Power In	J3	Input	Power Connector. 12 to 18 VDC
Left In Right In	J1 J10	Input	Analog input to CS4525
S/PIDF Input	J6	Input	Coaxial digital input to CS8416
S/PIDF Input	J7	Input	Optical digital input to CS8416
Speaker Connector	J5	Output	Analog output from CS4525
USB	J8	Input/Output	USB connection to PC for software control
C2	J9	Input/Output	Connection for programming the on-board microcontroller (U3)

Table 1. System Connections

Control Name	Reference Designator	Tactile Control Function
Master Volume	S1	Controls settings of the volume control register
Board Reset	S2	Resets all devices in system
Mute	S3	Sets outputs of CS4525 to 50/50 duty cycle mute

Table 2. On-Board Tactile Controls

Connector Name	Reference Designator	Header Function
DSP IN	J2	When shunts are placed across column 1 and 2, the CS4525 serial audio input data is sourced by the CS8416 To use external serial audio input data, connect the PCM source cable across column 2 and 3
DSP OUT	J11	Auxiliary serial audio data from the CS4525
CRD4412 I/F	J4	Connection to CRD4412A daughter card

Table 3. System Headers

6. CRD SCHEMATICS

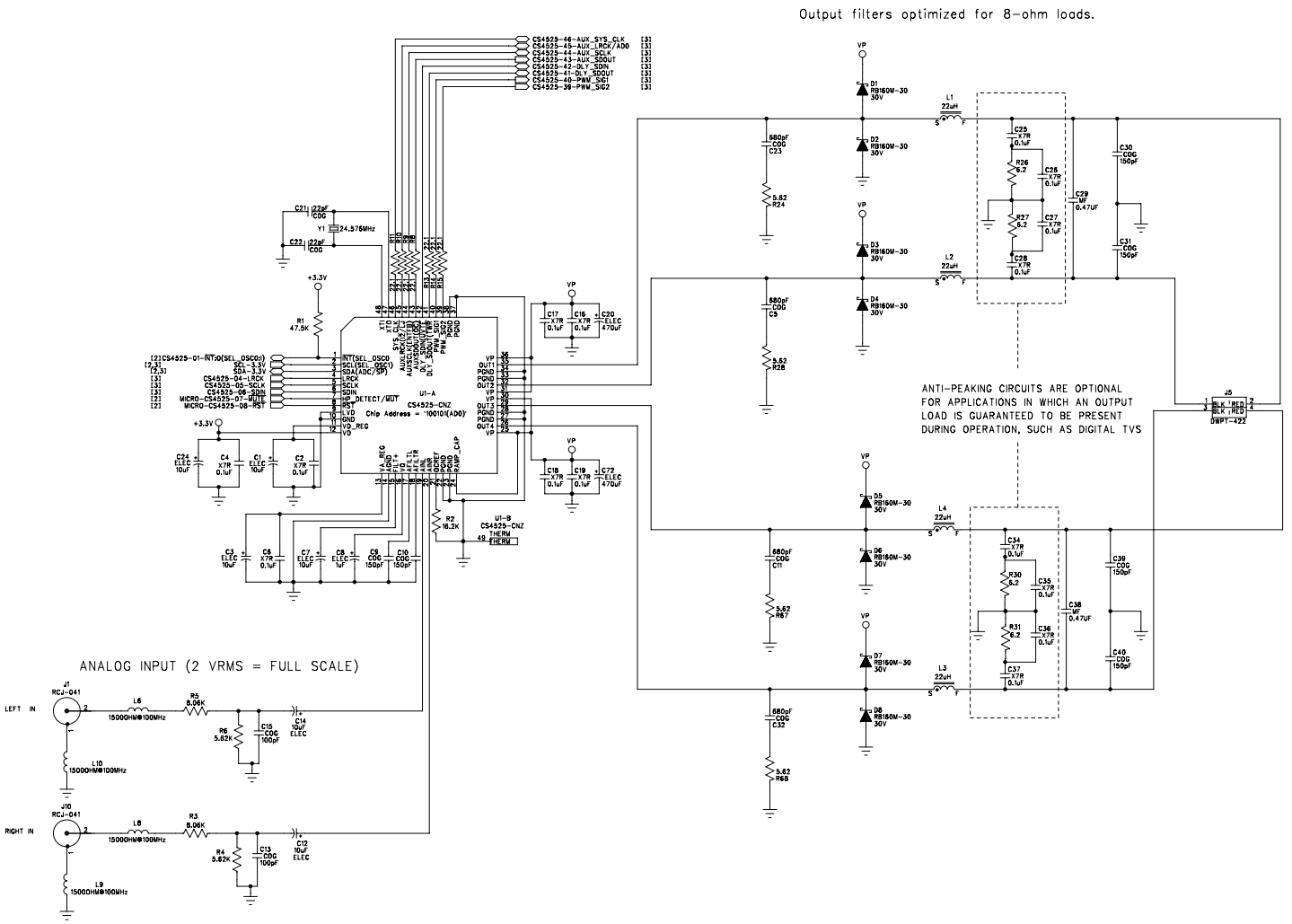


Figure 6. CS4525 - Schematic Page 1

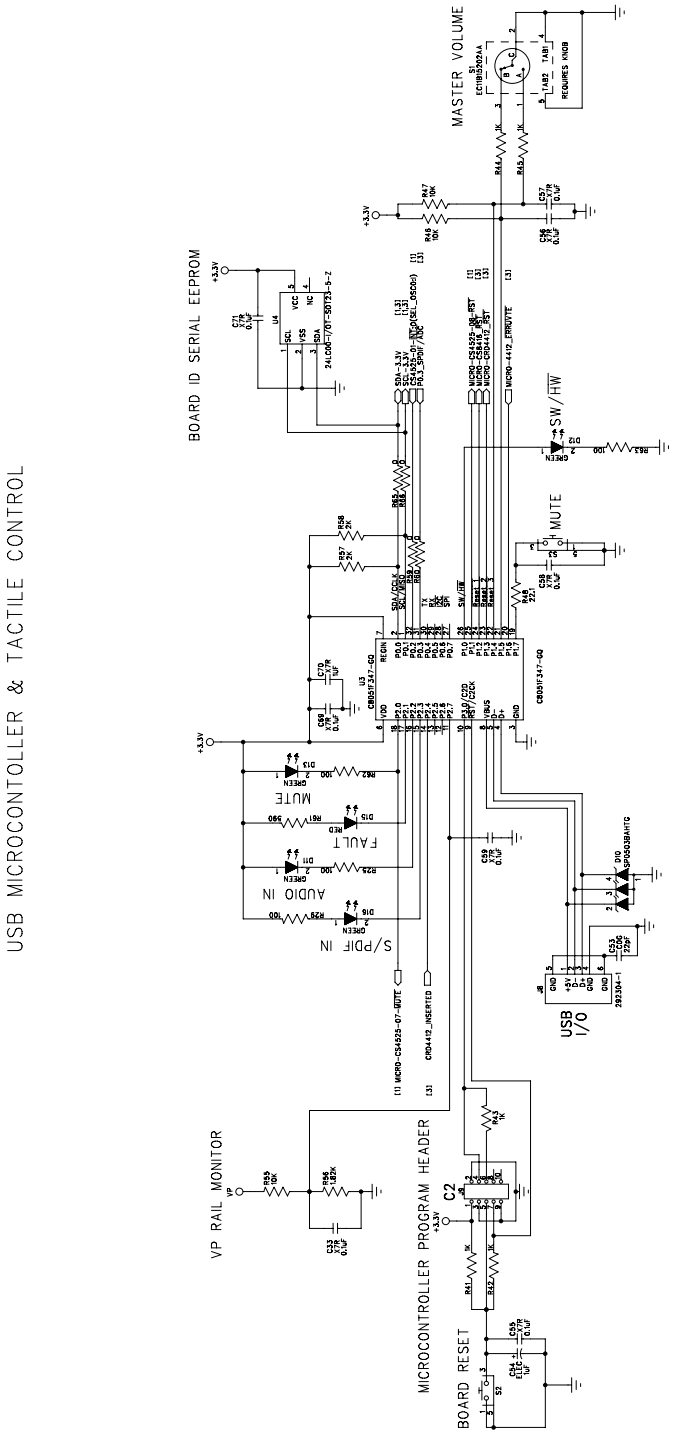


Figure 7. USB Microcontroller & Tactile Control - Schematic Page 2

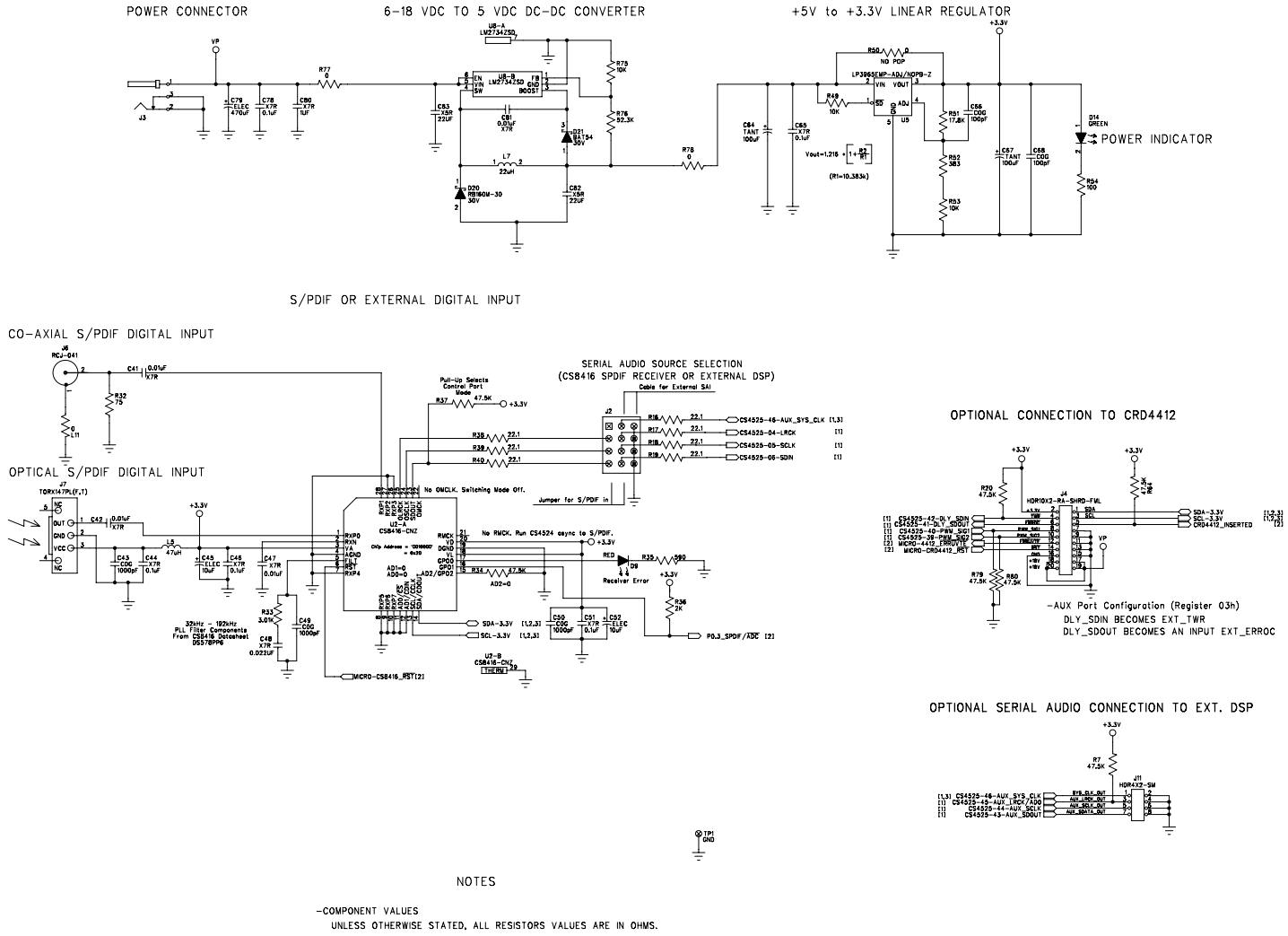


Figure 8. Power & I/O Connections - Schematic Page 3

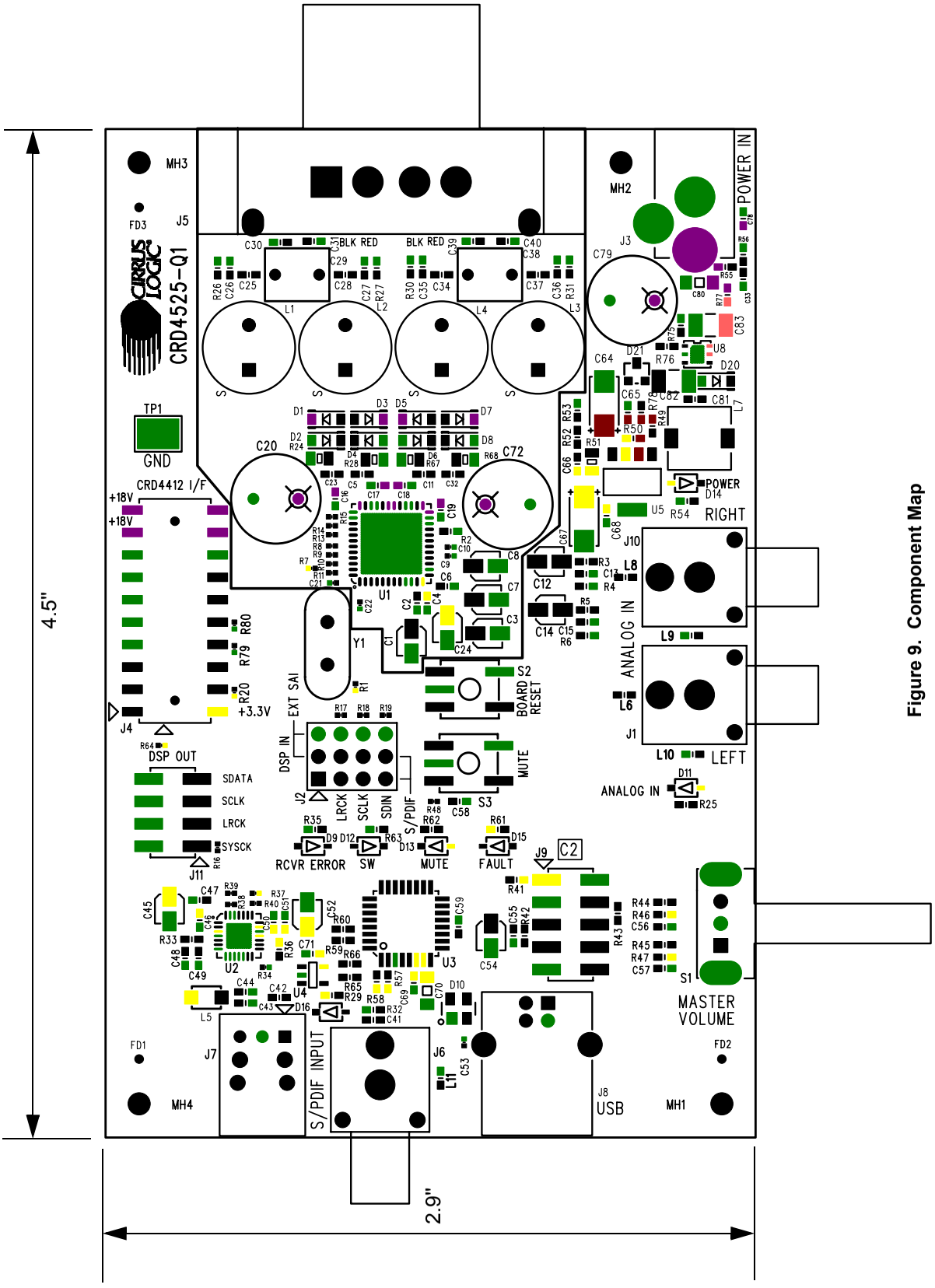


Figure 9. Component Map

7. CRD LAYOUT

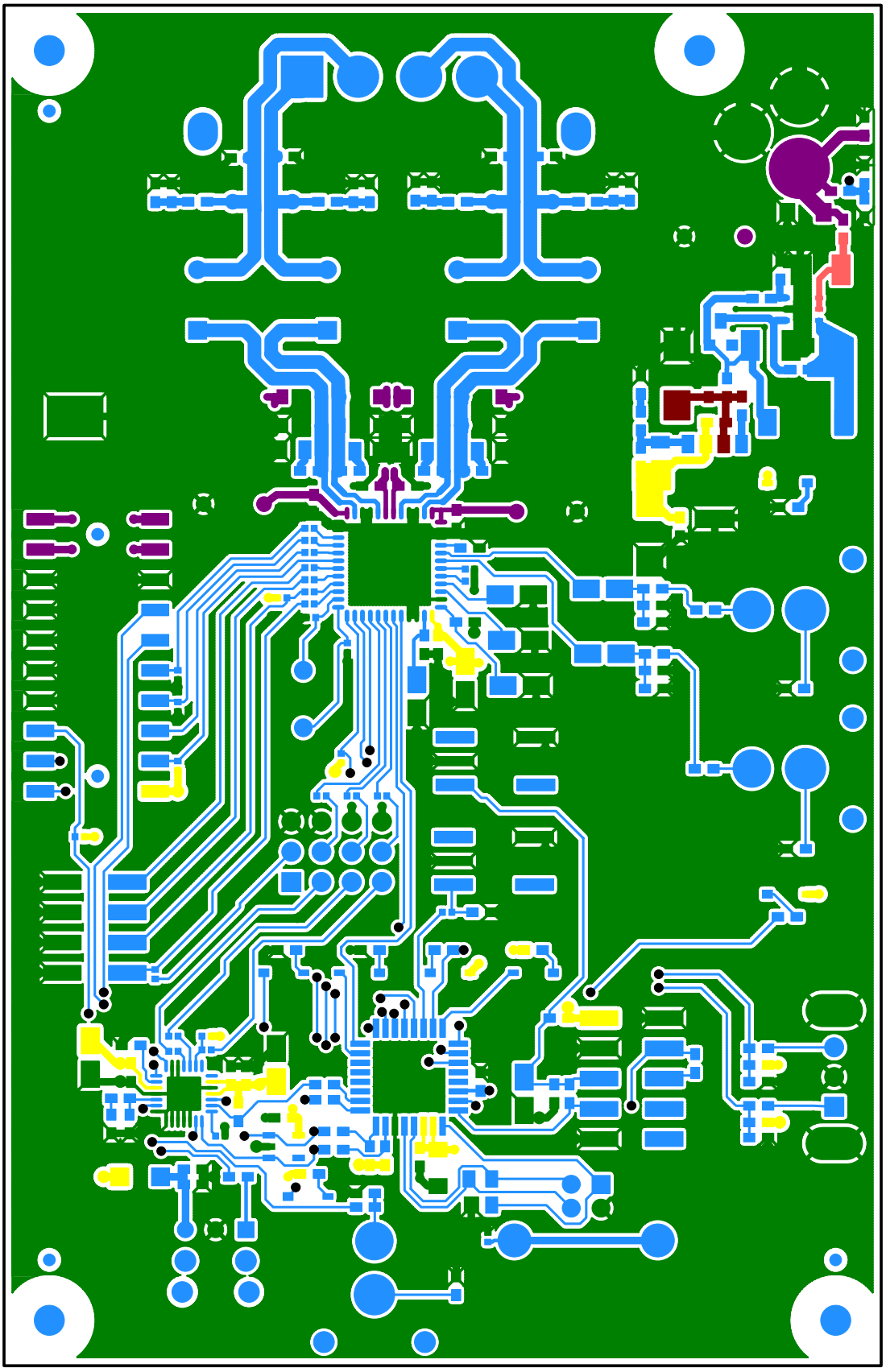


Figure 10. Top-Side Copper Layer

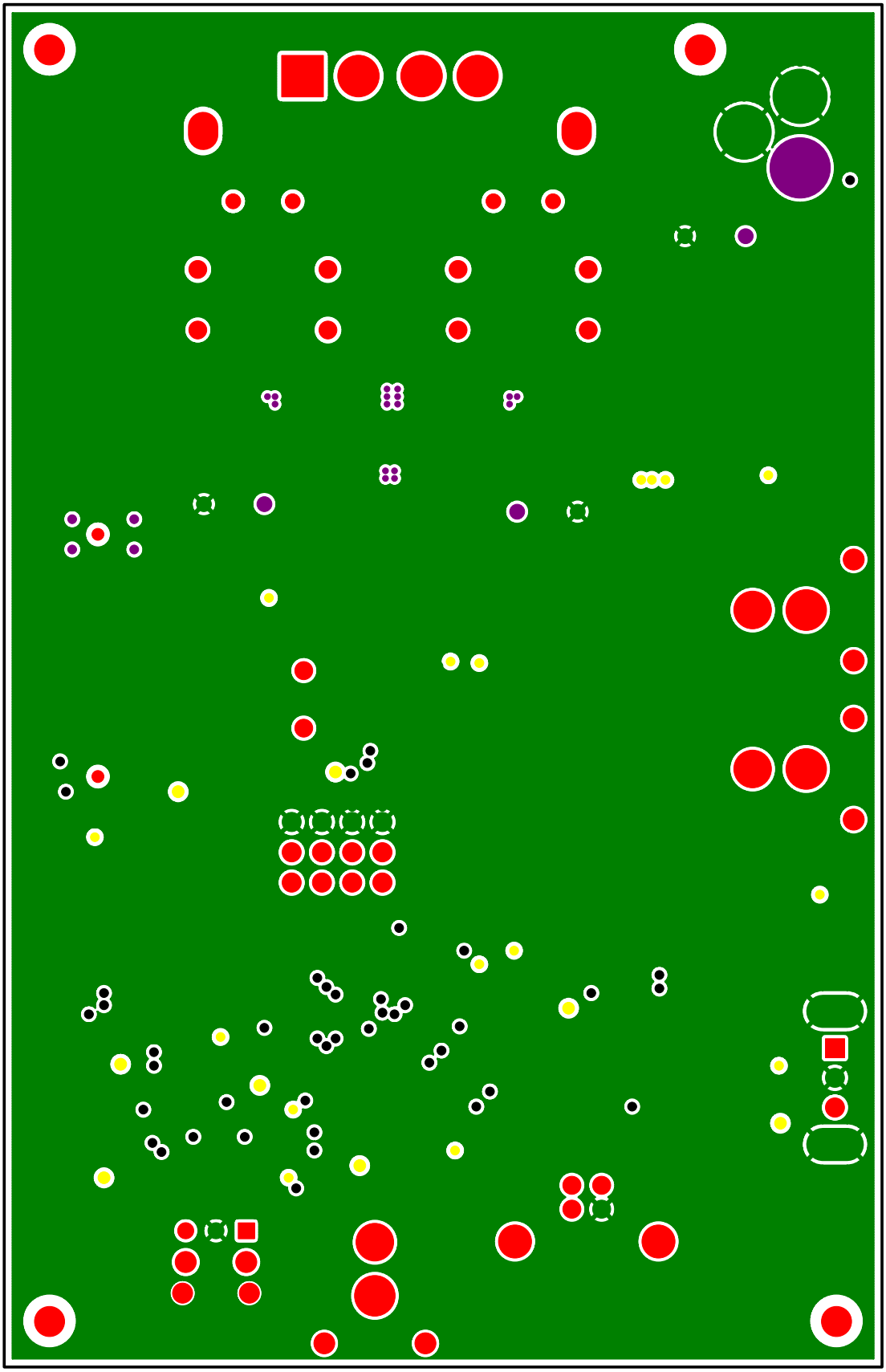


Figure 11. Inner Copper Layer 1

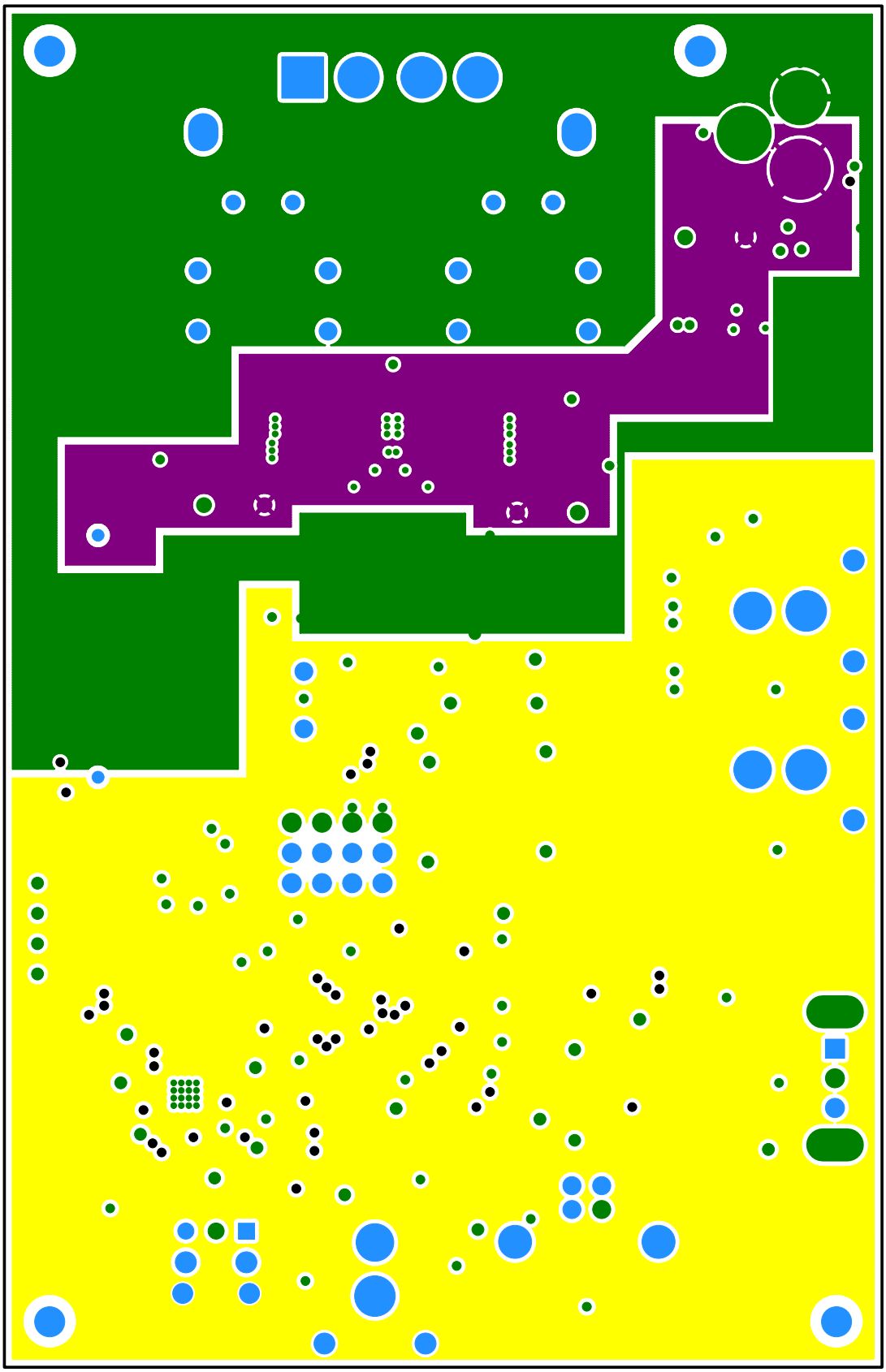


Figure 12. Inner Copper Layer 2

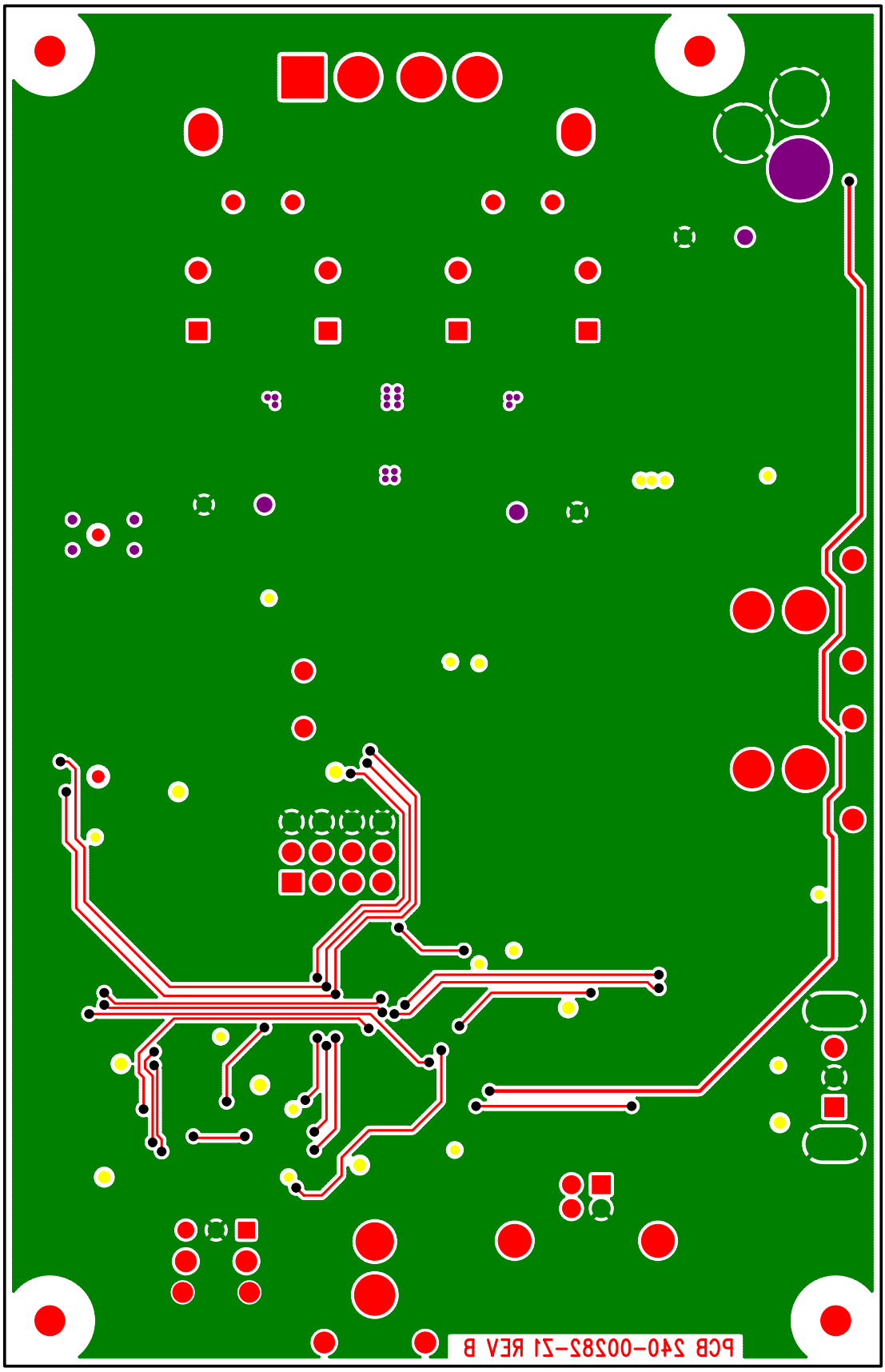


Figure 13. Bottom-Side Copper Layer

8. PERFORMANCE PLOTS

Unless otherwise stated, all measurements taken utilizing digital optical input at 1 kHz. Both channels were driven into 8 Ω resistive loads, and an AES-17 20 Hz to 20 kHz filter was enabled during testing.

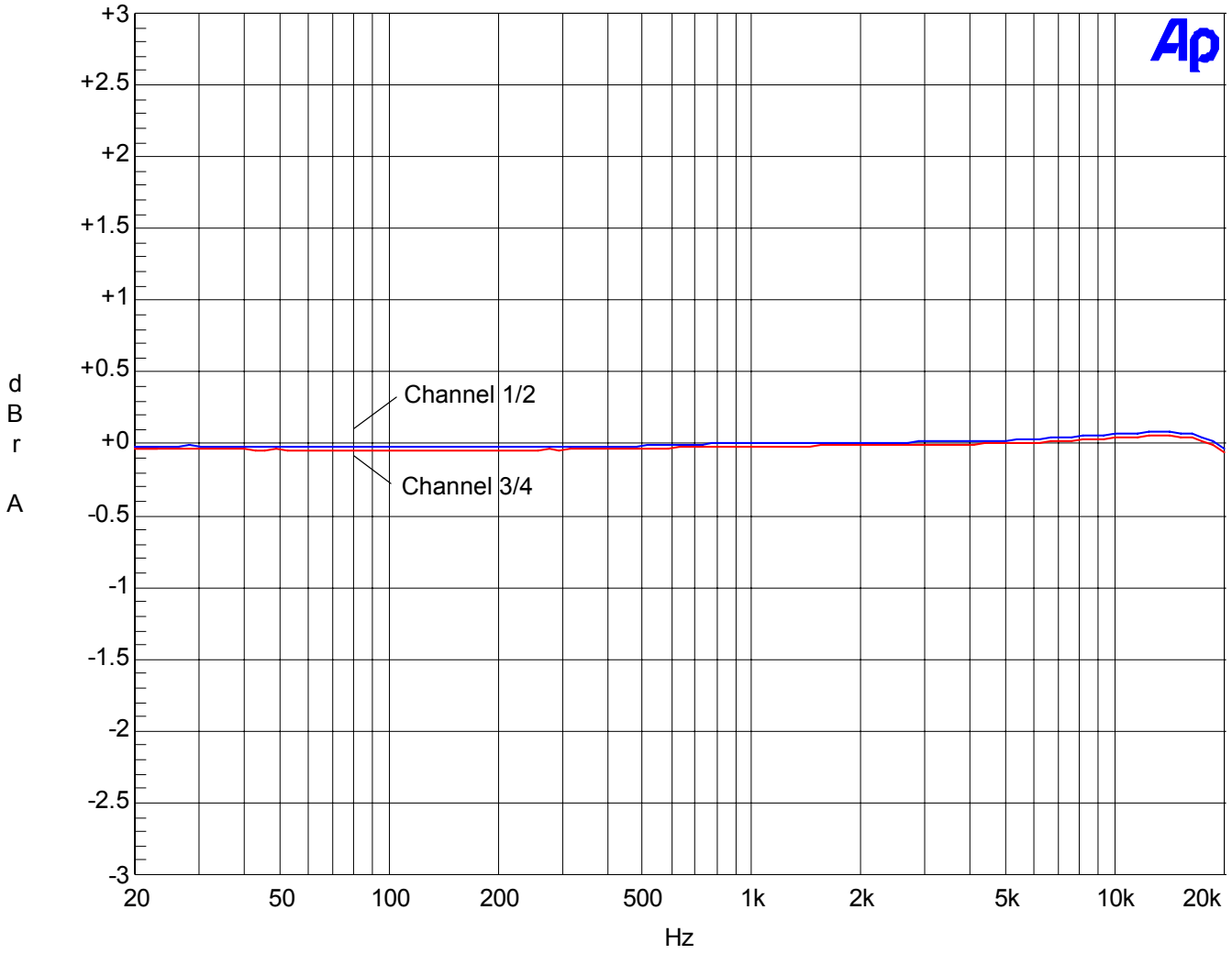


Figure 14. Frequency Response

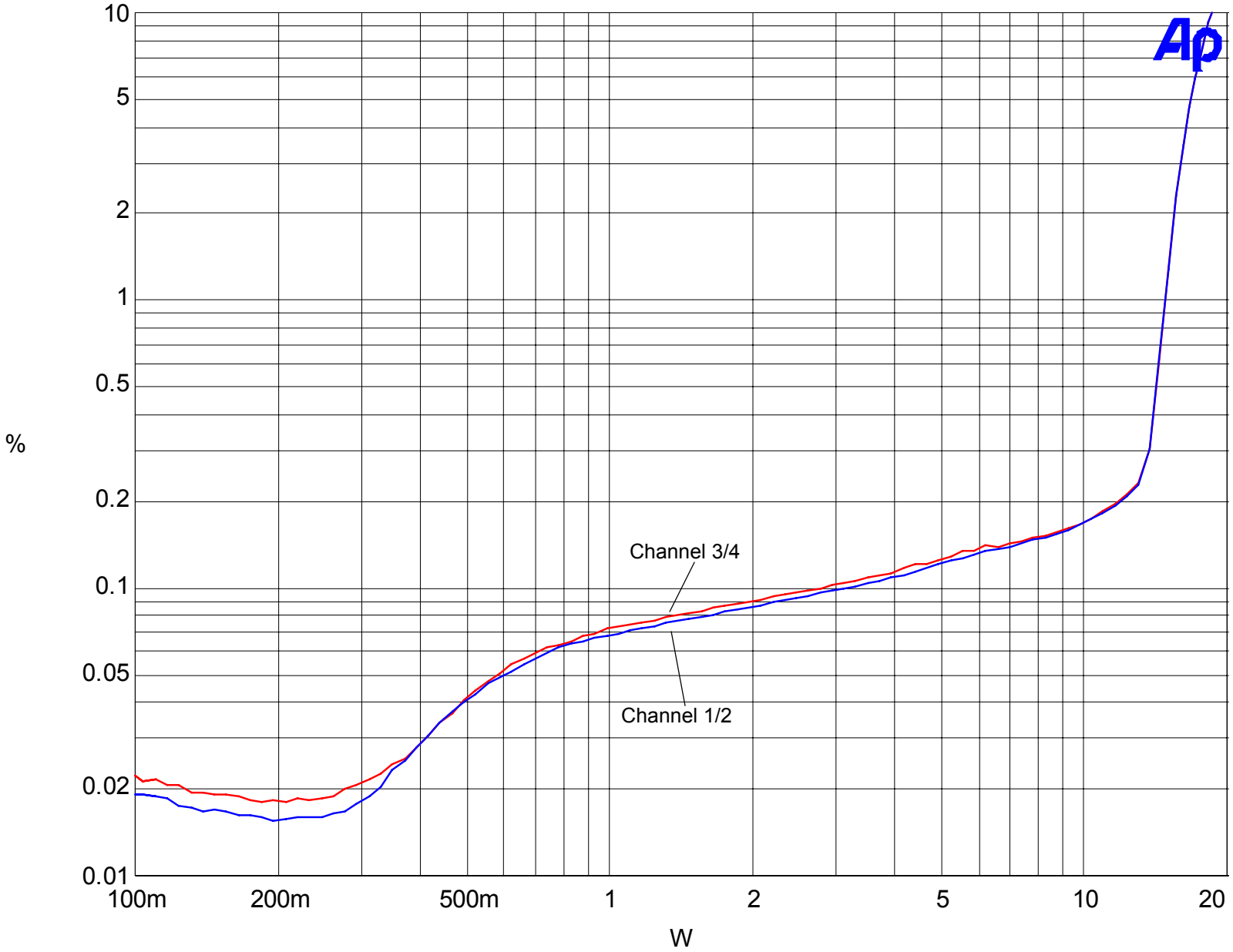


Figure 15. THD+N vs. Power

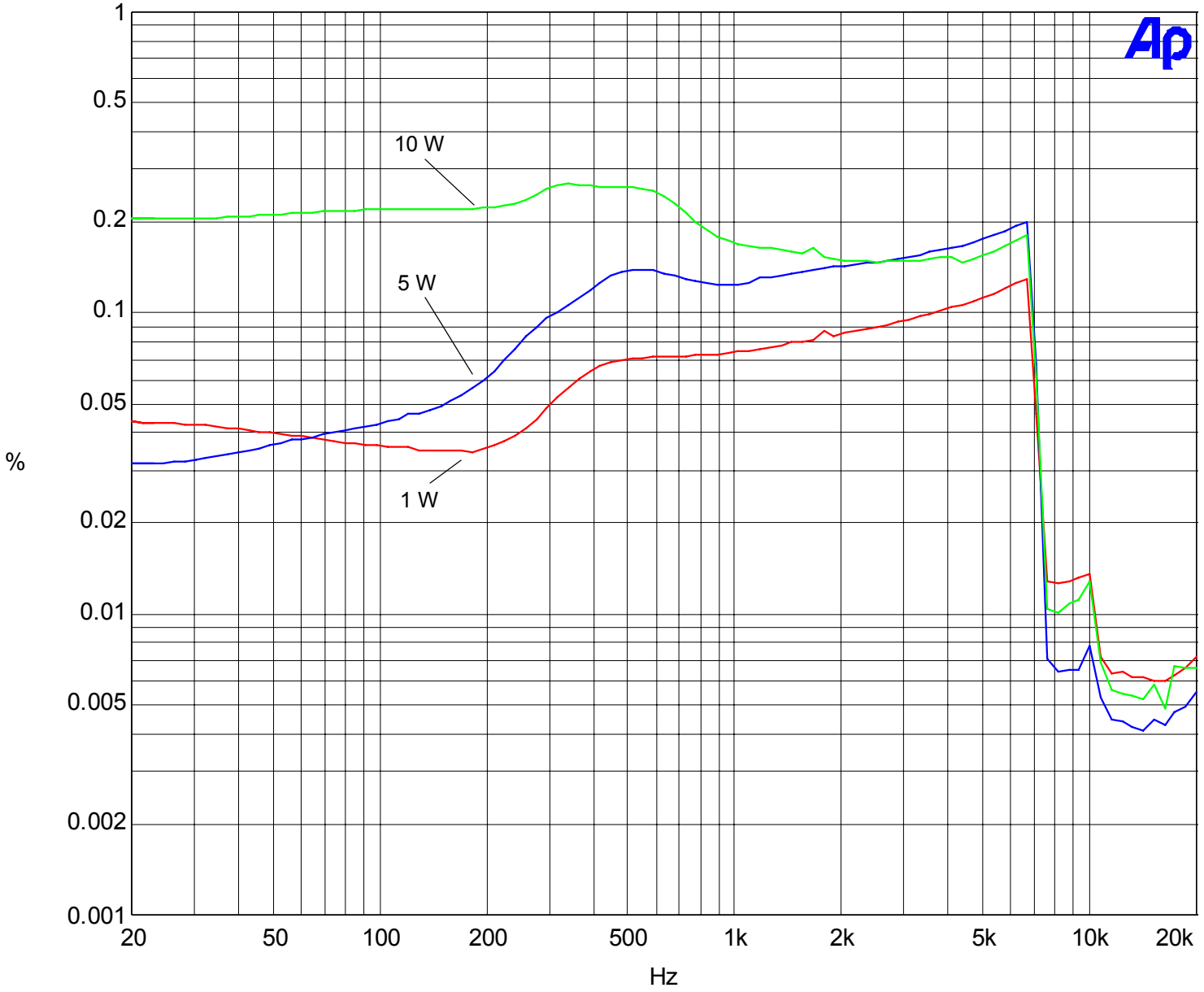


Figure 16. THD+N vs. Frequency

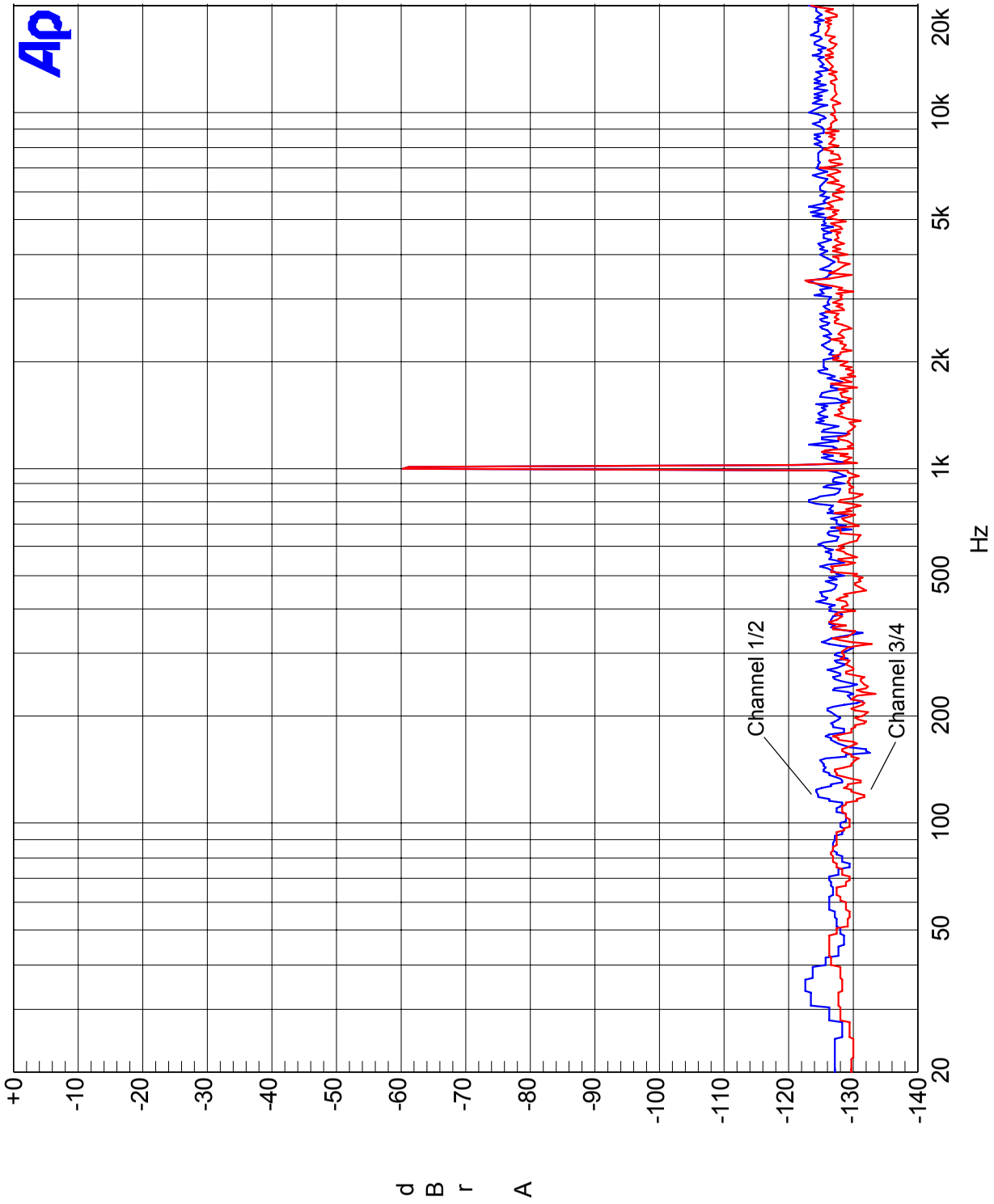


Figure 17. FFT at -60 dB Input

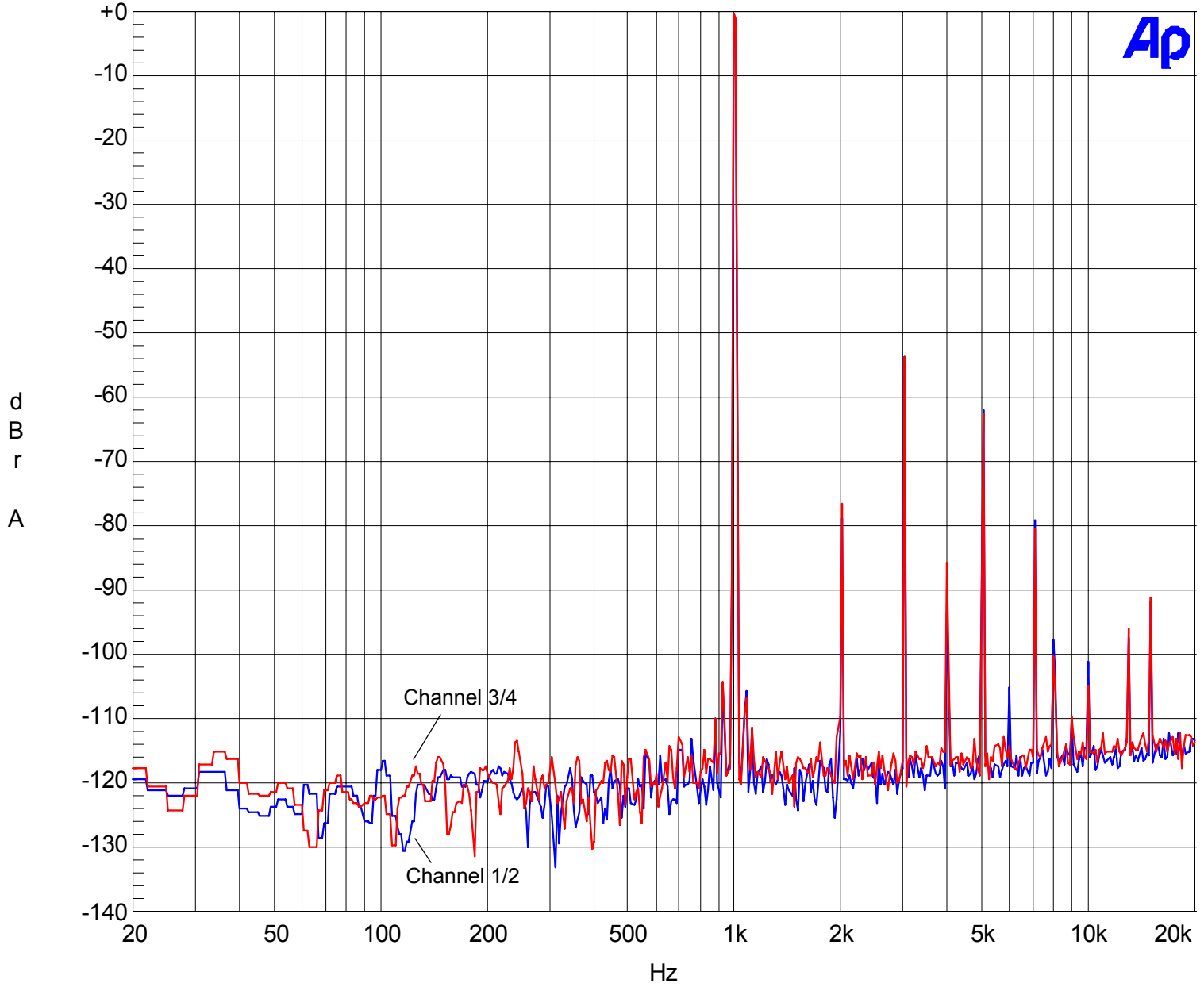


Figure 18. FFT at 0 dB Input

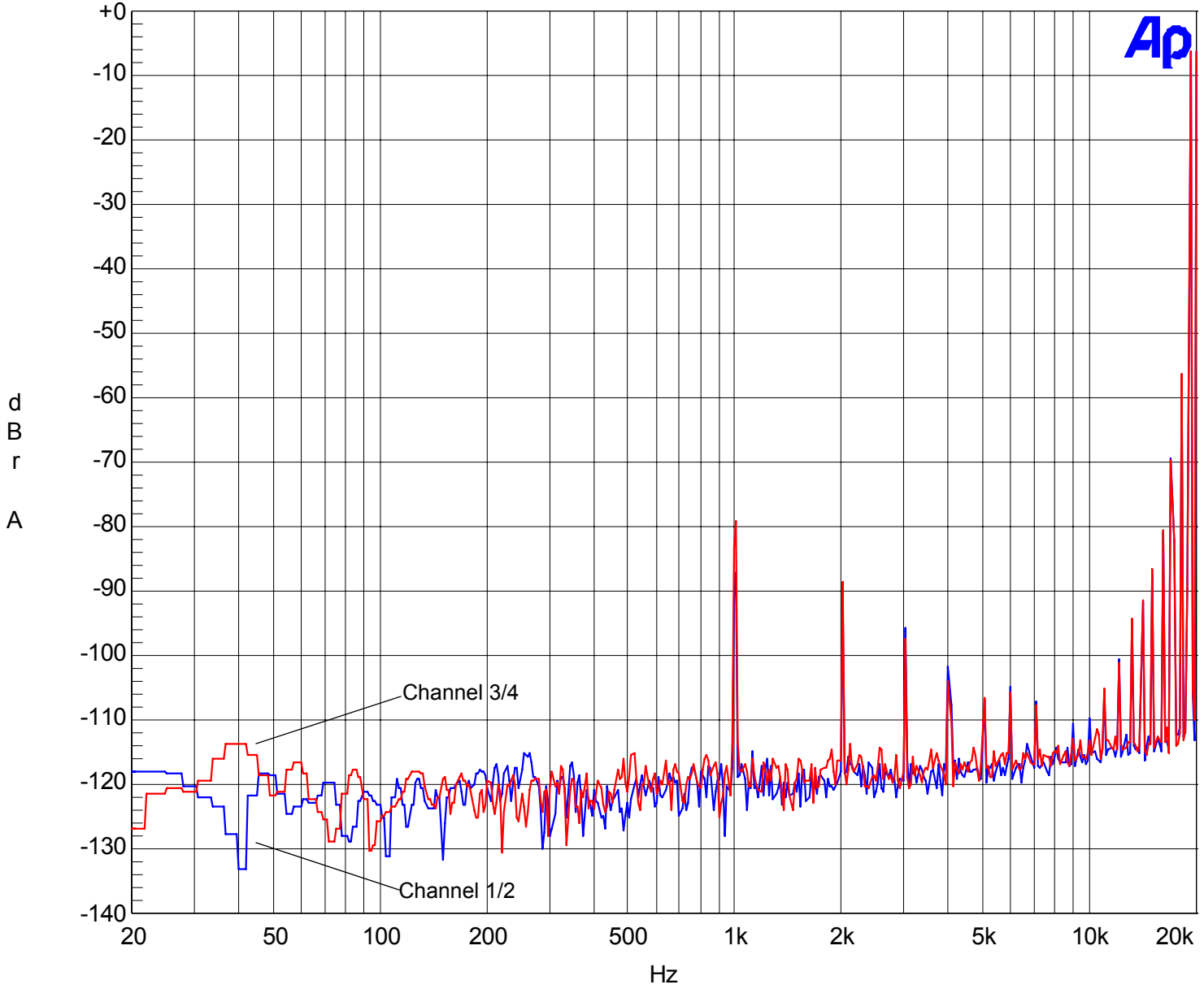


Figure 19. Inter-Modulation Distortion of 19 kHz + 20 kHz

9. THERMAL DE-RATING

The CRD4525-Q1 is a four-layer PCB design with 1 oz. (0.036 mm thick) copper. These parameters affect the thermal resistance and, since the PCB acts as a heat sink for the CS4525, the maximum sustained output power of the CRD4525-Q1. The CS4525 will generate heat that will flow into the PCB and then out to the ambient air surrounding the CRD4525-Q1; the more output power the CS4525 is delivering, the more heat it will produce. This transfer of heat is less effective at greater ambient temperatures. Because of this, there is a function between the ambient temperature and the maximum sustained output power the CS4525 can deliver before heating to the point of thermal error. This function is commonly detailed in a thermal de-rating curve, which describes how an amplifiers' rated output power is affected by ambient temperature. The thermal de-rating curve of a typical CRD4525-Q1 is shown in Figure 20.

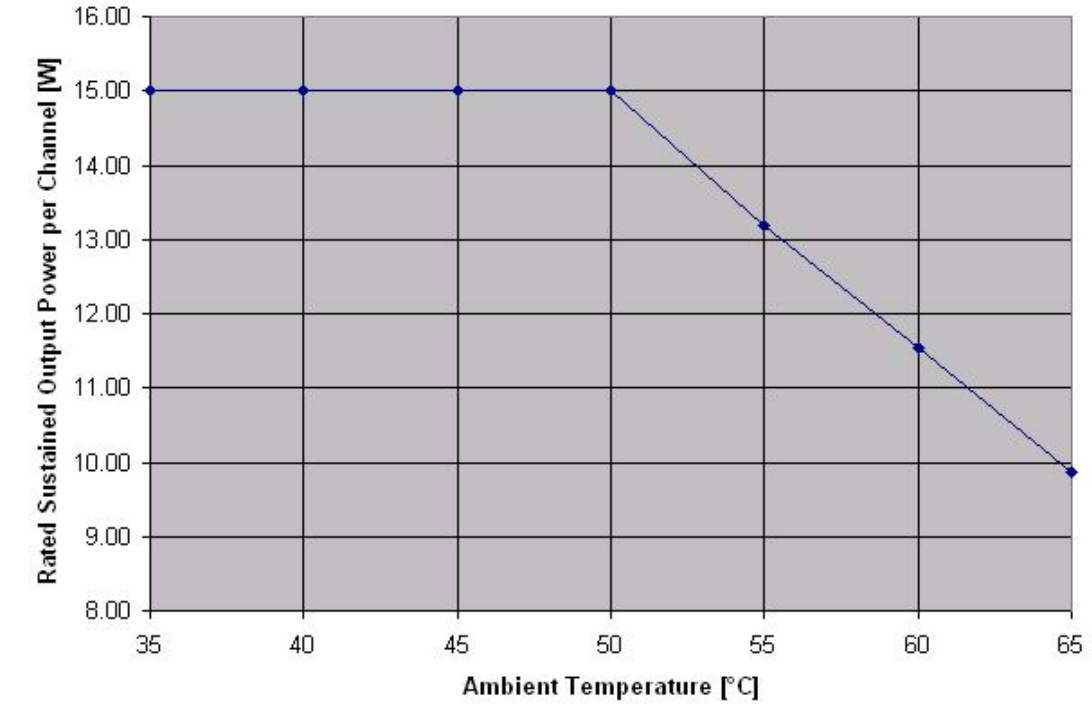


Figure 20. Thermal De-Rating Curve for a Typical CRD4525-Q1

For more information concerning thermal considerations of QFN packages, please refer to Cirrus Logic application note AN315.

10.ELECTROMAGNETIC COMPLIANCE

The electromagnetic interference (EMI) performance of the CRD4525-Q1 system has been tested for electromagnetic compliance (EMC) according to the FCC Class B Part 15 and CISPR22 standards for radiated emissions. The test results show that the CRD4525-Q1 reference design complies with both of these standards.

For optimal EMI performance, all printed circuit boards (PCB's) implementing the CS4525 device should be designed to match the PCB layout of the CRD4525-Q1 as closely as possible. In particular, the designer should take care to make the VP power input and PWM output filter section of the design, including component placement and trace routing, identical to that of the CRD4525-Q1 board.

10.1 EMI Testing Procedures

The purpose of radiated emissions testing is to ensure that the equipment under test (EUT) does not produce a level of EMI that would interrupt the normal operation of other devices or systems within close proximity to it.

To measure the EMI levels, the EUT and associated auxiliary equipment are placed into operation on top of a non-conductive table inside of an electromagnetically isolated chamber, as shown in Figure 21. As the table is rotated 360°, near field antennas record the amount of noise radiating from the EUT in the frequency range of 30 MHz to 1.0 GHz. These near field antennas (and associated electronics) scan and capture the EMI levels at various antenna heights and orientations (vertical or horizontal), relative to the EUT.

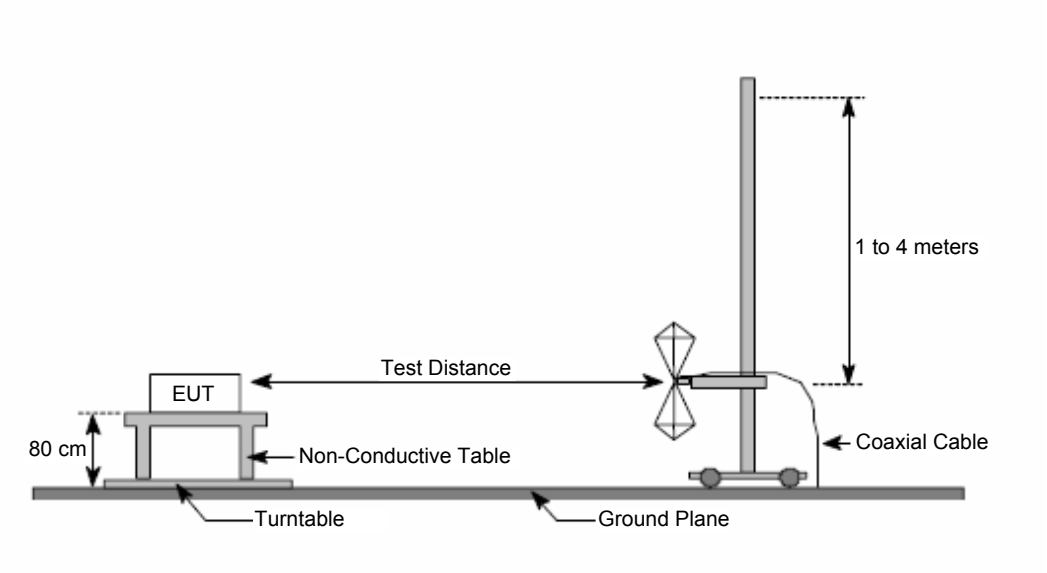


Figure 21. Test Facility Setup

The EMI data from these scans are combined to create a plot of the maximum levels of noise across all antenna heights and table rotation. The plots gathered from this procedure are called "Peak Scans". A set of peak scans (vertical and horizontal) is created for each possible operating mode, i.e. input configuration, output configuration, etc. The operating mode that produces the peak scans with highest levels of EMI is then evaluated more closely through the gathering of quasi-peak data.

Quasi-peak data is gathered by measuring the actual power content of the EMI detected during the peak scan procedure. Once this quasi-peak data has been recorded, it is compared against the limits of the applicable EMC standard to determine if the EUT is in compliance with the standard. In the case of the CS4525, these limits are defined by the FCC Class B Part 15 and the CISPR 22 EMC standards.

10.2 System Configuration

The source signal for EMC testing was a 1 kHz test tone generated by a battery-operated portable CD player. The CS4525 was driven at 1/8th of its rated power into two 8 Ω resistive loads connected to the CRD4525-Q1's output connectors through 3 meters of standard speaker wire. The CRD4525-Q1 was powered by a Mean Well U65S107-P2J 18 V power supply.

10.3 CRD4525-Q1 Test Results

Upon quasi-peak analysis of the peak scan data for all modes of operation, it has been confirmed that the CRD4525-Q1 complies with both the FCC Class B Part 15 and CISPR 22 EMC standards for radiated emissions. The peak scans for the "Optical S/PDIF In" mode of operation can be seen in Figure 22 and Figure 23. In this mode of operation, the 1 kHz test tone is supplied through an optical S/PDIF signal applied to J7. It should be noted that an open frame PCB, such as the CRD4525-Q1, represents the worst case scenario for EMC testing. Systems which include a shielded chassis and an earth ground will produce lower levels of EMI, given the same schematic and layout configuration as that of the CRD4525-Q1. A full compliance report is available upon request.

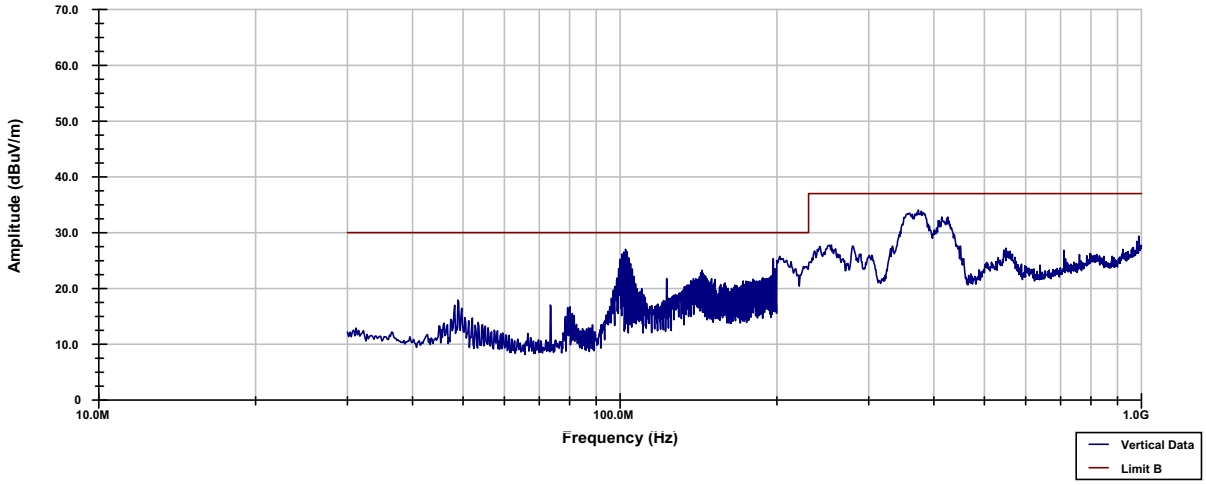


Figure 22. Vertical Peak Scan Data for the CRD4525-Q1

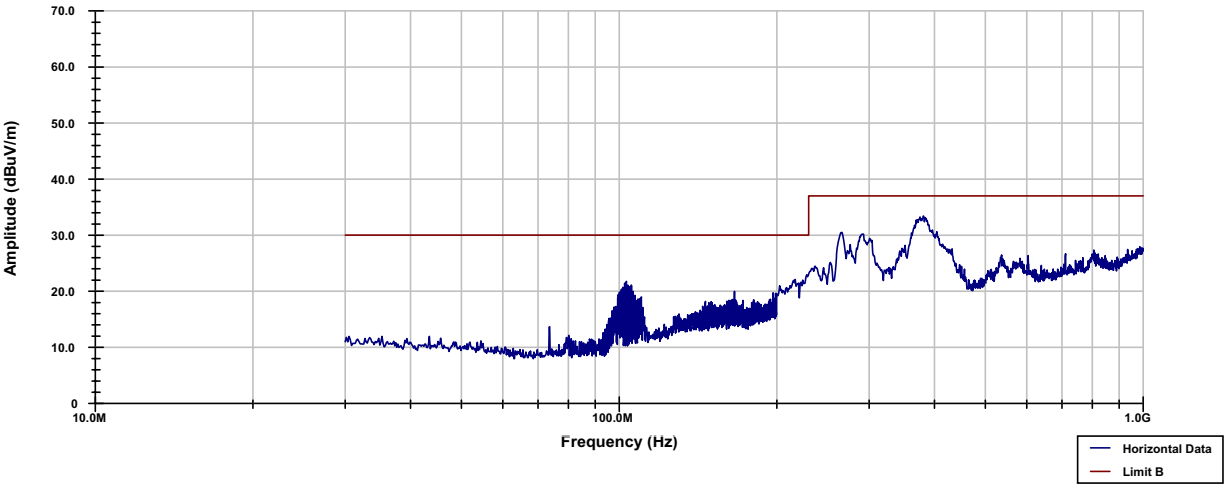


Figure 23. Horizontal Peak Scan Data for the CRD4525-Q1

11.REVISION HISTORY

Release	Changes
RD1	Initial Release.
RD2	Added Section 10. “Electromagnetic Compliance” on page 30.
RD3	Updated to reflect Rev. B PCB design.
RD4	Updated to reflect Rev. B PCB EMC and performance results.

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