

-100mA / -50V Digital transistor (with built-in resistors)

DTA125TUA / DTA125TKA

● Applications

Inverter, Interface, Driver

● Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors.
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input, and parasitic effects are almost completely eliminated.
- 3) Only the on / off conditions need to be set for operation, making the device design easy.
- 4) Higher mounting densities can be achieved.

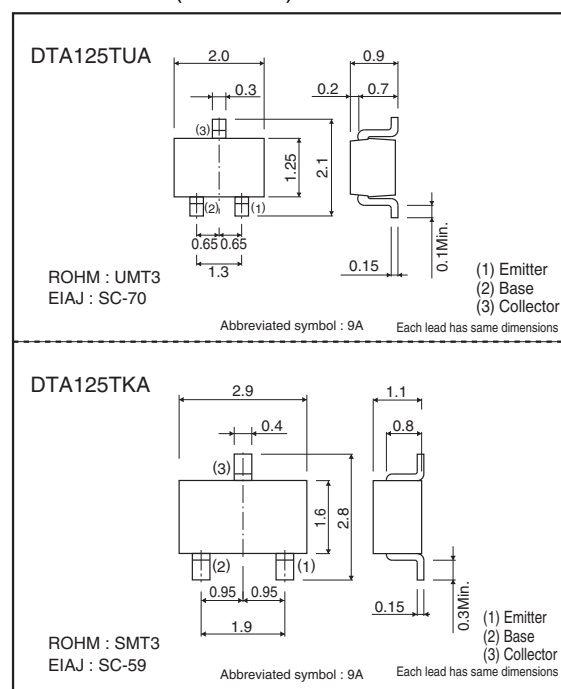
● Structure

PNP epitaxial planar silicon transistor
 (Resistor built-in type)

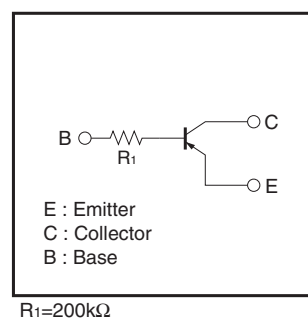
● Packaging specifications

	Package	UMT3	SMT3
	Packaging type	Taping	Taping
	Code	T106	T146
Part No.	Basic ordering unit (pieces)	3000	3000
DTA125TUA		○	—
DTA125TKA		—	○

● Dimensions (Unit : mm)



● Inner circuit



● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	-50	V
Collector-emitter voltage	V_{CEO}	-50	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-100	mA
Collector power dissipation	P_C	200	mW
Junction temperature	T_J	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

● Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	-50	—	—	V	$I_C = -50\mu A$
Collector-emitter breakdown voltage	BV_{CEO}	-50	—	—	V	$I_C = -1mA$
Emitter-base breakdown voltage	BV_{EBO}	-5	—	—	V	$I_E = -50\mu A$
Collector cutoff current	I_{CBO}	—	—	-0.5	μA	$V_{CB} = -50V$
Emitter cutoff current	I_{EBO}	—	—	-0.5	μA	$V_{EB} = -4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	-0.3	V	$I_C = -0.5mA, I_B = -0.05mA$
DC current transfer ratio	h_{FE}	100	250	600	—	$I_C = -1mA, V_{CE} = -5V$
Input resistance	R_i	140	200	260	$k\Omega$	—
Transition frequency	f_T *	—	250	—	MHz	$V_{CE} = -10V, I_E = 5mA, f = 100MHz$

* Characteristics of built-in transistor

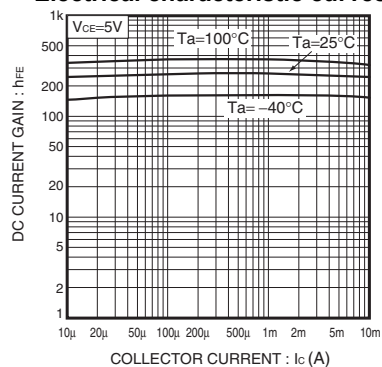
● Electrical characteristic curves


Fig.1 DC current gain
vs. Collector current

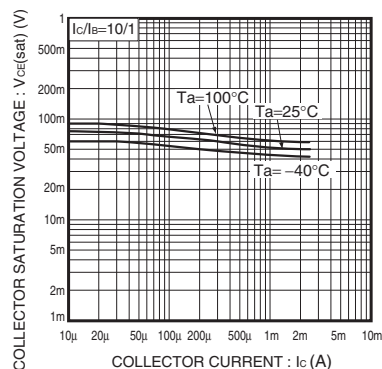


Fig.2 Collector-Emitter saturation voltage
vs. Collector current

Notes

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