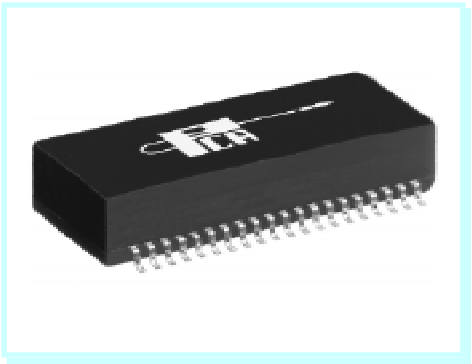
10/100 BX Module for Quad-Port Application

EPF8034S



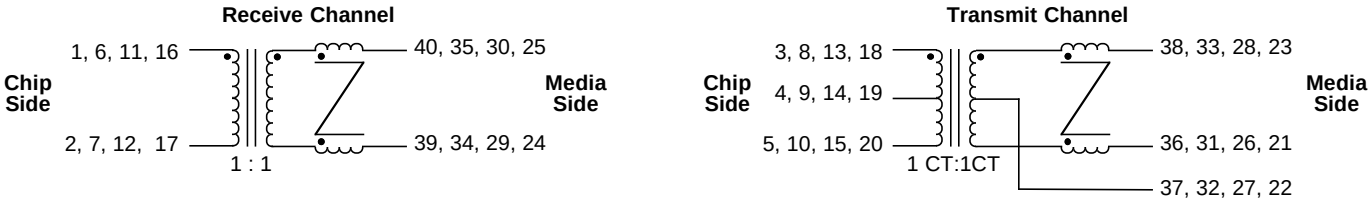
- Optimized for DP83840A/Twister combination •
- Recommended for use with ICS1890 series, SSI TSC78Q2120 chips •
- Guaranteed to operate with 8 mA DC bias at 70°C •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

Electrical Parameters @ 25° C

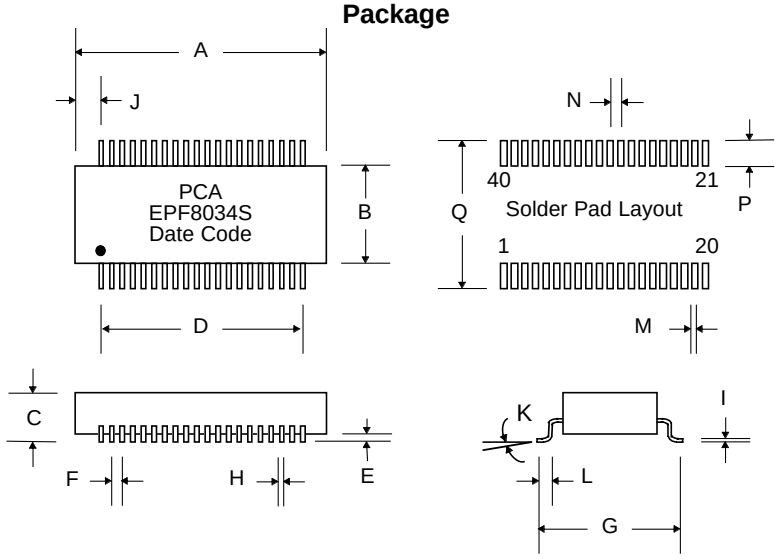
OCL @ 70°C	Insertion Loss (dB Max.)				Return Loss (dB Min.)						Common Mode Rejection (dB Min.)								Crosstalk (dB Min.)
100 KHz, 0.1 Vrms 8 mA DC Bias	0.1-100 MHz		150 MHz		1-30 MHz		60 MHz		100 MHz		30-100 MHz		200 MHz		300 MHz		500 MHz		0.1-100 MHz
Media Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	
350µH	-1	-1	-3	-3	-18	-18	-12	-12	-10	-10	-30	-25	-25	-20	-20	-10	-15	---	-30

• **Isolation** : 1500 Vrms • **Impedance** : 100 ohms • **Rise Time** : 3.0 nS Max. •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	1.110	1.130	1.120	28.19	28.70	28.45
B	.470	.490	.480	11.94	12.45	12.19
C	.250	.270	.260	6.35	6.86	6.60
D	---	---	.950	---	---	24.13
E	.010	.015	.0125	.254	.381	.317
F	---	---	.050	---	---	1.27
G	.590	.610	.600	14.99	15.49	15.24
H	.016	.022	.019	.406	.559	.483
I	.008	.012	.010	.203	.305	.254
J	---	---	.085	---	---	2.16
K	0°	8°	---	0°	8°	---
L	.025	.045	.035	.635	1.14	.889
M			.030			.762
N			.050			1.27
P			.090			2.29
Q			.670			17.02

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CSF8034Sa Rev. Orig.1 8/31/98

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EPF8034S

The circuit below is a guideline for interconnecting EPF8034S with DP83840A and DP83223 twister chip set for 100 Mb/s applications. Further details can be obtained from the chip manufacturer. Please consult PCA for application help regarding the SSI78Q2120 or ICS1890 series parts or consult with vendor's application notes on this.

Typical insertion loss of the isolation transformer is 0.5dB that covers the entire spectrum of the encoded signals in 100 protocols. This means that under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust TXREF resistor of the twister chip to get at least 2.12V pk-pk across the transmit input pins.

It is recommended that system designers do not use the receiver side center tap to ground, via a capacitor. This might worsen EMI specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

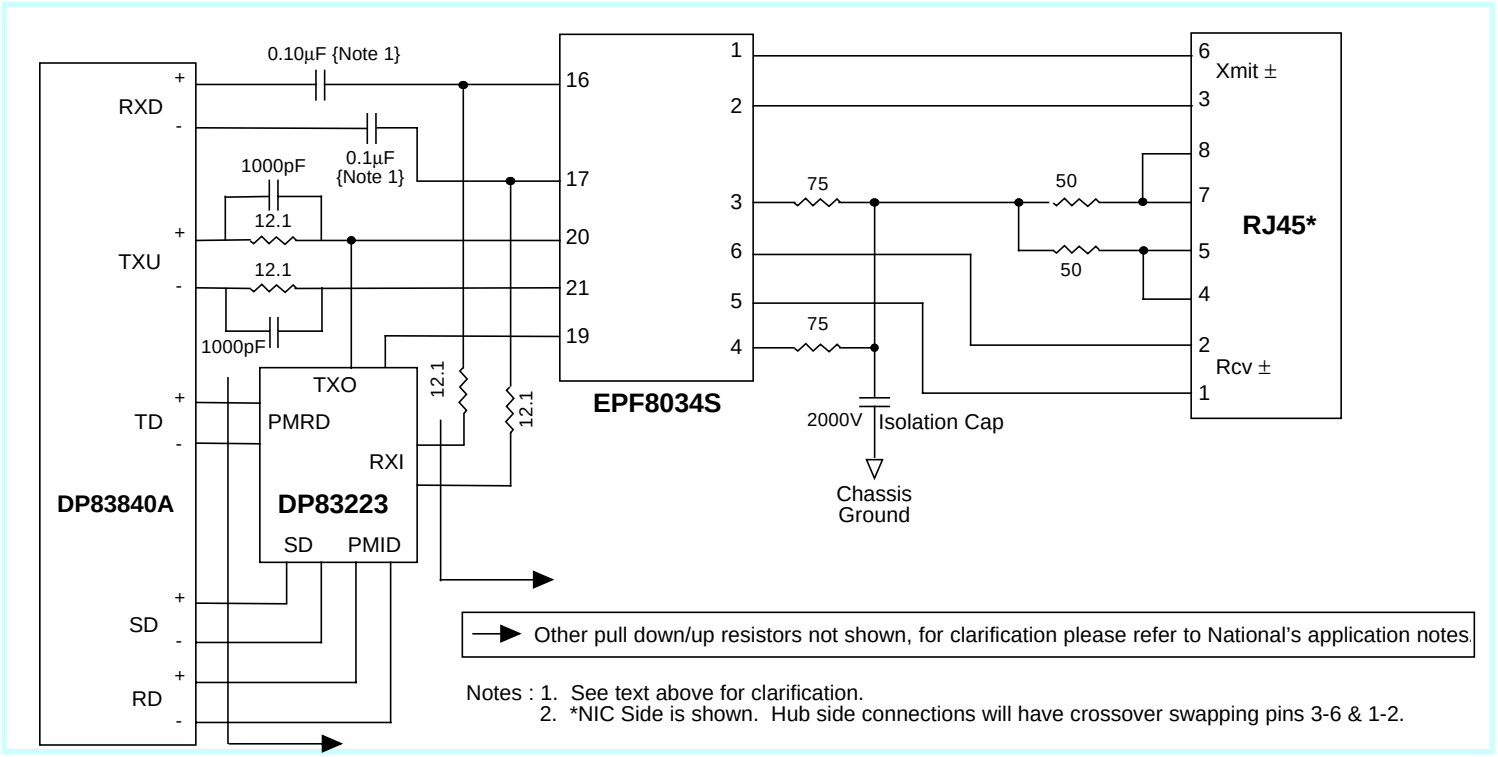
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75 Ω shown from the center taps of the secondary may be taken to chassis ground via a suitable cap. This depends upon user's design, EMI margin, etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8034S. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP (Excerpts from NSC DP83840A application notes). For one port only.



Notes : 1. See text above for clarification.
2. *NIC Side is shown. Hub side connections will have crossover swapping pins 3-6 & 1-2.

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