

74199
Shift Register

8-Bit Parallel-Access Shift Register
Product Specification

Logic Products

FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J-K (D) inputs to first stage
- Clock enable for hold (do nothing) mode
- Asynchronous Master Reset

DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74199	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^{\circ}C$ to $+70^{\circ}C$
Plastic DIP	N74199N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

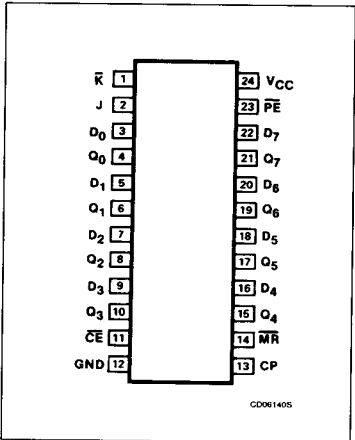
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
All	Inputs	1ul
$Q_0 - Q_7$	Parallel outputs	10ul

NOTE:

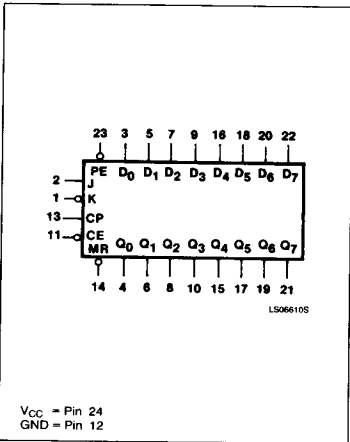
A 74 unit load (ul) is understood to be $40\mu A$ I_{IH} AND $-1.6mA$ I_{IL} .

PIN CONFIGURATION



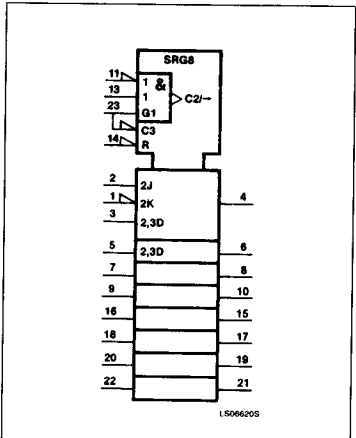
December 4, 1985

LOGIC SYMBOL



5-395

LOGIC SYMBOL (IEEE/IEC)

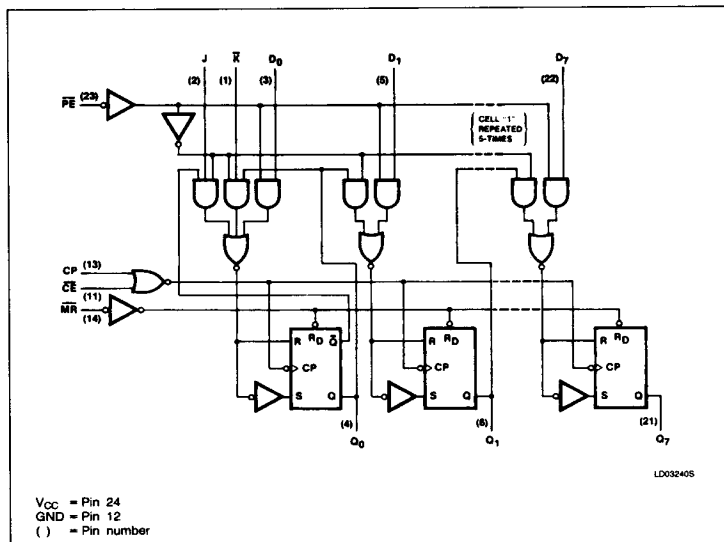


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Shift Register

74199

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS						
	MR	CP	CE	PE	J	K	D _n	Q ₀	Q ₁	Q ₆	Q ₇		
Reset (clear)	L	X	X	X	X	X	X	L	L	L	L		
Shift, set first stage	H	↑	I	h	h	h	X	H	q ₀	q ₅	q ₆		
Shift, reset first stage	H	↑	I	h	I	I	X	L	q ₀	q ₅	q ₆		
Shift, toggle first stage	H	↑	I	h	h	I	X	\bar{q}_0	q ₀	q ₅	q ₆		
Shift, retain first stage	H	↑	I	h	I	h	X	q ₀	q ₀	q ₅	Q ₆		
Parallel load	H	↑	I	I	X	X	d _n	d ₀	d ₁	d ₆	d ₇		
Hold (do nothing)	H	↑	h ^(a)	X	X	X	X	q ₀	q ₁	q ₆	q ₇		

H = HIGH voltage level steady state.

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level steady state.

I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't care

d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH clock transition.

NOTE:

a. The LOW-to-HIGH transition of CE should only occur while CP is HIGH for conventional operation.

The '199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable (PE) input. Serial data enters the first flip-flop (Q_0) via the J and K inputs when the PE input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2$ following each LOW-to-HIGH clock transition. The J and K inputs provide the flexibility of the J-K type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the PE input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_7$) is transferred to the respective $Q_0 - Q_7$ outputs.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, K, D_n, and PE inputs for logic operation, other than the set-up and release time requirements.

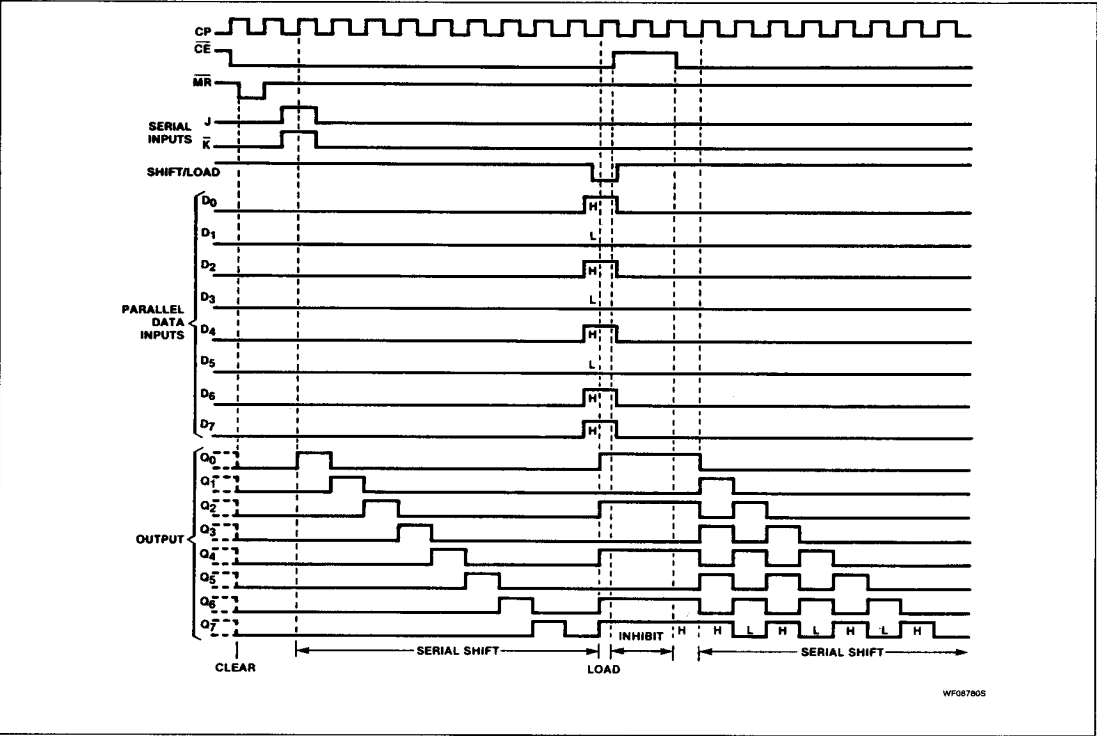
The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable (CE) input. The pin assignment for the CP and CE inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of CE input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

Shift Register

74199

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.8	V
I _{IK}	Input clamp current			-12	mA
I _{OH}	HIGH-level output current			-800	V
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

Shift Register

74199

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74199			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		90	127	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with \bar{K} , J and D inputs at 4.5V, momentary ground clock, then apply 4.5V, ground \overline{CE} , \overline{MR} and \overline{PE} .

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		UNIT
			C _L = 15pF, R _L = 400Ω		
			Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to output	Waveform 1		26 30	ns
t _{PHL}	Propagation delay MR to output	Waveform 2		35	ns

Per industry convention, f_{MAX} is the worst case of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

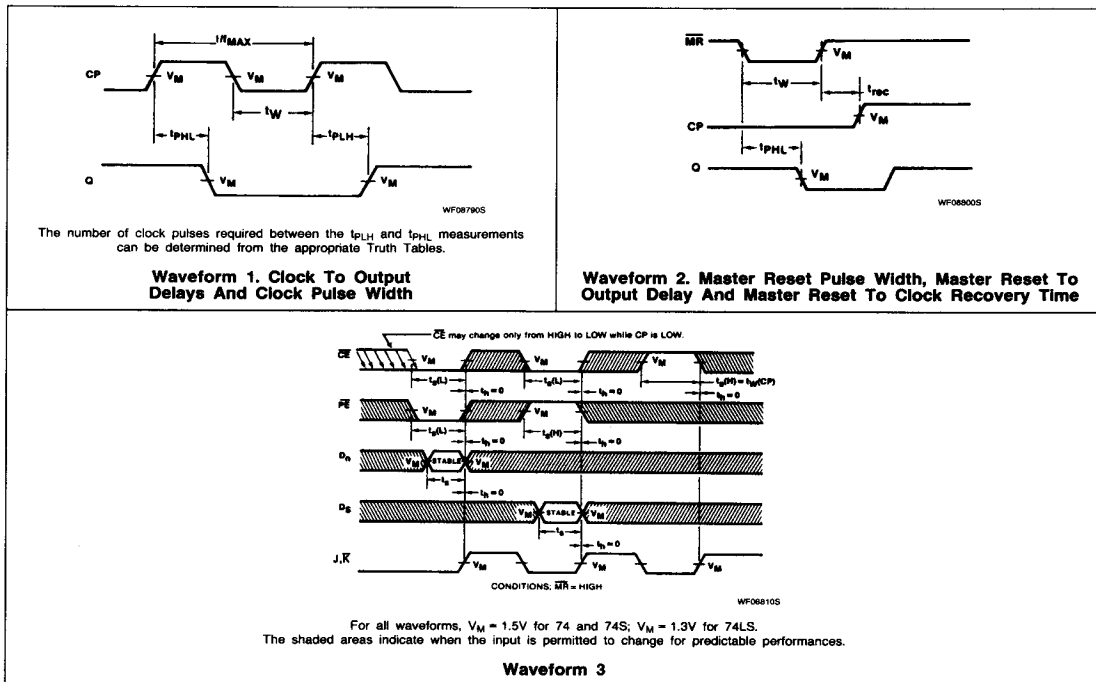
AC SET-UP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
t _W Clock pulse width	Waveform 1	20		ns
t _W \overline{MR} pulse width	Waveform 2	20		ns
t _s Set-up time, J, \bar{K} and data to clock	Waveform 3	20		ns
t _h Hold time, J, \bar{K} and data to clock	Waveform 3	0		ns
t _s Set-up time, \overline{CE} to clock	Waveform 3	30		ns
t _h Hold time, \overline{CE} to clock	Waveform 3	0		ns
t _s Set-up time, \overline{PE} to clock	Waveform 3	30		ns
t _h Hold time, \overline{PE} to clock	Waveform 3	0		ns
t _{rec} Recovery time, \overline{MR} to clock	Waveform 2	30		ns

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74199

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

