

# MC74HC161A, MC74HC163A

## Presettable Counters

### High-Performance Silicon-Gate CMOS

The MC74HC161A and HC163A are identical in pinout to the LS161 and LS163. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC161A and HC163A are programmable 4-bit binary counters with asynchronous and synchronous reset, respectively.

#### Features

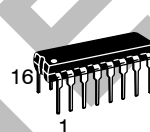
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates
- Pb-Free Packages are Available\*



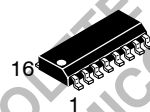
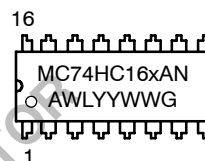
ON Semiconductor®

<http://onsemi.com>

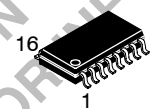
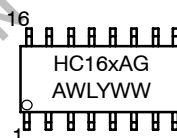
#### MARKING DIAGRAMS



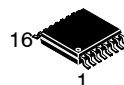
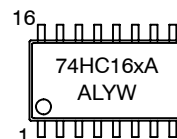
PDIP-16  
N SUFFIX  
CASE 648



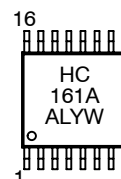
SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



TSSOP-16  
DT SUFFIX  
CASE 948F



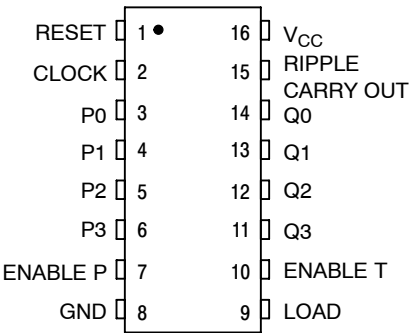
x = 1 or 3  
A = Assembly Location  
WL, L = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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FUNCTION TABLE

| Inputs |        |      |          |          | Output<br>Q      |
|--------|--------|------|----------|----------|------------------|
| Clock  | Reset* | Load | Enable P | Enable T |                  |
|        | L      | X    | X        | X        | Reset            |
|        | H      | L    | X        | X        | Load Preset Data |
|        | H      | H    | H        | H        | Count            |
|        | H      | H    | L        | X        | No Count         |
|        | H      | H    | X        | L        | No Count         |

\*HC163A only. HC161A is an Asynchronous Reset Device  
H = high level, L = low level, X = don't care

Figure 1. Pin Assignment

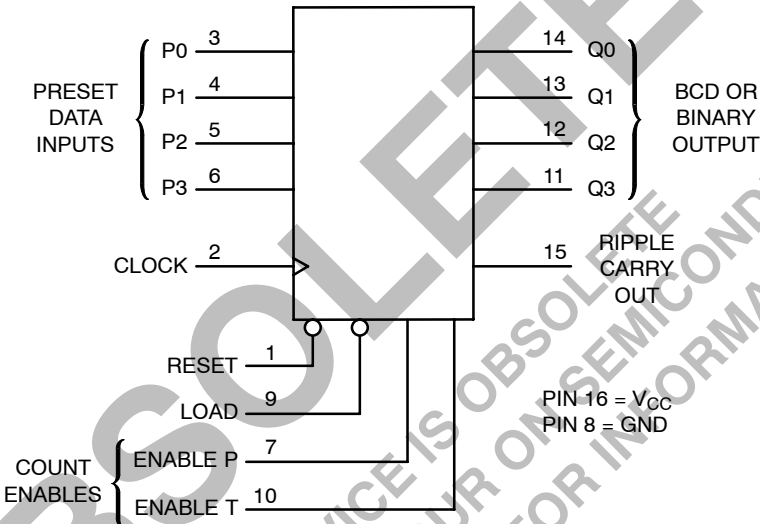


Figure 2. Logic Diagram

DEVICE/MODE TABLE

| Device | Count Mode | Reset Mode   |
|--------|------------|--------------|
| HC161A | Binary     | Asynchronous |
| HC163A | Binary     | Synchronous  |

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## MAXIMUM RATINGS

| Symbol               | Parameter                                       | Value                                                                                                    | Unit        |
|----------------------|-------------------------------------------------|----------------------------------------------------------------------------------------------------------|-------------|
| V <sub>CC</sub>      | DC Supply Voltage                               | − 0.5 to + 7.0                                                                                           | V           |
| V <sub>I</sub>       | DC Input Voltage                                | − 0.5 to V <sub>CC</sub> + 0.5                                                                           | V           |
| V <sub>O</sub>       | DC Output Voltage (Note 1)                      | − 0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5                                                           | V           |
| I <sub>IK</sub>      | DC Input Diode Current                          | ± 20                                                                                                     | mA          |
| I <sub>OK</sub>      | DC Output Diode Current                         | ± 25                                                                                                     | mA          |
| I <sub>O</sub>       | DC Output Sink Current                          | ± 25                                                                                                     | mA          |
| I <sub>CC</sub>      | DC Supply Current per Supply Pin                | ± 50                                                                                                     | mA          |
| I <sub>GND</sub>     | DC Ground Current per Ground Pin                | ± 50                                                                                                     | mA          |
| T <sub>STG</sub>     | Storage Temperature Range                       | − 65 to + 150                                                                                            | °C          |
| T <sub>L</sub>       | Lead Temperature, 1 mm from Case for 10 Seconds | 260                                                                                                      | °C          |
| T <sub>J</sub>       | Junction Temperature Under Bias                 | + 150                                                                                                    | °C          |
| θ <sub>JA</sub>      | Thermal Resistance                              | PDIP 78<br>SOIC 112<br>TSSOP 148                                                                         | °C/W        |
| P <sub>D</sub>       | Power Dissipation in Still Air at 85°C          | PDIP 750<br>SOIC 500<br>TSSOP 450                                                                        | mW          |
| MSL                  | Moisture Sensitivity                            | Level 1                                                                                                  |             |
| F <sub>R</sub>       | Flammability Rating                             | Oxygen Index: 30% – 35%<br>UL 94 V-0 @ 0.125 in                                                          |             |
| V <sub>ESD</sub>     | ESD Withstand Voltage                           | Human Body Model (Note 2) > 2000<br>Machine Model (Note 3) > 200<br>Charged Device Model (Note 4) > 1000 | V           |
| I <sub>LATCHUP</sub> | Latchup Performance                             | Above V <sub>CC</sub> and Below GND at 85°C (Note 5)                                                     | ± 300<br>mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I<sub>O</sub> absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                            | Min                                                                                                              | Max                       | Unit |
|------------------------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|---------------------------|------|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                | 2.0                                                                                                              | 6.0                       | V    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0                                                                                                                | V <sub>CC</sub>           | V    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types             | − 55                                                                                                             | + 125                     | °C   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time (Figure 4)                  | V <sub>CC</sub> = 2.0 V 0<br>V <sub>CC</sub> = 3.0 V 0<br>V <sub>CC</sub> = 4.5 V 0<br>V <sub>CC</sub> = 6.0 V 0 | 1000<br>600<br>500<br>400 | ns   |

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                         | Test Conditions                                                                                                                                      | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                 |                                   |                                                                                                                                                      |                      | -55 to 25°C      | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage  | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                                   | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |                                   |                                                                                                                                                      | 3.0                  | 2.1              | 2.1    | 2.1     |      |
|                 |                                   |                                                                                                                                                      | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |                                   |                                                                                                                                                      | 6.0                  | 4.2              | 4.2    | 4.2     |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage   | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                                   | 2.0                  | 0.5              | 0.5    | 0.5     | V    |
|                 |                                   |                                                                                                                                                      | 3.0                  | 0.9              | 0.9    | 0.9     |      |
|                 |                                   |                                                                                                                                                      | 4.5                  | 1.35             | 1.35   | 1.35    |      |
|                 |                                   |                                                                                                                                                      | 6.0                  | 1.8              | 1.8    | 1.8     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                                  | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |                                   |                                                                                                                                                      | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |                                   |                                                                                                                                                      | 6.0                  | 5.9              | 5.9    | 5.9     |      |
|                 |                                   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 3.6 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 2.48             | 2.34   | 2.2     |      |
|                 |                                   |                                                                                                                                                      | 4.5                  | 3.98             | 3.84   | 3.7     |      |
|                 |                                   |                                                                                                                                                      | 6.0                  | 5.48             | 5.34   | 5.2     |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                                  | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |                                   |                                                                                                                                                      | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |                                   |                                                                                                                                                      | 6.0                  | 0.1              | 0.1    | 0.1     |      |
|                 |                                   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 3.6 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 0.26             | 0.33   | 0.4     |      |
|                 |                                   |                                                                                                                                                      | 4.5                  | 0.26             | 0.33   | 0.4     |      |
|                 |                                   |                                                                                                                                                      | 6.0                  | 0.26             | 0.33   | 0.4     |      |
| I <sub>in</sub> | Maximum Input Leakage Current     | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                                             | 6.0                  | ±0.1             | ±1.0   | ±1.0    | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current  | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                                                                  | 6.0                  | 4.0              | 40     | 160     | μA   |

7. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

| Symbol                                 | Parameter                                                                | Figure | V <sub>CC</sub><br>V | Guaranteed Limit |         |          | Unit |
|----------------------------------------|--------------------------------------------------------------------------|--------|----------------------|------------------|---------|----------|------|
|                                        |                                                                          |        |                      | – 55 to 25 °C    | ≤ 85 °C | ≤ 125 °C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency<br>(50% Duty Cycle)<br>(Note 8)                  | 4, 10  | 2.0                  | 6                | 5       | 4        | MHz  |
|                                        |                                                                          |        | 3.0                  | 15               | 12      | 10       |      |
|                                        |                                                                          |        | 4.5                  | 30               | 24      | 20       |      |
|                                        |                                                                          |        | 6.0                  | 35               | 28      | 24       |      |
| t <sub>PLH</sub>                       | Maximum Propagation Delay,<br>Clock to Q                                 | 4, 10  | 2.0                  | 120              | 160     | 200      | ns   |
|                                        |                                                                          |        | 3.0                  | 75               | 120     | 150      |      |
|                                        |                                                                          |        | 4.5                  | 20               | 23      | 28       |      |
|                                        |                                                                          |        | 6.0                  | 16               | 20      | 22       |      |
| t <sub>PHL</sub>                       |                                                                          | 4, 10  | 2.0                  | 145              | 185     | 220      | ns   |
|                                        |                                                                          |        | 3.0                  | 100              | 135     | 150      |      |
|                                        |                                                                          |        | 4.5                  | 22               | 25      | 30       |      |
|                                        |                                                                          |        | 6.0                  | 18               | 20      | 23       |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay,<br>Reset to Q (HC161A Only)                   | 5, 10  | 2.0                  | 145              | 185     | 220      | ns   |
|                                        |                                                                          |        | 3.0                  | 100              | 135     | 150      |      |
|                                        |                                                                          |        | 4.5                  | 20               | 22      | 25       |      |
|                                        |                                                                          |        | 6.0                  | 17               | 19      | 21       |      |
| t <sub>PLH</sub>                       | Maximum Propagation Delay,<br>Enable T to Ripple Carry Out               | 6, 10  | 2.0                  | 110              | 150     | 190      | ns   |
|                                        |                                                                          |        | 3.0                  | 60               | 115     | 140      |      |
|                                        |                                                                          |        | 4.5                  | 16               | 18      | 20       |      |
|                                        |                                                                          |        | 6.0                  | 14               | 15      | 17       |      |
| t <sub>PHL</sub>                       |                                                                          | 6, 10  | 2.0                  | 135              | 175     | 210      | ns   |
|                                        |                                                                          |        | 3.0                  | 100              | 130     | 160      |      |
|                                        |                                                                          |        | 4.5                  | 18               | 20      | 22       |      |
|                                        |                                                                          |        | 6.0                  | 15               | 16      | 20       |      |
| t <sub>PLH</sub>                       | Maximum Propagation Delay,<br>Clock to Ripple Carry Out                  | 4, 10  | 2.0                  | 120              | 160     | 200      | ns   |
|                                        |                                                                          |        | 3.0                  | 75               | 135     | 150      |      |
|                                        |                                                                          |        | 4.5                  | 22               | 27      | 30       |      |
|                                        |                                                                          |        | 6.0                  | 18               | 22      | 25       |      |
| t <sub>PHL</sub>                       |                                                                          | 4, 10  | 2.0                  | 145              | 185     | 220      | ns   |
|                                        |                                                                          |        | 3.0                  | 100              | 135     | 150      |      |
|                                        |                                                                          |        | 4.5                  | 22               | 28      | 35       |      |
|                                        |                                                                          |        | 6.0                  | 20               | 24      | 28       |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay,<br>Reset to Ripple Carry Out<br>(HC161A Only) | 5, 10  | 2.0                  | 155              | 190     | 230      | ns   |
|                                        |                                                                          |        | 3.0                  | 120              | 140     | 155      |      |
|                                        |                                                                          |        | 4.5                  | 22               | 26      | 30       |      |
|                                        |                                                                          |        | 6.0                  | 18               | 22      | 25       |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time,<br>Any Output                            | 5, 10  | 2.0                  | 75               | 95      | 110      | ns   |
|                                        |                                                                          |        | 3.0                  | 30               | 40      | 55       |      |
|                                        |                                                                          |        | 4.5                  | 15               | 19      | 22       |      |
|                                        |                                                                          |        | 6.0                  | 13               | 16      | 19       |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                | 4, 10  | –                    | 10               | 10      | 10       | pF   |

8. Applies to noncascaded/nonsynchronous clocked configurations only with synchronously cascaded counters. (1) Clock to Ripple Carry Out propagation delays. (2) Enable T or Enable P to Clock setup times and (3) Clock to Enable T or Enable P hold times determine f<sub>max</sub>. However, if Ripple Carry out of each stage is tied to the Clock of the next stage (nonsynchronously clocked) the f<sub>max</sub> in the table above is applicable. See Applications information in this data sheet.
9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Gate) (Note 10) | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |    |
|-----------------|----------------------------------------------------|-----------------------------------------|----|
|                 |                                                    | 45                                      | pF |

10. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

# MC74HC161A, MC74HC163A

## TIMING REQUIREMENTS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

| Symbol                          | Parameter                                                       | Figure | V <sub>CC</sub><br>V | Guaranteed Limit |         |          | Unit |
|---------------------------------|-----------------------------------------------------------------|--------|----------------------|------------------|---------|----------|------|
|                                 |                                                                 |        |                      | – 55 to 25 °C    | ≤ 85 °C | ≤ 125 °C |      |
| t <sub>su</sub>                 | Minimum Setup Time,<br>Preset Data Inputs to Clock              | 8      | 2.0                  | 40               | 60      | 80       | ns   |
|                                 |                                                                 |        | 3.0                  | 20               | 30      | 40       |      |
|                                 |                                                                 |        | 4.5                  | 15               | 20      | 30       |      |
|                                 |                                                                 |        | 6.0                  | 12               | 18      | 20       |      |
| t <sub>su</sub>                 | Minimum Setup Time,<br>Load to Clock                            | 8      | 2.0                  | 60               | 75      | 90       | ns   |
|                                 |                                                                 |        | 3.0                  | 25               | 30      | 40       |      |
|                                 |                                                                 |        | 4.5                  | 15               | 20      | 30       |      |
|                                 |                                                                 |        | 6.0                  | 12               | 18      | 20       |      |
| t <sub>su</sub>                 | Minimum Setup Time,<br>Reset to Clock (HC163A Only)             | 7      | 2.0                  | 60               | 75      | 90       | ns   |
|                                 |                                                                 |        | 3.0                  | 25               | 30      | 40       |      |
|                                 |                                                                 |        | 4.5                  | 20               | 25      | 35       |      |
|                                 |                                                                 |        | 6.0                  | 17               | 23      | 25       |      |
| t <sub>su</sub>                 | Minimum Setup Time,<br>Enable T or Enable P to Clock            | 9      | 2.0                  | 80               | 95      | 110      | ns   |
|                                 |                                                                 |        | 3.0                  | 35               | 40      | 50       |      |
|                                 |                                                                 |        | 4.5                  | 20               | 25      | 35       |      |
|                                 |                                                                 |        | 6.0                  | 17               | 23      | 25       |      |
| t <sub>h</sub>                  | Minimum Hold Time,<br>Clock to Load or Preset Data Inputs       | 8      | 2.0                  | 3                | 3       | 3        | ns   |
|                                 |                                                                 |        | 3.0                  | 3                | 3       | 3        |      |
|                                 |                                                                 |        | 4.5                  | 3                | 3       | 3        |      |
|                                 |                                                                 |        | 6.0                  | 3                | 3       | 3        |      |
| t <sub>h</sub>                  | Minimum Hold Time,<br>Clock to Reset (HC163A Only)              | 7      | 2.0                  | 3                | 3       | 3        | ns   |
|                                 |                                                                 |        | 3.0                  | 3                | 3       | 3        |      |
|                                 |                                                                 |        | 4.5                  | 3                | 3       | 3        |      |
|                                 |                                                                 |        | 6.0                  | 3                | 3       | 3        |      |
| t <sub>h</sub>                  | Minimum Hold Time,<br>Clock to Enable T or Enable P             | 9      | 2.0                  | 3                | 3       | 3        | ns   |
|                                 |                                                                 |        | 3.0                  | 3                | 3       | 3        |      |
|                                 |                                                                 |        | 4.5                  | 3                | 3       | 3        |      |
|                                 |                                                                 |        | 6.0                  | 3                | 3       | 3        |      |
| t <sub>rec</sub>                | Minimum Recovery Time,<br>Reset Inactive to Clock (HC161A Only) | 5      | 2.0                  | 80               | 95      | 110      | ns   |
|                                 |                                                                 |        | 3.0                  | 35               | 40      | 50       |      |
|                                 |                                                                 |        | 4.5                  | 15               | 20      | 26       |      |
|                                 |                                                                 |        | 6.0                  | 12               | 17      | 23       |      |
| t <sub>rec</sub>                | Minimum Recovery Time,<br>Load Inactive to Clock                | 8      | 2.0                  | 80               | 95      | 110      | ns   |
|                                 |                                                                 |        | 3.0                  | 35               | 40      | 50       |      |
|                                 |                                                                 |        | 4.5                  | 15               | 20      | 26       |      |
|                                 |                                                                 |        | 6.0                  | 12               | 17      | 23       |      |
| t <sub>w</sub>                  | Minimum Pulse Width,<br>Clock                                   | 4      | 2.0                  | 60               | 75      | 90       | ns   |
|                                 |                                                                 |        | 3.0                  | 25               | 30      | 40       |      |
|                                 |                                                                 |        | 4.5                  | 12               | 15      | 18       |      |
|                                 |                                                                 |        | 6.0                  | 10               | 13      | 15       |      |
| t <sub>w</sub>                  | Minimum Pulse Width,<br>Reset (HC161A Only)                     | 5      | 2.0                  | 60               | 75      | 90       | ns   |
|                                 |                                                                 |        | 3.0                  | 25               | 30      | 40       |      |
|                                 |                                                                 |        | 4.5                  | 12               | 15      | 18       |      |
|                                 |                                                                 |        | 6.0                  | 10               | 13      | 15       |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times                               |        | 2.0                  | 1000             | 1000    | 1000     | ns   |
|                                 |                                                                 |        | 3.0                  | 800              | 800     | 800      |      |
|                                 |                                                                 |        | 4.5                  | 500              | 500     | 500      |      |
|                                 |                                                                 |        | 6.0                  | 400              | 400     | 400      |      |

# MC74HC161A, MC74HC163A

## FUNCTION DESCRIPTION

The HC161A/163A are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC161A and HC163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

### INPUTS

#### Clock (Pin 2)

The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading, occur with the rising edge of the Clock input.

#### Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (Pin 3) is the least-significant bit and P3 (Pin 6) is the most-significant bit.

### OUTPUTS

#### Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least-significant bit and Q3 (Pin 11) is the most-significant bit.

#### Ripple Carry Out (Pin 15)

When the counter is in its maximum state, 1111, this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \cdot Q0 \cdot Q1 \cdot Q2 \cdot Q3$$

### OUTPUT STATE DIAGRAMS

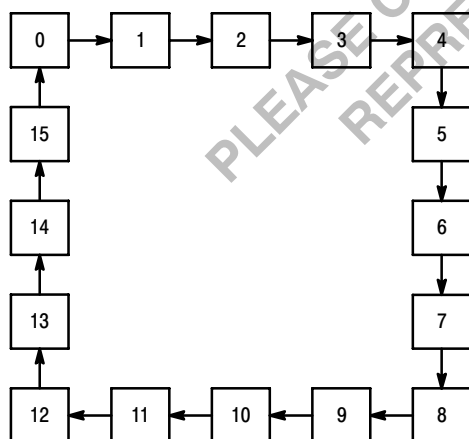


Figure 3. Binary Counters

### CONTROL FUNCTIONS

#### Resetting

A low level on the Reset pin (Pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC161A resets asynchronously, and the HC163A resets with the rising edge of the Clock input (synchronous reset).

#### Loading

With the rising edge of the Clock, a low level on Load (Pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

#### Count Enable/Disable

These devices have two count-enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

Table 1. Count Enable/Disable

| Control Inputs |          |          | Result at Outputs |                              |
|----------------|----------|----------|-------------------|------------------------------|
| Load           | Enable P | Enable T | Q0 – Q3           | Ripple Carry Out             |
| H              | H        | H        | Count             | High when Q0–Q3 are maximum* |
| L              | H        | H        | No Count          |                              |
| X              | L        | H        | No Count          | High when Q0–Q3 are maximum* |
| X              | X        | L        | No Count          | L                            |

\*Q0 through Q3 are maximum when Q3, Q2, Q1, Q0 = 1111.

# MC74HC161A, MC74HC163A

## SWITCHING WAVEFORMS

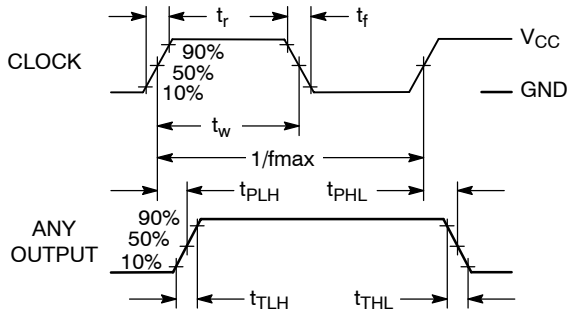


Figure 4.

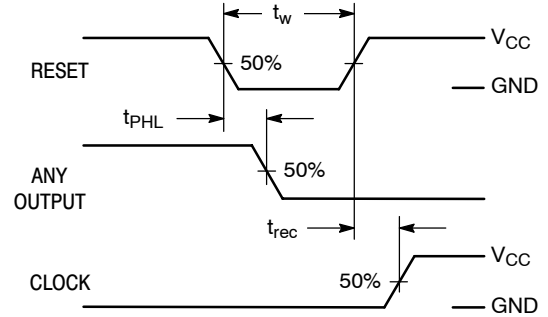


Figure 5.

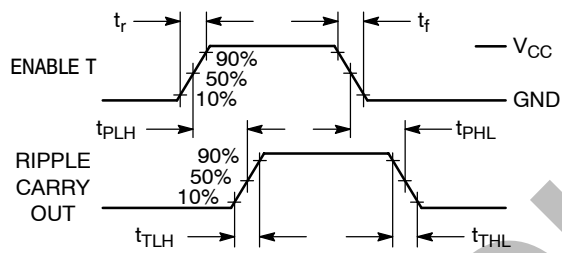


Figure 6.

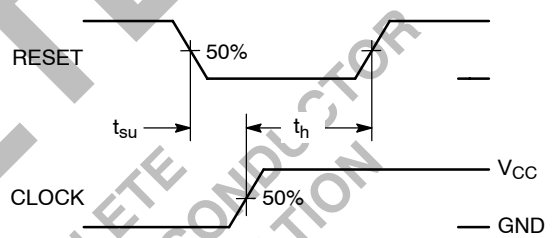


Figure 7. HC163A Only

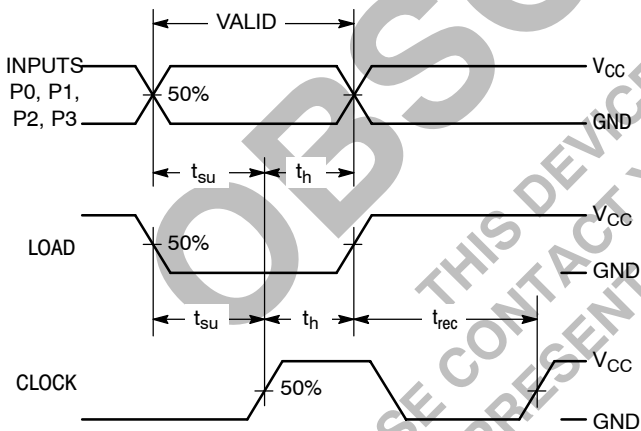


Figure 8.

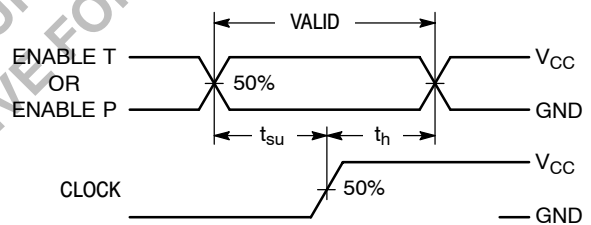
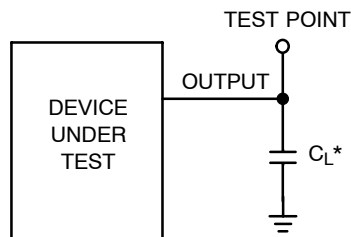


Figure 9.

## TEST CIRCUIT



\*Includes all probe and jig capacitance

Figure 10.

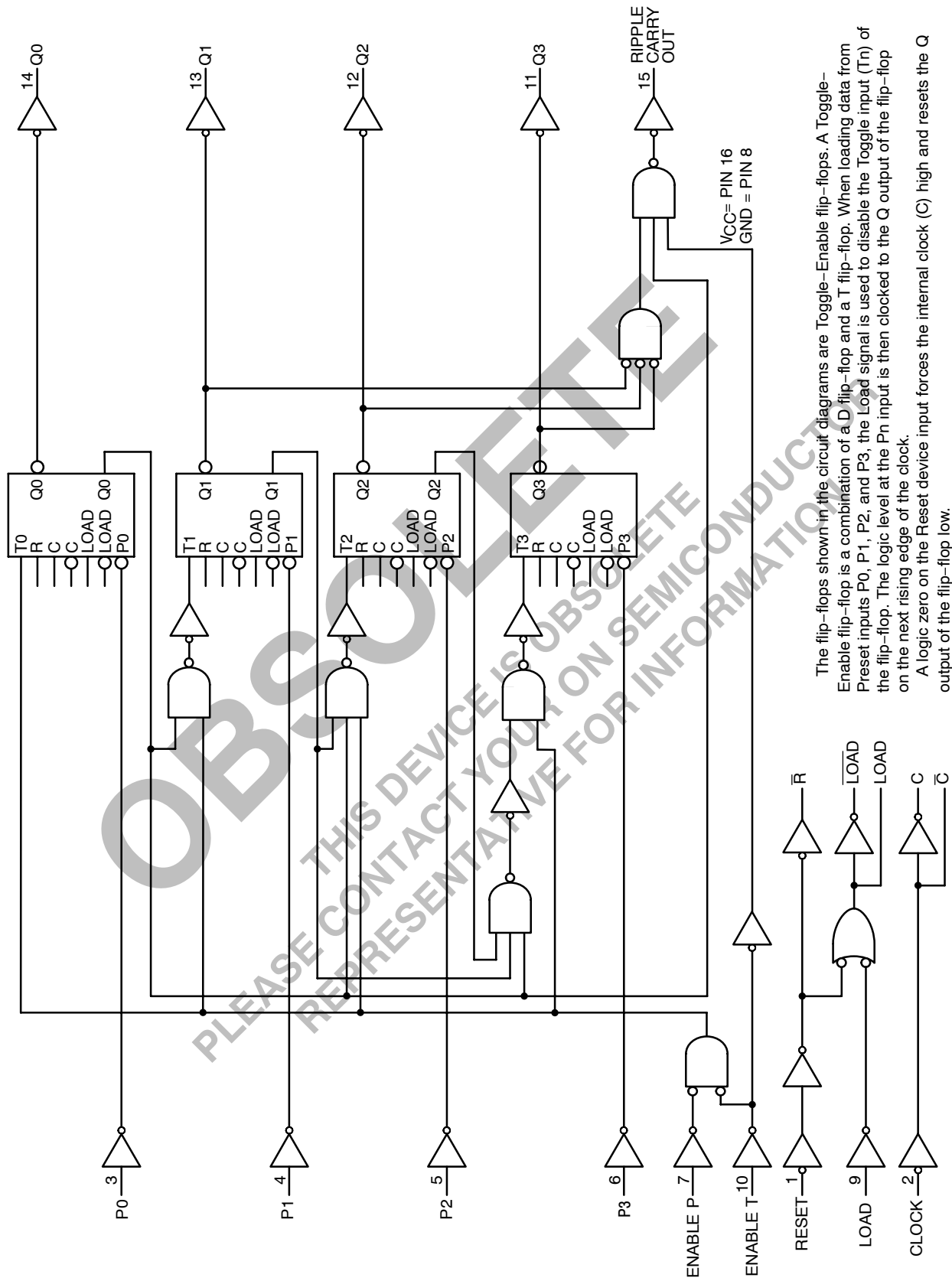


Figure 11. 4-Bit Binary Counter with Asynchronous Reset (MC74HC161A)

## MC74HC161A, MC74HC163A

Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.

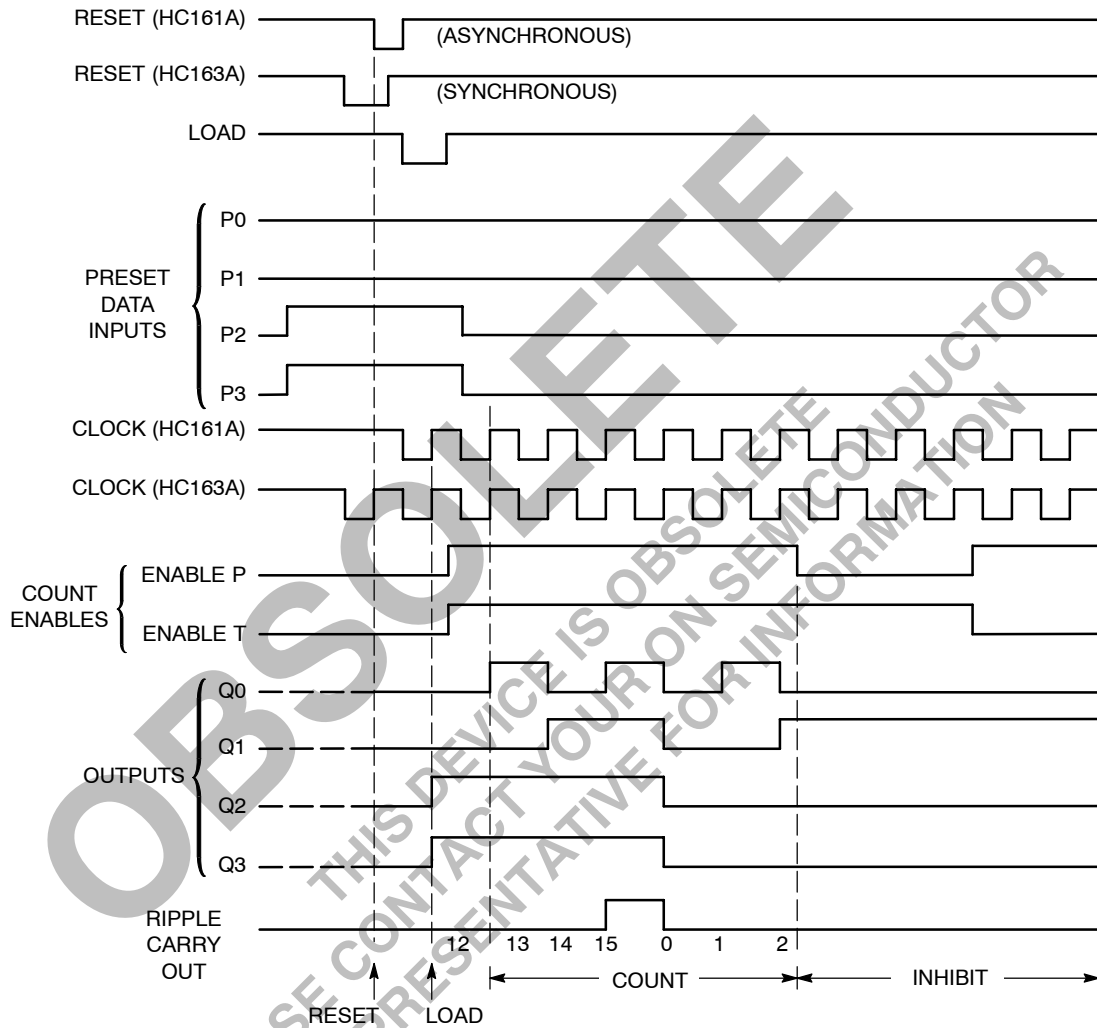


Figure 12. Timing Diagram

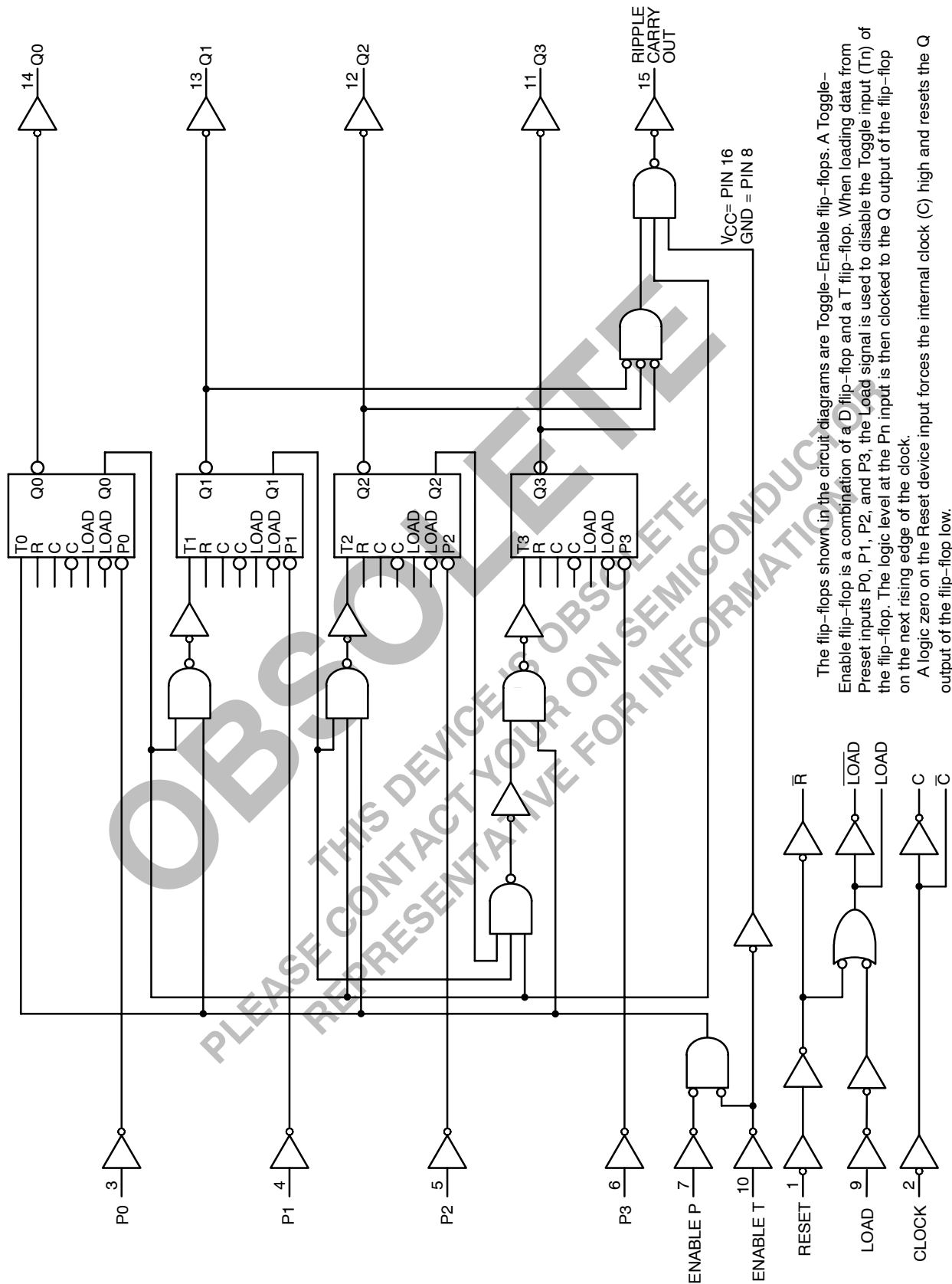
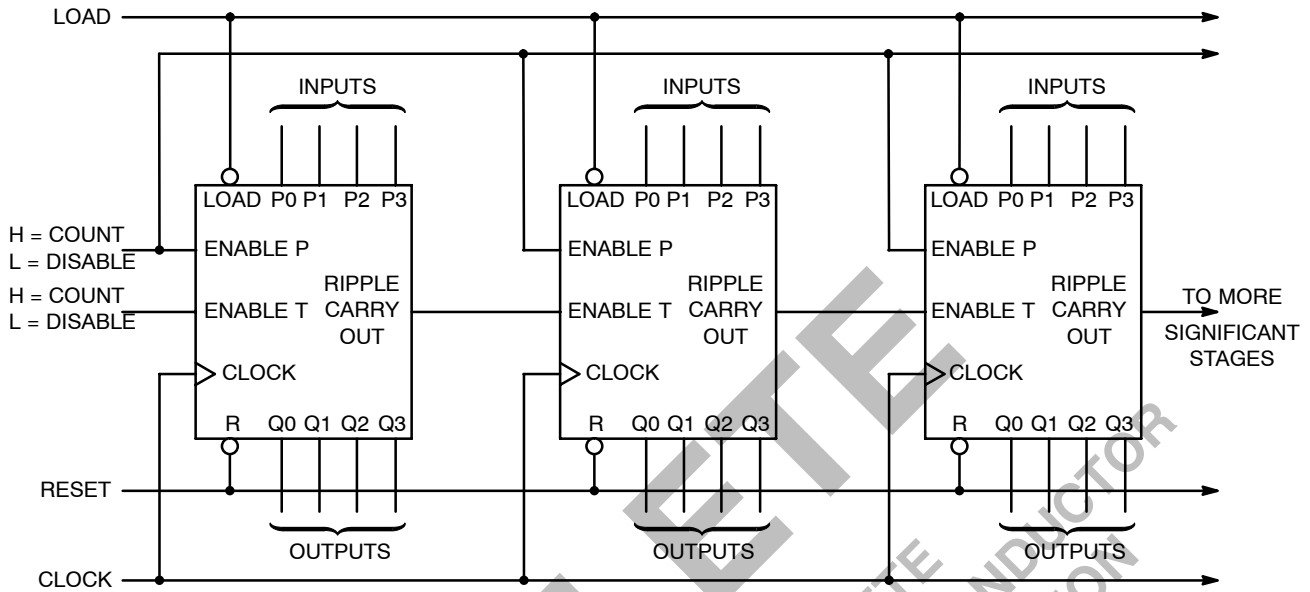


Figure 13. 4-Bit Binary Counter with Synchronous Reset (MC74HC163A)

# MC74HC161A, MC74HC163A

## TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock  $f_{max}$  guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Figure 14. N-Bit Synchronous Counters

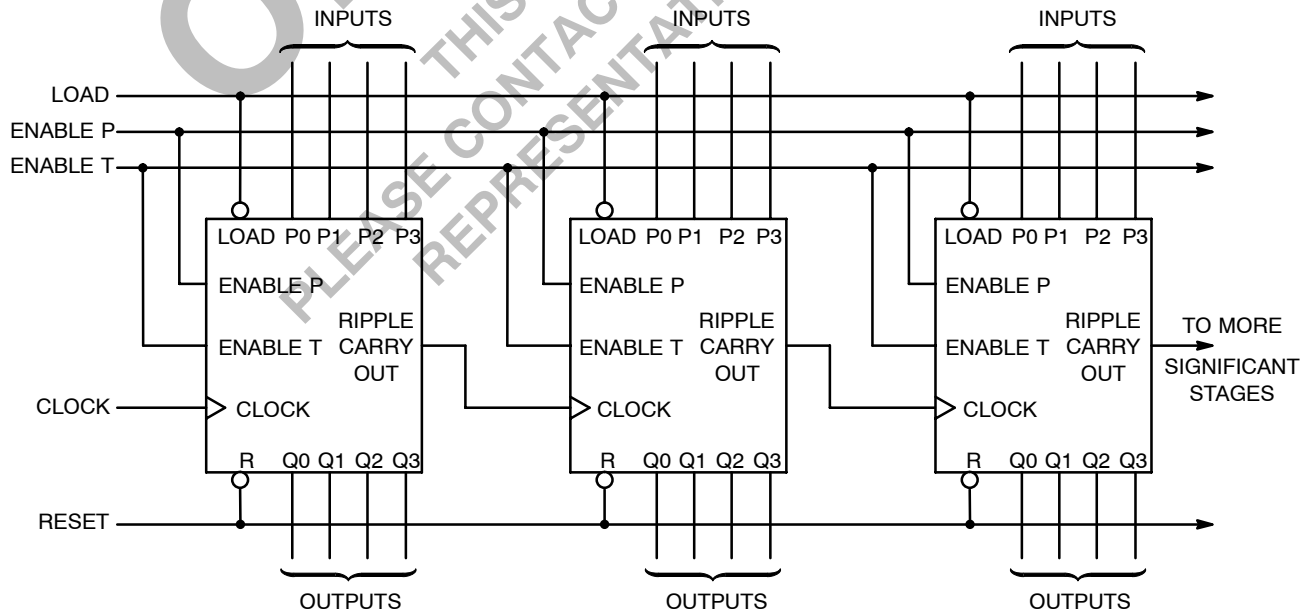


Figure 15. Nibble Ripple Counter

# MC74HC161A, MC74HC163A

## TYPICAL APPLICATIONS VARYING THE MODULUS

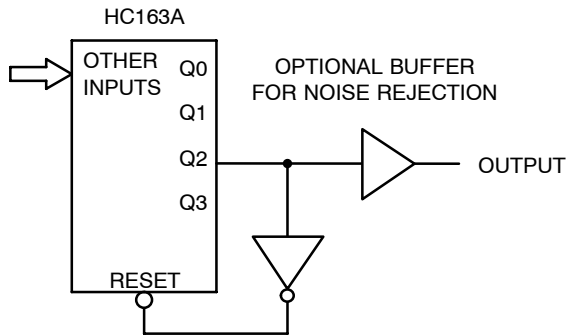


Figure 16. Modulo-5 Counter

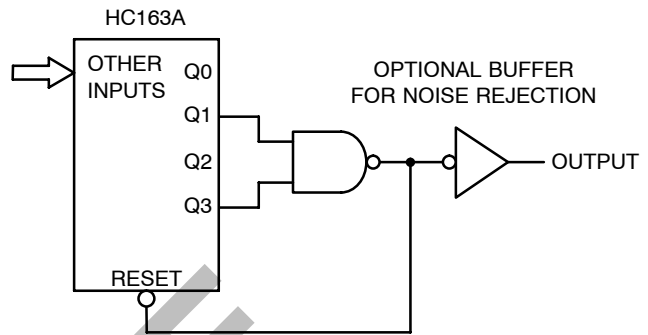


Figure 17. Modulo-11 Counter

The HC163A facilitates designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.

### ORDERING INFORMATION

| Device         | Package              | Shipping <sup>†</sup>    |
|----------------|----------------------|--------------------------|
| MC74HC161AN    | PDIP-16              | 500 Units / Box          |
| MC74HC161ANG   | PDIP-16<br>(Pb-Free) | 500 Units / Box          |
| MC74HC161AD    | SOIC-16              | 48 Units / Rail          |
| MC74HC161ADG   | SOIC-16<br>(Pb-Free) | 48 Units / Rail          |
| MC74HC161ADR2  | SOIC-16              | 2500 Units / Tape & Reel |
| MC74HC161ADR2G | SOIC-16<br>(Pb-Free) | 2500 Units / Tape & Reel |
| MC74HC161AFEL  | SOEIAJ-16            | 2000 Units / Tape & Reel |
| MC74HC161ADTR2 | TSSOP-16*            | 2500 Units / Tape & Reel |
| MC74HC163AN    | PDIP-16              | 500 Units / Box          |
| MC74HC163ANG   | PDIP-16<br>(Pb-Free) | 500 Units / Box          |
| MC74HC163AD    | SOIC-16              | 48 Units / Rail          |
| MC74HC163ADG   | SOIC-16<br>(Pb-Free) | 48 Units / Rail          |
| MC74HC4163DR2  | SOIC-16              | 2500 Units / Tape & Reel |
| MC74HC163ADR2G | SOIC-16<br>(Pb-Free) | 2500 Units / Tape & Reel |
| MC74HC163AFEL  | SOEIAJ-16            | 2000 Units / Tape & Reel |

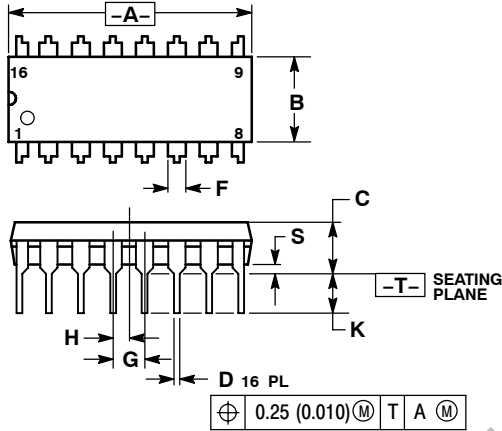
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HC161A, MC74HC163A

## PACKAGE DIMENSIONS

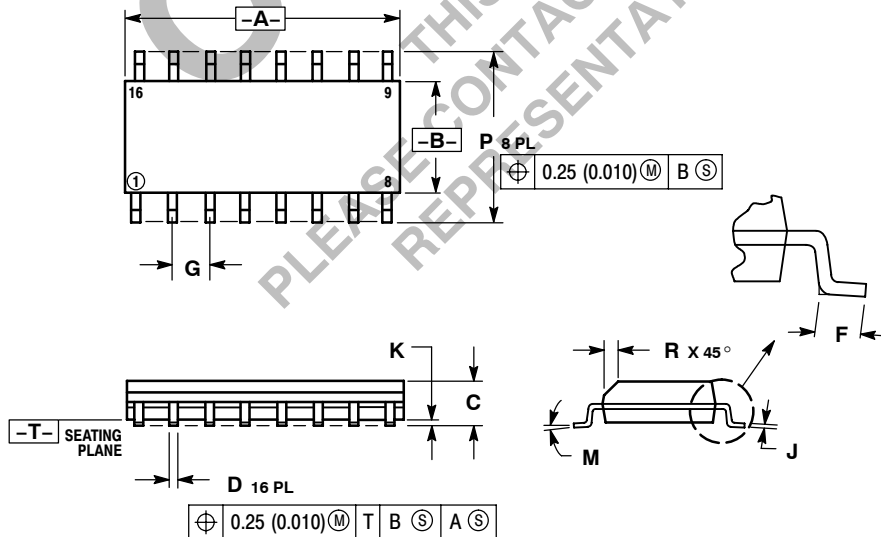
PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



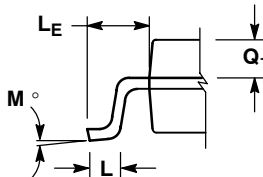
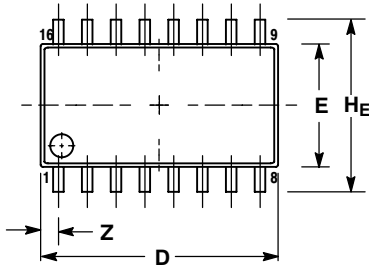
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

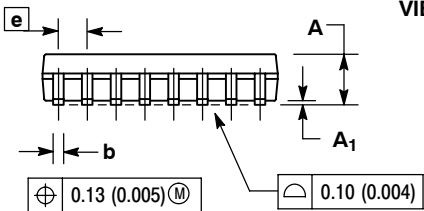
# MC74HC161A, MC74HC163A

## PACKAGE DIMENSIONS

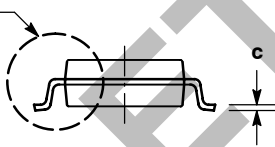
SOEIAJ-16  
F SUFFIX  
CASE 966-01  
ISSUE O



DETAIL P



VIEW P



### NOTES:

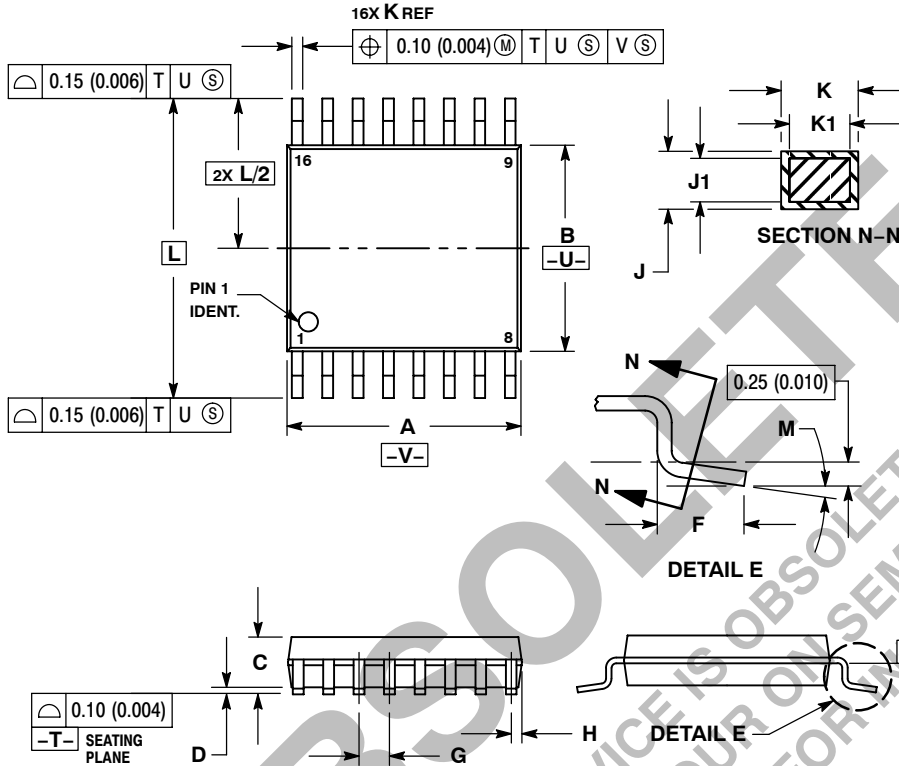
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

# MC74HC161A, MC74HC163A

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

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