

Evaluating the AD7450A and AD7451

FEATURES

Full-featured evaluation board for the **AD7450A** and **AD7451**
PC control in conjunction with the system demonstration
platform (**EVAL-SDP-CB1Z**)

PC software for control and data analysis (time and
frequency domain)

Standalone capability

EVALUATION KIT CONTENTS

EVAL-AD7450ASDZ/EVAL-AD7451SDZ evaluation board

Evaluation software CD for the **AD7450A/AD7451**

9 V mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

System demonstration platform (**EVAL-SDP-CB1Z**)

Precision analog signal source

SMB cables

USB cables

GENERAL DESCRIPTION

The **EVAL-AD7450ASDZ/EVAL-AD7451SDZ** is a full-featured evaluation board designed to allow the user to easily evaluate all features of the **AD7450A** and **AD7451**. The evaluation board

can be controlled via the system demonstration platform (SDP) connector (J8). The **EVAL-SDP-CB1Z** board allows the evaluation board to be controlled via the USB port of a PC using the **AD7450A/AD7451** evaluation software.

The **EVAL-AD7450ASDZ/EVAL-AD7451SDZ** generates all required power supplies on board and supplies power to the **EVAL-SDP-CB1Z** controller board. On-board components include the following:

- **AD8599**: Ultralow distortion, ultralow noise op amp (dual)
- **ADP1613**: Step-up PWM dc-to-dc switching converter
- **ADP3303-5**: High accuracy anyCAP™ 200 mA low dropout linear regulator
- **ADP1720**: 50 mA, high voltage, micropower linear regulator
- **ADP7104**: 20 V, 500 mA, low noise, CMOS LDO
- **ADM1185**: Quad voltage monitor and sequencer
- **ADG3308**: Low voltage, 1.15 V to 5.5 V, 8-channel bidirectional logic level translator
- **ADR431**: Ultralow noise XFET® voltage reference with current sink and source capability

Various link options are described in the Evaluation Board Hardware section.

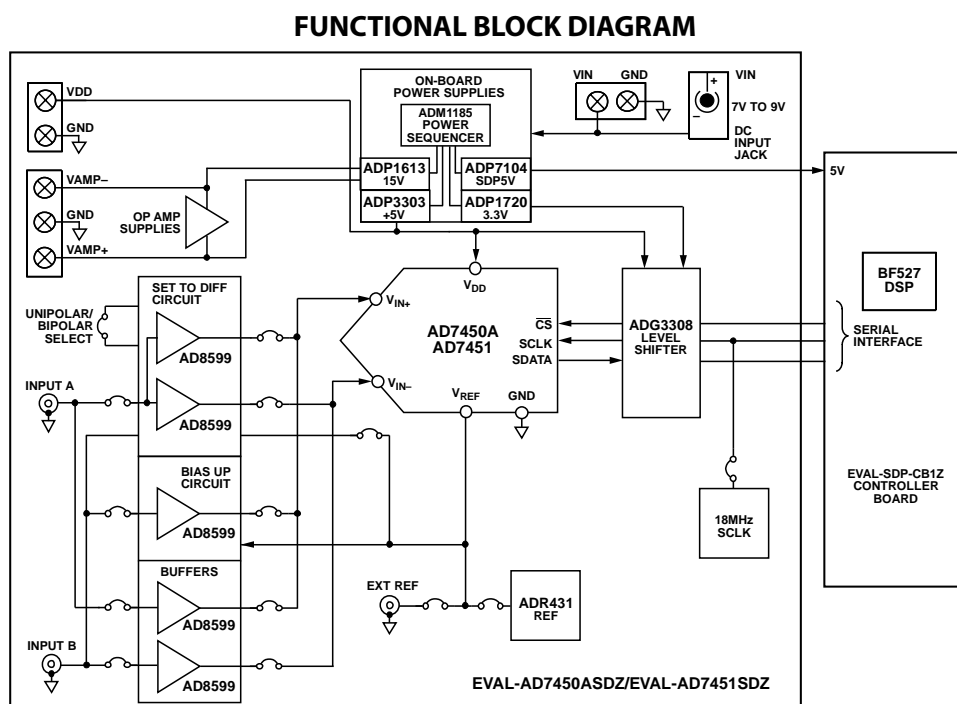


Figure 1.

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REVISION HISTORY

4/13—Rev. 0 to Rev. A

Replaced EVAL-AD7440/AD7450A and EVAL-AD7441/AD7451
with EVAL-AD7450A/EVAL-AD7451 Universal
Updated Format..... Universal
Replaced All Sections, Tables, and Figures Universal

3/07—EVAL-AD7440/AD7450A Revision 0: Initial Version

12/06—EVAL-AD7441/AD7451 Revision 0: Initial Version

GETTING STARTED

QUICK START STEPS

To install the software do the following:

1. Install the [AD7450A/AD7451](#) software from the enclosed CD.
Ensure that the [EVAL-SDP-CB1Z](#) board is not connected from the USB port of the PC while installing the software. The PC must be restarted after the installation.
2. Connect the [EVAL-SDP-CB1Z](#) board to the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) board as shown in Figure 2. Screw the two boards together with the enclosed nylon screw-nut set to ensure the boards connect firmly together.
3. Connect the 9 V power supply adapter included in the kit to connector J702 on the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) board.
4. Connect the [EVAL-SDP-CB1Z](#) board to the PC via the USB cable. For Windows® XP, you may need to search for the [EVAL-SDP-CB1Z](#) drivers. Choose to automatically search for the drivers for the [EVAL-SDP-CB1Z](#) board if prompted by the operating system.
5. Launch the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) software from the **Analog Devices** subfolder in the **Programs** menu.

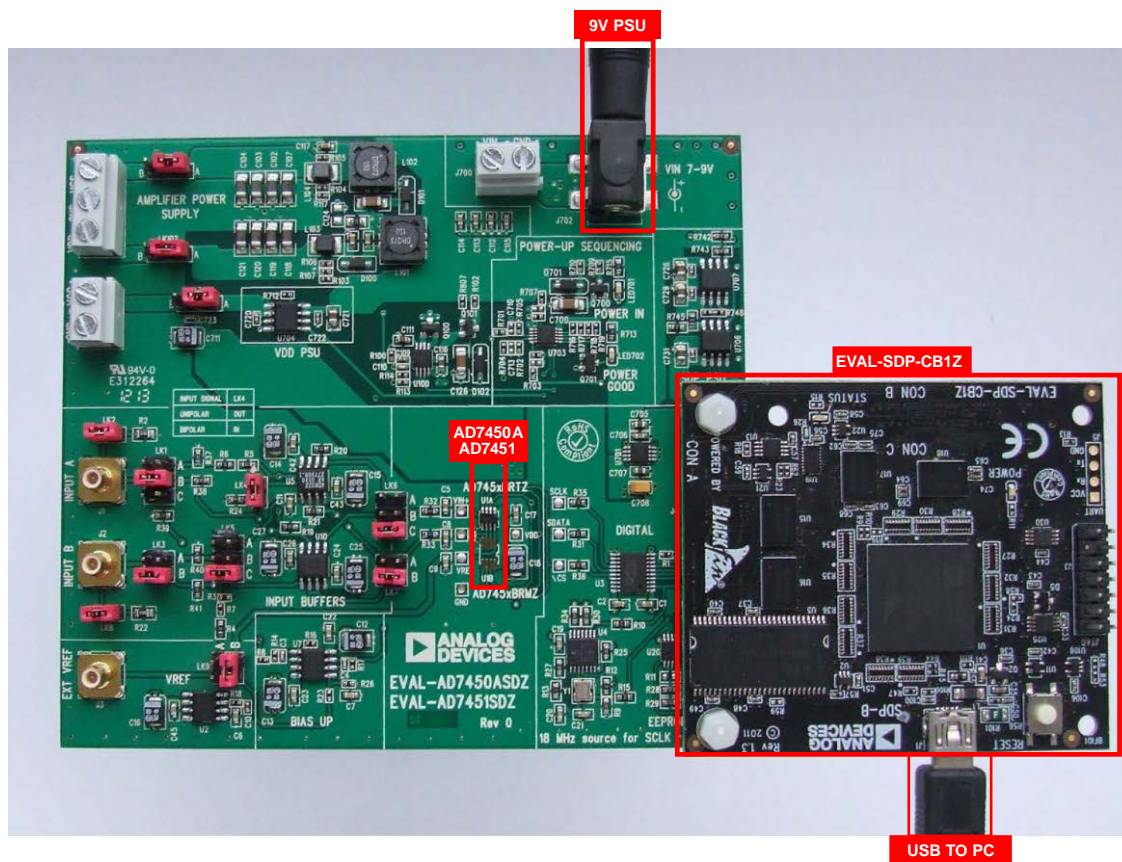


Figure 2. Hardware Configuration—Setting Up the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#)

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SOFTWARE INSTALLATION PROCEDURES

The [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the install. The default location for the software is **C:\Program Files\Analog Devices\AD7450A/AD7451**.

There are two parts to the installation:

- [AD7450A/AD7451](#) evaluation board software installation
- [EVAL-SDP-CB1Z](#) system demonstration platform board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and [EVAL-SDP-CB1Z](#) board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

Installing the [AD7450A/AD7451](#) Evaluation Board Software

To install the [AD7450A/AD7451](#) evaluation board software,

1. With the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the **setup.exe** file to begin the evaluation board software installation. The software is installed to the following default location: **C:\Program Files\Analog Devices\AD7450A/AD7451**.
3. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.

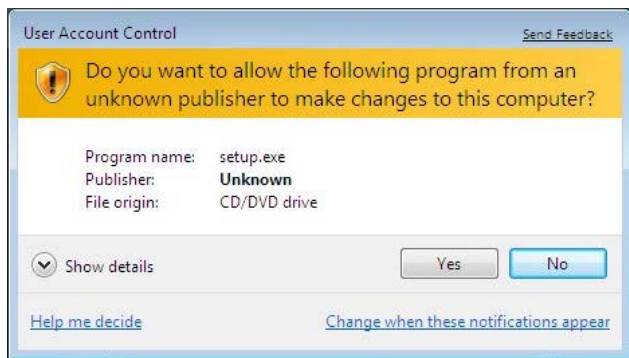


Figure 3. [AD7450A/AD7451](#) Evaluation Board Software Installation: Granting Permission for Program to Make Changes

4. Select the location to install the software, and then click **Next**.

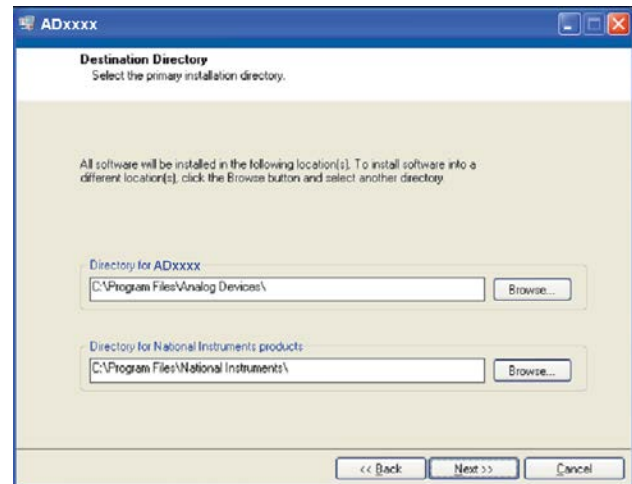


Figure 4. [AD7450A/AD7451](#) Evaluation Board Software Installation: Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, and then select **I accept the License Agreement** and click **Next**.



Figure 5. [AD7450A/AD7451](#) Evaluation Board Software Installation: Accepting the License Agreement

- A summary of the installation is displayed. Click **Next** to continue.

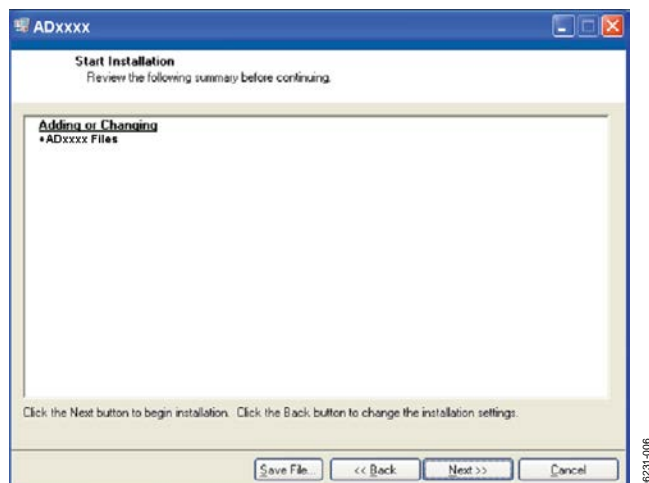


Figure 6. AD7450A/AD7451 Evaluation Board Software Installation: Reviewing a Summary of the Installation

- A dialog box informs you when the installation is complete. Click **Next**.

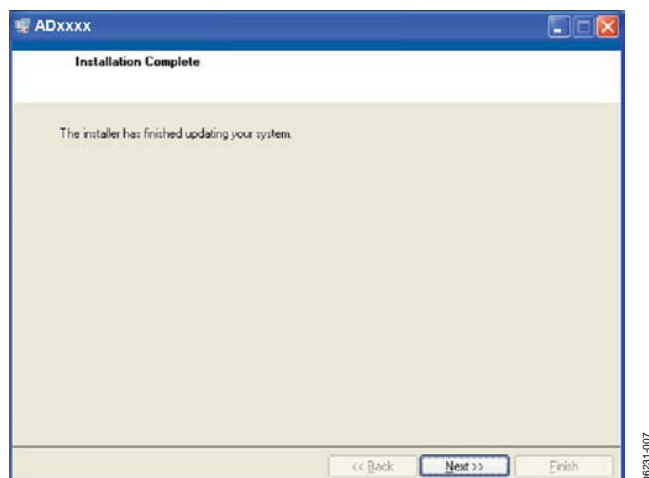


Figure 7. AD7450A/AD7451 Evaluation Board Software Installation: Indicating When the Installation Is Complete

Installing the EVAL-SDP-CB1Z System Demonstration Platform Board Drivers

After the installation of the evaluation board software is complete, a welcome window is displayed for the installation of the EVAL-SDP-CB1Z system demonstration platform board drivers.

- With the EVAL-SDP-CB1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click **Next**.



Figure 8. EVAL-SDP-CB1Z Drivers Setup

- Select the location to install the drivers, and then click **Next**.

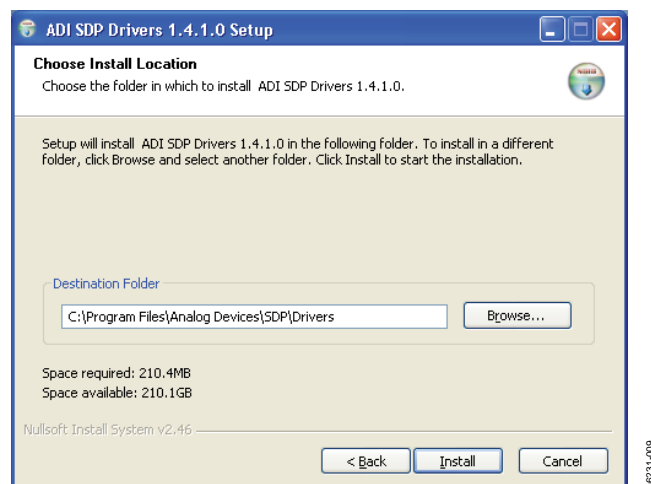


Figure 9. EVAL-SDP-CB1Z Drivers Setup: Selecting the Location for Drivers Installation

3. Click **Install** to confirm that you would like to install the drivers.

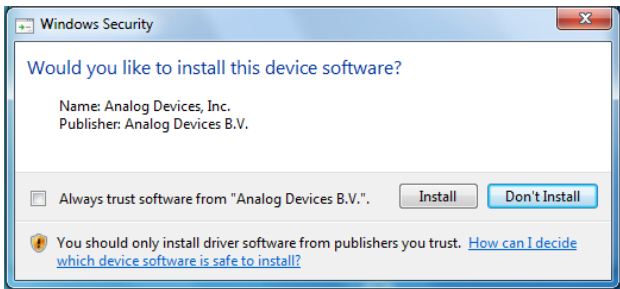


Figure 10. EVAL-SDP-CB1Z Drivers Setup:
Granting Permission to Install Drivers

4. To complete the drivers installation, click **Finish**, which closes the installation wizard.



Figure 11. EVAL-SDP-CB1Z Drivers Setup:
Completing the Drivers Setup Wizard

5. Before using the evaluation board, you must restart your computer. A dialog box opens, giving you the following options: **Restart**, **Shut Down**, **Restart Later**. Click the appropriate button.

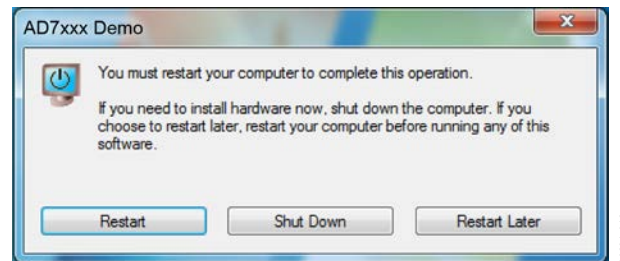


Figure 12. EVAL-SDP-CB1Z Drivers Setup:
Restarting the Computer

EVALUATION BOARD SETUP PROCEDURES

The AD7450A/AD7451 evaluation board connects to the (EVAL-SDP-CB1Z) system demonstration board. The EVAL-SDP-CB1Z board is the controller board, which is the communication link between the PC and the main evaluation board. Figure 2 shows a photograph of the connections made between the AD7450A/AD7451 daughter board and the EVAL-SDP-CB1Z board.

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

Configuring the Evaluation and SDP Boards

1. Connect the EVAL-AD7450ASDZ/EVAL-AD7451SDZ board to Connector A or Connector B on the EVAL-SDP-CB1Z board.
 - a. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
2. Connect the power supplies on the EVAL-AD7450ASDZ/EVAL-AD7451SDZ board to the J702 connector on the EVAL-AD7450ASDZ/EVAL-AD7451SDZ board. (Alternatively, a bench power supply may be used to power the EVAL-AD7450ASDZ/EVAL-AD7451SDZ via J700. See Table 1 for more information about the connections and options for the required power supplies.)
3. Connect the EVAL-SDP-CB1Z board to the PC via the USB cable enclosed in the EVAL-SDP-CB1Z kit. If using Windows XP platform, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.

EVALUATION BOARD HARDWARE

AD7450A/AD7451 DEVICE DESCRIPTION

The [AD7450A/AD7451](#) are 12-bit high speed, low power, successive approximation (SAR) analog-to-digital converters with a fully differential/pseudo differential analog input. The parts operate from a single 3 V or 5 V power supply and use advanced design techniques to achieve very low power dissipation at throughput rates up to 1 MSPS. The SAR architecture ensures that there are no pipeline delays.

POWER SUPPLIES

Take care before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode.

When using the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) in conjunction with the [EVAL-SDP-CB1Z](#) board, connect the ac transformer to Connector J702. V_{CC} , V_{DD} , V_{SS} , and V_{DRIVE} are generated on board. Alternatively, a bench power supply may be connected to J700 to supply 7 V to 9 V.

Table 1. External Power Supply Required

Power Supply	Connector	Voltage Range	Purpose
V_{IN} ¹	J700 or J702	7 V to 9 V	Supplies all on-board power supplies, which generate all required voltages to run the evaluation board.
V_{DD}	J100	+12 V to +16.5 V	Amplifier positive supply.
V_{SS}	J100	−12 V to −16.5 V	Amplifier negative supply.
V_{CC}	J703	4.75 V to 5.25 V	V_{DD} digital supply.

¹ When V_{IN} is supplied, all other power supplies are available on board. If this supply is not used, then all other supplies must be sourced from an external source.

LINK CONFIGURATION OPTIONS

There are 12 link options that must be set for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 2, which shows the position in which all the links are set when the evaluation board is packaged. Jumper and solder link (LKx)

options must be set correctly to select the appropriate operating setup before using the evaluation board. The default link positions are shown in Table 3 and Table 4 and the functions of these options are outlined in Table 2.

Table 2. Link Options

Link No.	Function
LK1	INPUT A destination selection. This selects which buffer INPUT A is connected to. Position A: INPUT A is connected to single-ended to differential buffer. Position B: INPUT A is connected to single-ended buffer (U10-A). Position C: INPUT A is connected to bias up circuit (U7-A/U7-B).
LK2	INPUT A input impedance selection. Insert: INPUT A input impedance is 51 Ω .
LK3	INPUT B destination selection. This selects which buffer INPUT B is connected to. Position A: INPUT B is connected to LK5 Position B. Position B: INPUT B is connected to single-ended buffer (U10-B).
LK4	Input signal selection. Insert when input signal at INPUT A is bipolar. Remove when input signal at INPUT A is unipolar.
LK5	This selects the source for the positive terminal of U5-B. Position A: $\frac{1}{2} V_{REF}$ is supplied to U5-B. Position B: INPUT B is supplied to U5-B. Position C: 0 V is supplied to U5-B.
LK6	VIN+ source selection. Select which buffered signal is routed to AD7450A/AD7451 Pin VIN+. Position A: Signal is sourced from single-ended to differential buffer output (U5-A). Position B: Signal is sourced from single-ended buffer (U10-A). Position C: Signal is sourced from bias up circuit (U7-B).
LK7	VIN– source selection. Select which buffered signal is routed to AD7450A/AD7451 Pin VIN–. Position A: Signal is sourced from single-ended to differential buffer output (U5-B). Position B: Signal is sourced from single-ended buffer (U10-B).
LK8	INPUT B input impedance selection. Insert: INPUT B input impedance is 51 Ω .
LK9	VREF source selection. Position A: VREF is sourced from U2 (ADR431 an ultralow noise XFET® voltage reference). Position B: VREF is sourced externally via SMB connector EXT_VREF.
LK101 ¹	Amplifier negative voltage supply selection. Position A: Amplifier negative voltage supplied from on-board supply. Position B: Amplifier negative voltage supplied from external source via J100 Terminal 1 labeled VSS.
LK102 ¹	Amplifier positive voltage selection. Position A: Amplifier positive voltage supplied from on board supply. Position B: Amplifier positive voltage supplied from external source via J100 Terminal 3 labeled VDD.
LK701	VDD supply for AD7450A/AD7451 . Position A: VDD supplied from on board supply (5 V). Position B: VDD supplied from external source via J703 terminal labeled VCC.

¹ Both LK101 and LK102 should always be in corresponding positions.

Table 3. Link Options—Setup Conditions for [AD7450A](#)

Link No.	Position	Function
LK1	A	INPUT A is connected to single-ended to differential converter (U5-A).
LK2	Inserted	INPUT A input impedance is 51 Ω .
LK3	B	INPUT B is connected to single-ended buffer (U10-B).
LK4	Inserted	Input signal at INPUT A is bipolar.
LK5	C	$V_{REF}/2$ is supplied to U5-B.
LK6	A	Signal is sourced from single-ended to differential converter (U5-A).
LK7	A	Signal is sourced from single-ended to differential converter (U5-B).
LK8	Inserted	INPUT B input impedance is 51 Ω .
LK9	B	V_{REF} is sourced from U2.
LK101	A	Amplifier negative voltage supplied from an on-board supply.
LK102	A	Amplifier positive voltage supplied from an on-board supply.
LK701	A	V_{DD} supplied from on-board supply (5 V).

Table 4. Link Options—Setup Conditions for [AD7451](#)

Link No.	Position	Function
LK1	C	INPUT A is connected to bias up circuit (U7).
LK2	Inserted	INPUT A input impedance is 51 Ω .
LK3	B	INPUT B is connected to single-ended buffer (U10-B).
LK4	Inserted	Input signal at INPUT A is bipolar.
LK5	C	$V_{REF}/2$ is supplied to U5-B.
LK6	C	Signal is sourced from bias up circuit (U7-B).
LK7	B	Signal is sourced from input buffer (U10-B).
LK8	Inserted	INPUT B input impedance is 51 Ω .
LK9	B	V_{REF} is sourced from U2.
LK101	A	Amplifier negative voltage supplied from an on-board supply.
LK102	A	Amplifier positive voltage supplied from an on-board supply.
LK701	A	V_{DD} supplied from an on-board supply (5 V).

EVALUATION BOARD CIRCUITRY

ANALOG INPUTS

Three buffer circuits are available as follows.

Single-Ended to Differential

A single input signal applied to the INPUT A SMB socket can be used to generate a differential signal.

For bipolar signals, the input range should be $+V_{REF}$ to $-V_{REF}$. LK4 is inserted.

For unipolar signals, the input should be 0 V to V_{REF} . LK4 is removed.

Individual Channel Buffers

INPUT A and INPUT B are used in this configuration. Both inputs are buffered individually. The outputs from these amplifiers are available to the [AD7450A/AD7451](#) V_{IN+} and V_{IN-} inputs via low-pass RC filter networks.

Level Shifter

The analog inputs on the [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) are filtered and buffered by an [AD8599](#). The outputs from this amplifier are available to the [AD7450A/AD7451](#) V_{IN+} input via low-pass RC filter network.

REFERENCE OPTIONS

The reference source can be from an [ADR431](#) ultralow noise XFET® voltage references with current sink and source capability (U2). An external reference voltage may also be applied to J3 EXT_REF.

SOCKETS/CONNECTORS

Table 5. Socket Connector Functions

Socket	Function
J1 INPUT A	Input. This is routed to a selection of input buffers.
J2 INPUT B	Input. This is routed to a selection of input buffers.
J3 EXT_REF	External reference connection point.
J4	EVAL-SDP-CB1Z evaluation board controller socket.
J100 VSS and VDD	Screw terminal connectors for external amplifier power supplies.
J700	7 V to 9 V bench supply screw terminal connector.
J702	7 V to 9 V dc transformer power connector.
J703 VCC	External power supply for V_{DD} of the AD7450A/AD7451 .

MODES OF OPERATION

SERIAL INTERFACE

The [AD7450A/AD7451](#) use a high speed serial interface which allows sampling rates up to 1 MSPS. For details on the operation of the serial bus, refer to the [AD7450A](#) and [AD7451](#) data sheets.

The [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) communicates with the [EVAL-SDP-CB1Z](#) board using level shifters. The [EVAL-SDP-CB1Z](#) operates at a 3.3 V logic level. This allows VDRIVE voltages exceeding 3.3 V to be used without damaging the SDP interface.

Details of the serial interface can be found in the [AD7450A](#) and [AD7451](#) data sheets.

STANDALONE MODE

The [EVAL-AD7450ASDZ/EVAL-AD7451SDZ](#) may also be used without the [EVAL-SDP-CB1Z](#). In this case, connect to the digital interface via the test-point connectors.

Remove R31, R35, and R36 to isolate the [AD7450A/AD7451](#) from the SDP interface circuitry.

HOW TO USE THE SOFTWARE FOR EVALUATING THE AD7450A/AD7451

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Setup Procedures sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the **EVAL-SDP-CB1Z** board is plugged into your PC. (If you are using Windows XP, you may need to search for the **EVAL-SDP-CB1Z** drivers. Choose to automatically search for the drivers for the **EVAL-SDP-CB1Z** board if prompted by the operating system.)
2. Check that the board is connected to the PC correctly using the **Device Manager** of the PC.
 - a. Access the **Device Manager** as follows:
 - i. Right-click **My Computer** and then click **Manage**.
 - ii. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.
 - iii. The **Computer Management** box appears. Click **Device Manager** from the list of **System Tools** (see Figure 13).
 - b. **Analog Devices System Development Platform (32MB)** should appear under **ADI Development Tools**, indicating that the **EVAL-SDP-CB1Z** driver software is installed and that the board is connected to the PC correctly.

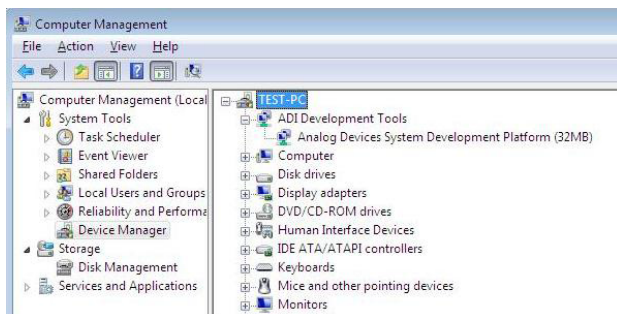


Figure 13. Device Manager:
Checking that the Board Is Connected to the PC Correctly

Launching The Software

After completing the steps in the Setting Up the System for Data Capture section, launch the **AD7450A/AD7451** software as follows:

1. From the **Start** menu, select **Programs > Analog Devices > AD7450A/AD7451**. The main software window appears.
2. If the **AD7450A/AD7451** evaluation system is not connected to the USB port via the **EVAL-SDP-CB1Z** when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

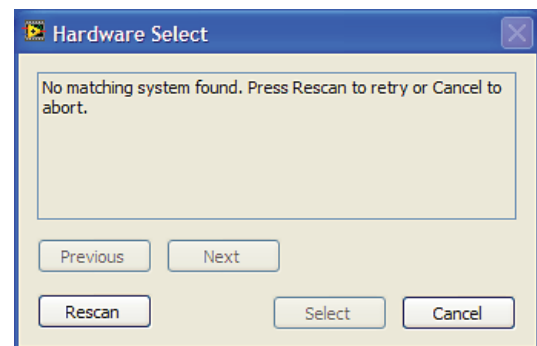
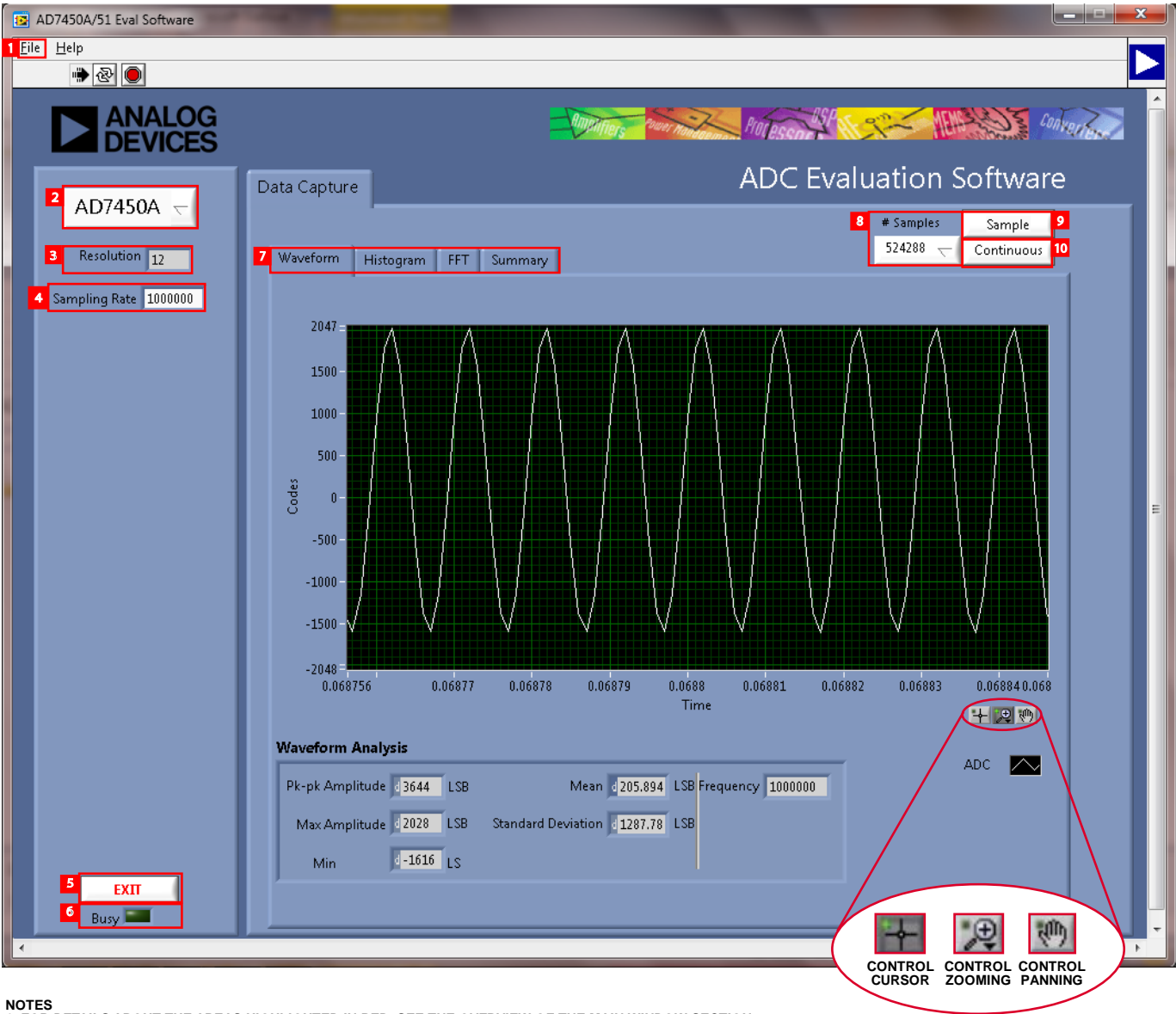


Figure 14. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the evaluation board attached to the PC is detected, and then the main window appears (see Figure 15).



NOTES
1. FOR DETAILS ABOUT THE AREAS HIGHLIGHTED IN RED, SEE THE OVERVIEW OF THE MAIN WINDOW SECTION.

Figure 15. Setup Screen

OVERVIEW OF THE MAIN WINDOW

The main window of the software is shown in Figure 15 and has the features described in this section.

File Menu (Section 1)

The **File** menu (labeled 1 in Figure 15) offers the choice to

- **Load data:** load previously captured data or example files in .tsv (tab separated values) format for analysis (see Figure 16). (The default location for the example files is C:\Program Files\Analog Devices\AD7450A\AD7451\examples.)
- **Save Data as .tsv:** save captured data in .tsv format for future analysis (see Figure 17).
- **Print Front Panel Picture:** print the main window to the default printer.
- **Save Picture:** save the current screen capture.
- **Exit:** quit the application.

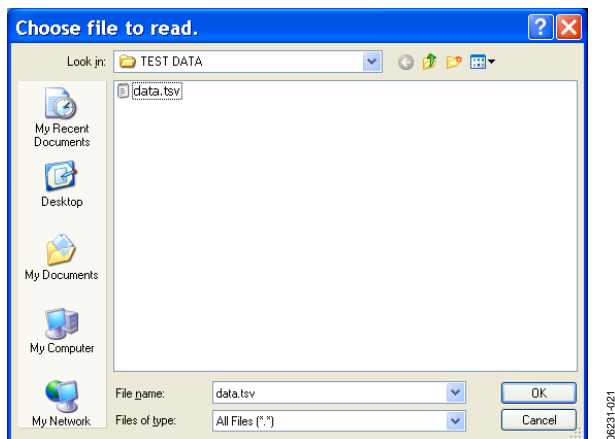


Figure 16. Load File Dialog Box
Loading Previously Captured Data or Example Files in .tsv Format

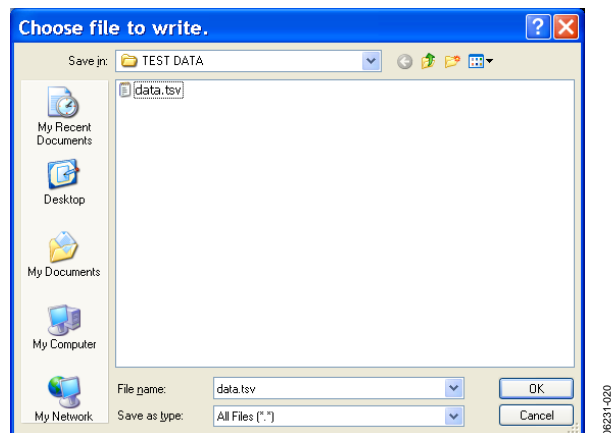


Figure 17. Save File Dialog Box
Saving Data as .tsv

Part Information Box (Section 2)

The **Part Information** box (labeled 2 in Figure 15) displays the generic being evaluated and is for informational purposes only.

Resolution Box (Section 3)

The **Resolution** box (labeled 3 in Figure 15) displays the resolution of the [AD7450A/AD7451](#) in bits.

Sampling Rate Box (Section 4)

The default sampling frequency in the **Sampling Rate** box (labeled 4 in Figure 15) matches the maximum sample rate of the ADC selected from the drop-down menu.

Exit Button (Section 5)

Clicking **Exit** (labeled 5 in Figure 15) closes the software. Alternatively, you can select **Exit** from the **File** menu.

Busy LED (Section 6)

The **Busy LED** (labeled 6 in Figure 15) indicates when a read is in progress from the [EVAL-SDP-CB1Z](#) board.

Tabs Area (Section 7)

There are four tabs available in the tabs area (labeled 7 in Figure 15) of the main window: **Waveform**, **Histogram**, **FFT**, and **Summary**. These tabs display the data in different formats. Navigation tools are provided within each tab to allow you to control the cursor, zooming, and panning (see Figure 15) within the graphs displayed.

Each tab is described in more detail in the Generating a Waveform Analysis Report; Generating a Histogram of the ADC Code Distribution; Generating a Fast Fourier Transform of AC Characteristics; and Generating a Summary of the Waveform, Histogram, and Fast Fourier Transform sections.

Samples Box (Section 8)

The **# Samples** box (labeled 8 in Figure 15) allows you to select the number of samples to analyze. When **Sample** or **Continuous** is clicked, the software requests this number of samples to be taken. This is the total number of samples taken on all channels.

Sample Button (Section 9)

Clicking **Sample** (labeled 9 in Figure 15) performs a single capture, acquiring a set number of samples at the selected sampling rate.

Continuous Button (Section 10)

Clicking **Continuous** (labeled 10 in Figure 15) performs a continuous capture from the ADC. Clicking **Continuous** a second time stops sampling.

GENERATING A WAVEFORM ANALYSIS REPORT

Figure 18 illustrates the waveform capture tab for a 100 kHz sine wave input signal.

The **Waveform Analysis** area (labeled 1 in Figure 18) reports the amplitudes recorded from the captured signal and the frequency of the signal tone.

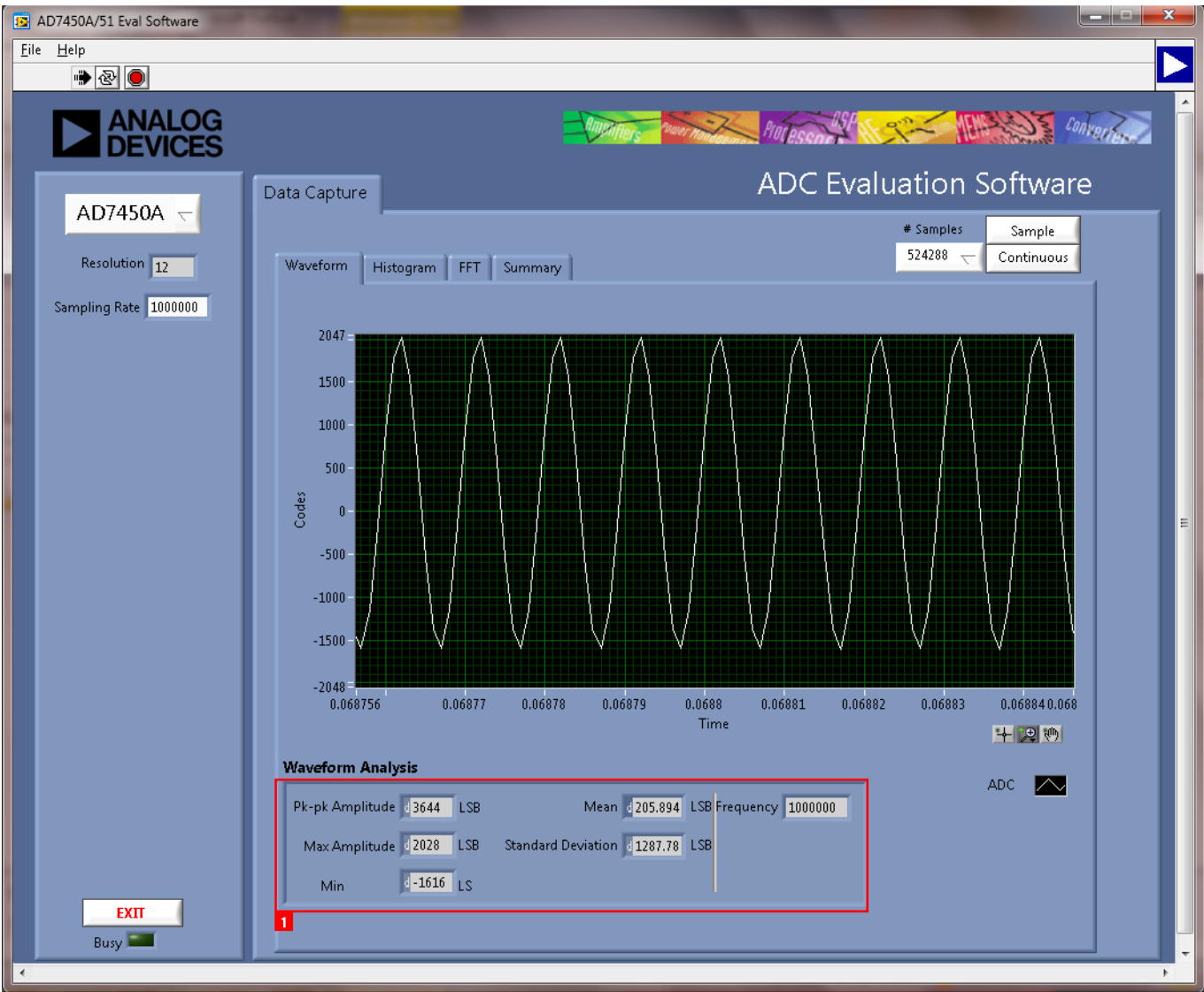


Figure 18. Waveform Tab

GENERATING A HISTOGRAM OF THE ADC CODE DISTRIBUTION

The **Histogram** tab can be used to perform ac testing or, more commonly, dc testing. This tab shows the ADC code distribution of the input and computes the mean and standard deviation, which are displayed as **Mean** and **Transition Noise**, respectively, in the **Histogram Analysis** area (labeled 1 in Figure 19).

AC Input

To perform a histogram test of ac input,

1. Apply a signal source to the J1/J2 input connectors.
2. Click the **Histogram** tab from the main window.
3. Click **Sample**.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

DC Input

More commonly, the histogram would be used for dc testing, where the user tests the ADC for the code distribution for dc input and computes the mean and standard deviation, or transition noise of the converter, which are displayed as **Mean** and **Transition Noise**, respectively, in the **Histogram Analysis** area (labeled 1 in Figure 19).

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

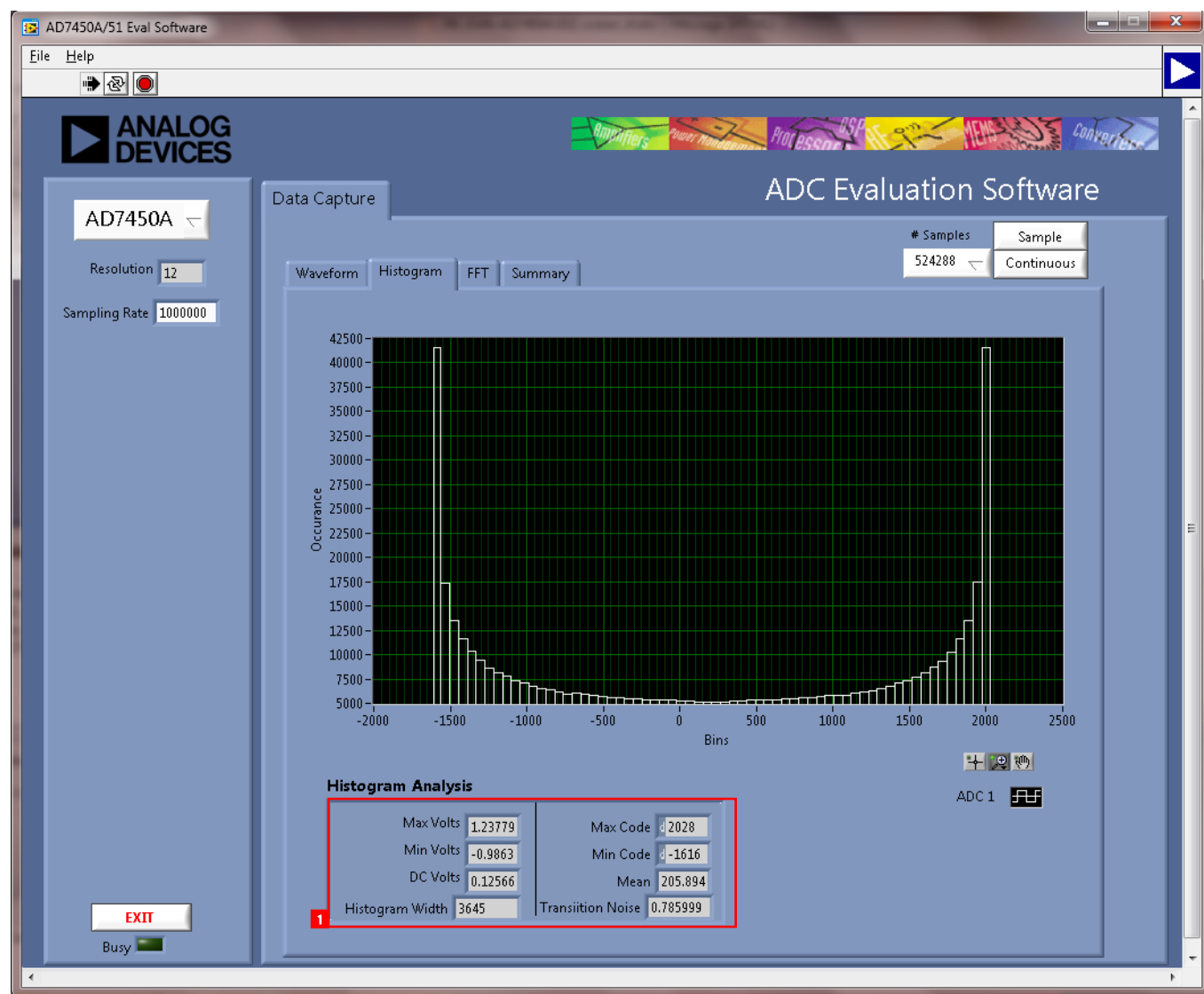


Figure 19. Histogram Capture Tab

GENERATING A FAST FOURIER TRANSFORM OF AC CHARACTERISTICS

Figure 20 shows the FFT tab. This feature tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results.

To perform an ac FFT test,

1. Apply a sinusoidal signal with low distortion (better than 100 dB) to the evaluation board at the SMB Inputs J1/J2. To attain the requisite low distortion, which is necessary to allow true evaluation of the part, one option is to
 - a. Filter the input signal from the ac source. Choose an appropriate band-pass filter based on the sinusoidal signal applied.
 - b. If a low frequency band-pass filter is used when the full-scale input range is more than a few volts peak-to-peak, use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

2. Click the **FFT** tab from the main window.
3. Click **Sample**.

As in the histogram test, raw data is captured and passed to the PC where the FFT is performed displaying SNR, SINAD, THD, and SFDR.

The **Spectrum Analysis** box displays the results of the captured data.

- The area labeled 1 in Figure 20 shows the input signal information.
- The area labeled 2 in Figure 20 displays the fundamental frequency and amplitude in addition to the second to fifth harmonics.
- The area labeled 3 in Figure 20 displays the performance data, including the SNR, THD, and SINAD.

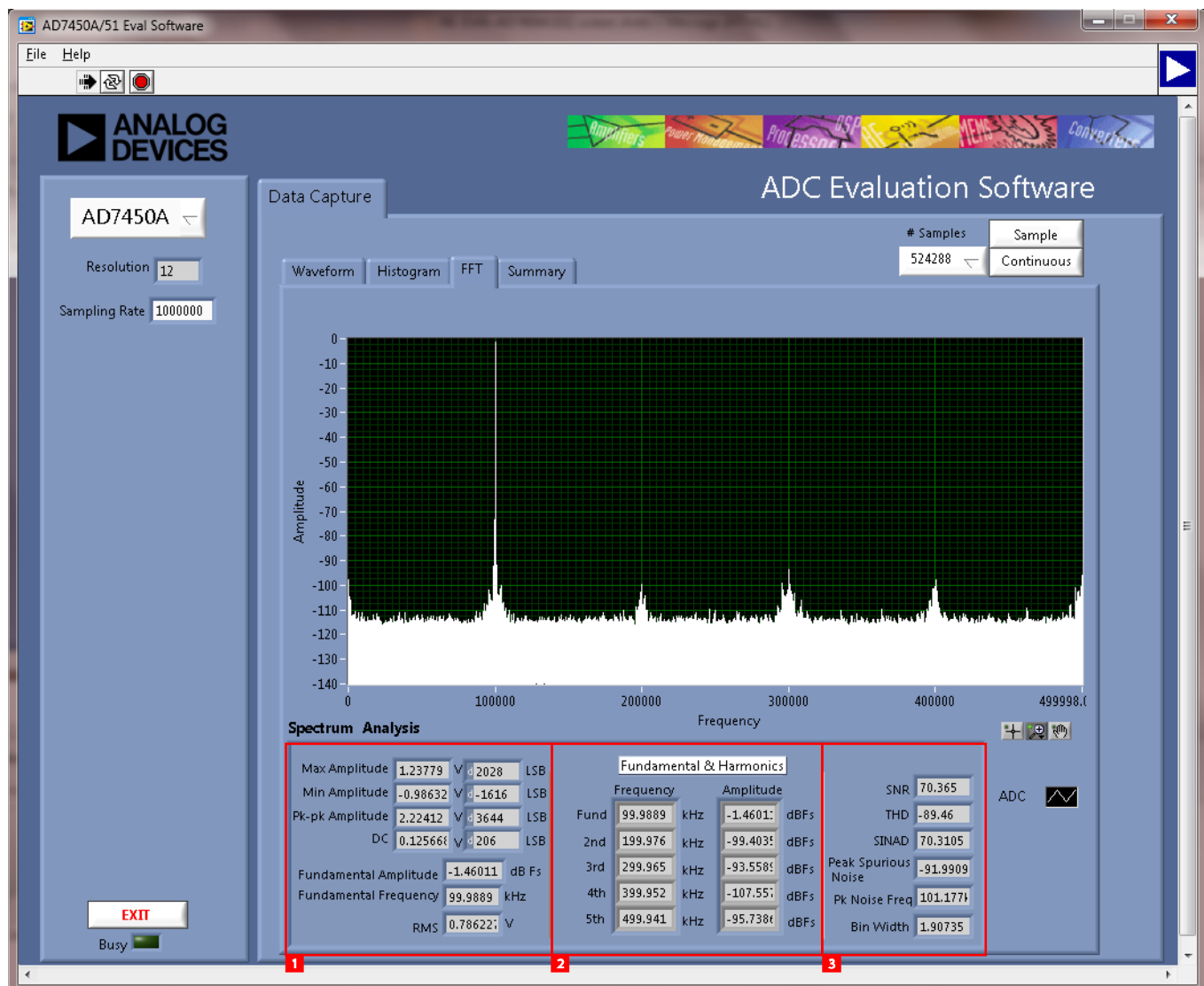


Figure 20. FFT Tab
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GENERATING A SUMMARY OF THE WAVEFORM, HISTOGRAM, AND FAST FOURIER TRANSFORM

Figure 21 shows the **Summary** tab. The **Summary** tab captures all the display information and provides it in one panel with a synopsis of the information, including key performance parameters such as SNR and THD.

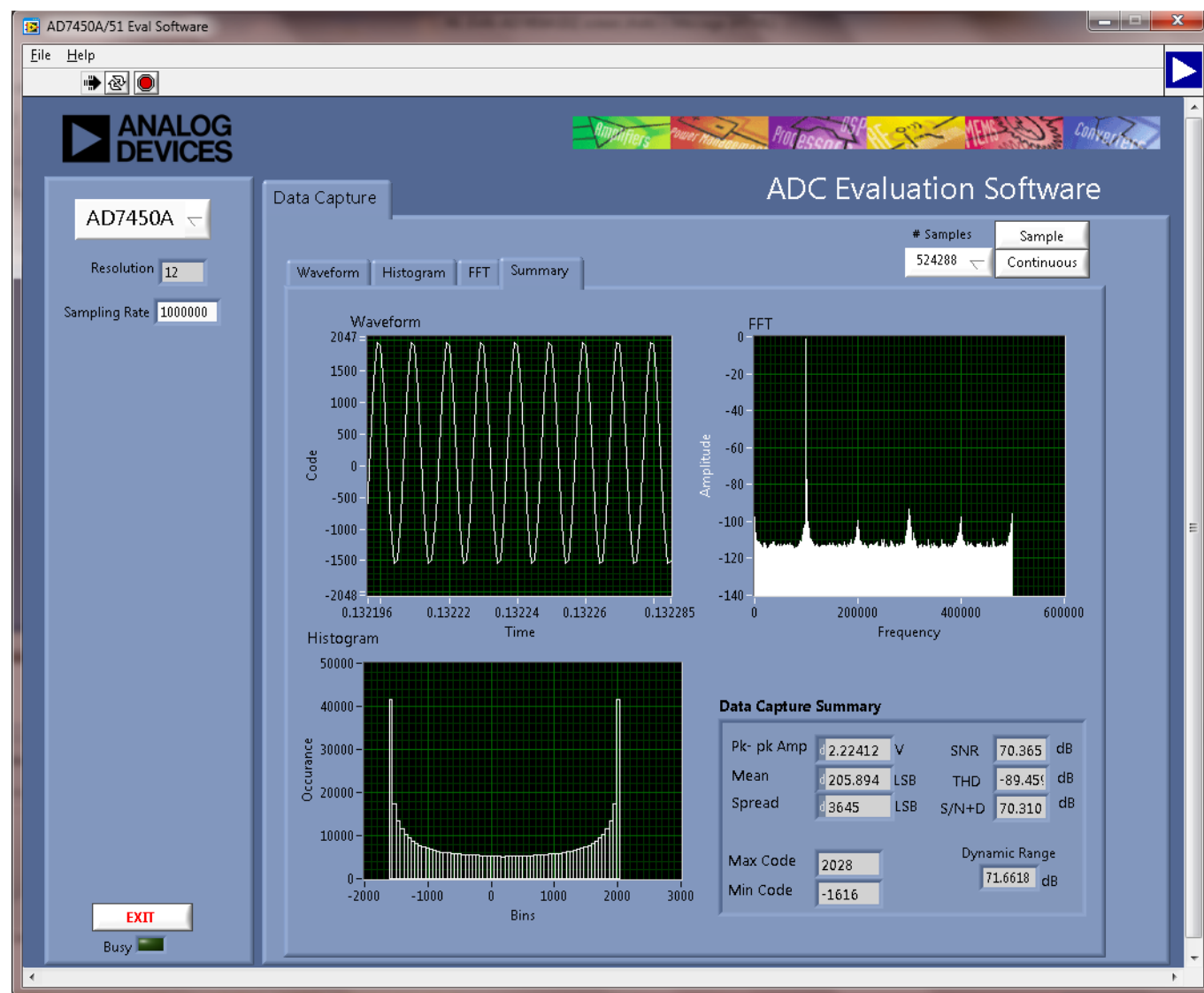


Figure 21. Summary Tab

06231-022



Figure 23. Schematic Page 2



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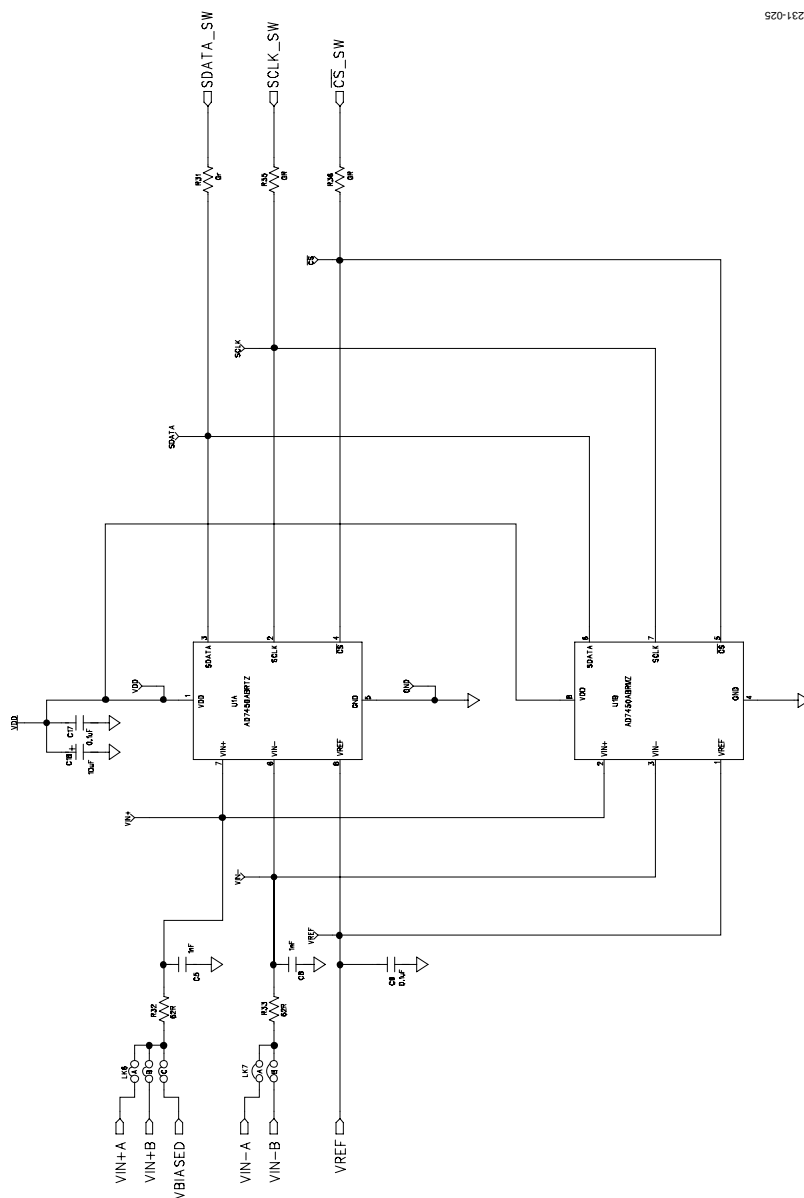


Figure 25. Schematic Page 4

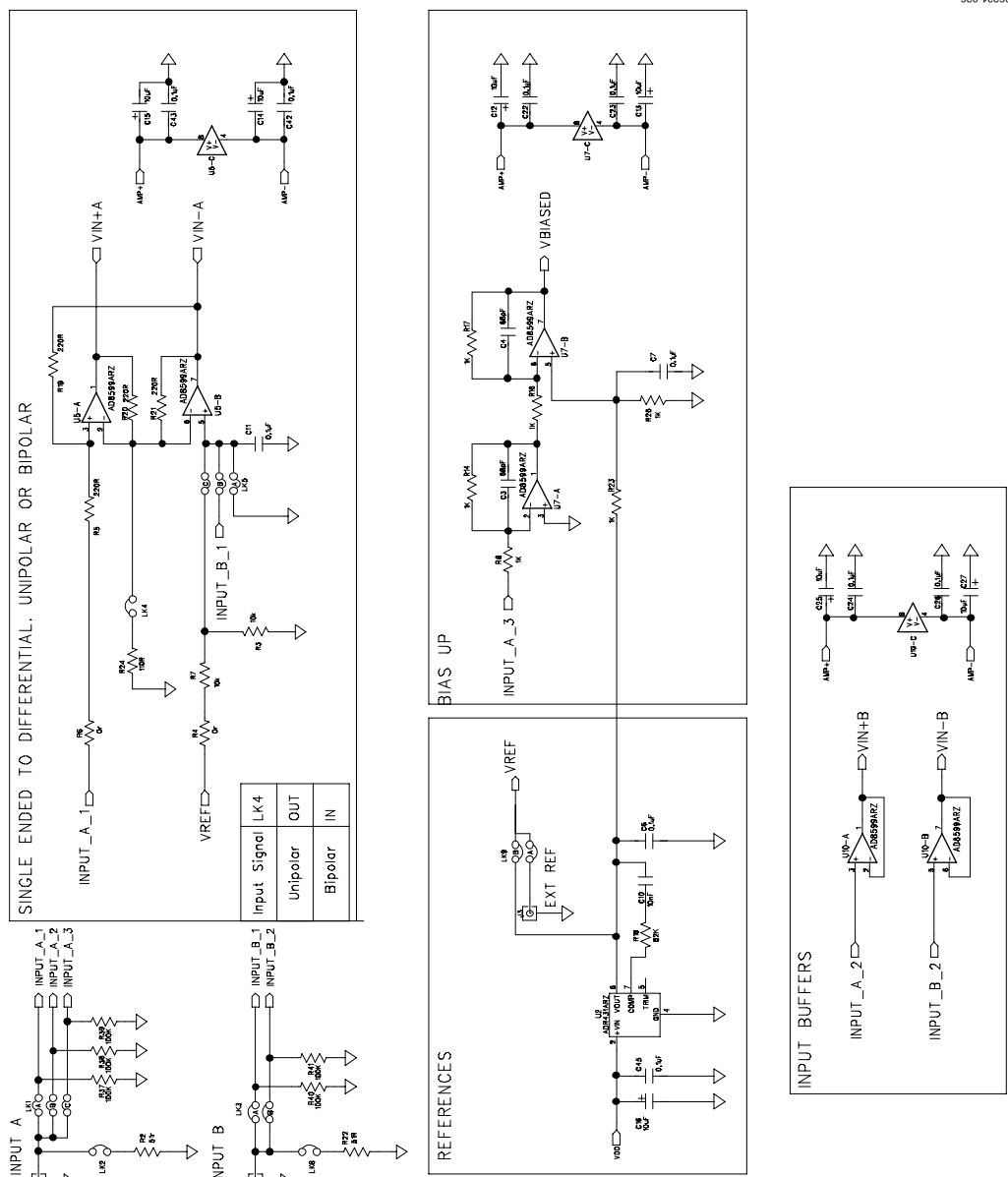


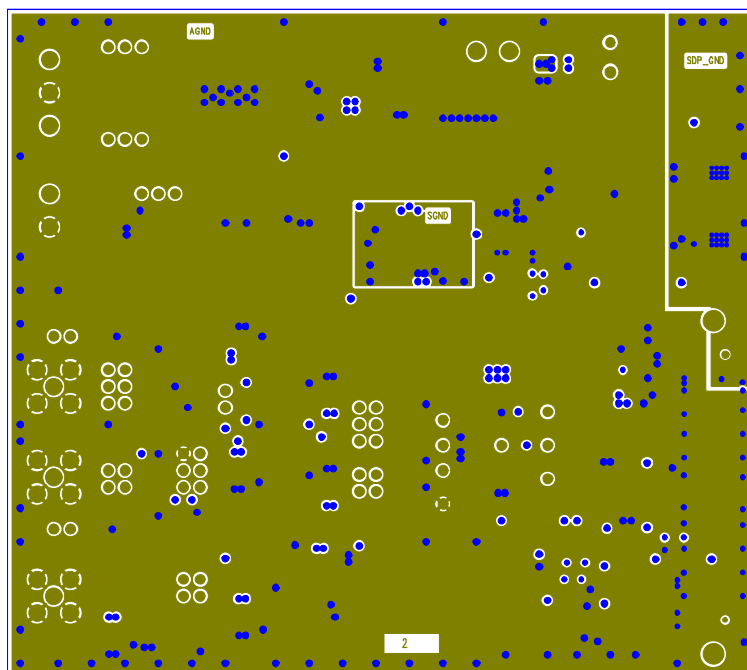
Figure 26. Schematic Page 5



Figure 27. Top Printed Circuit Board (PCB) Silkscreen

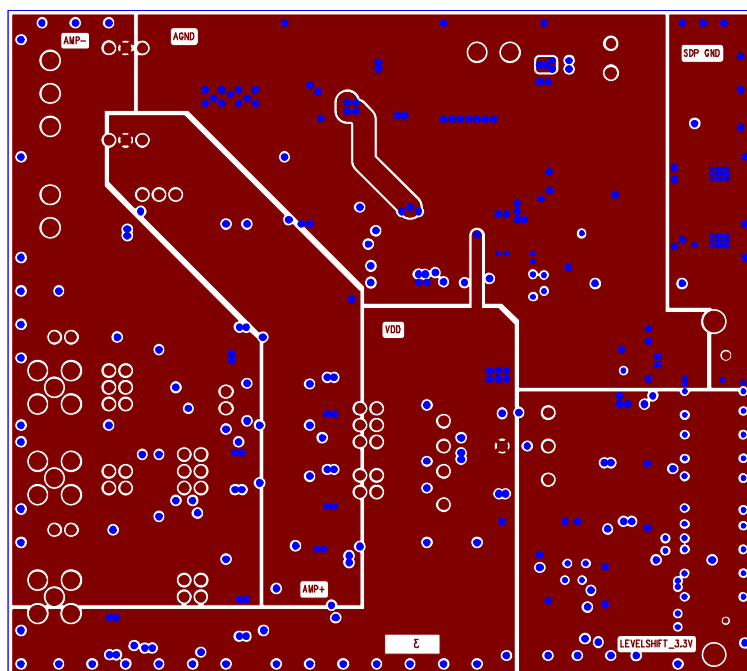


Figure 28. Layer 1 Component Side View



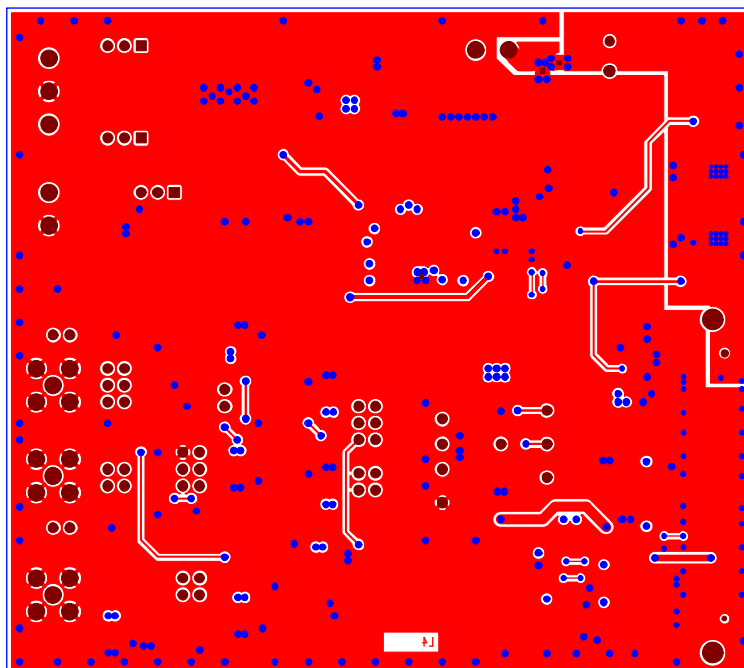
06231-029

Figure 29. Layer 2 Component Side View



06231-030

Figure 30. Layer 3 Component Side View



06231-031

Figure 31. Layer 4 Component Side View

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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