

M16C/1N Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0002-0100Z

Rev.1.00

2004.10.20

1. Overview

The M16C/1N group consists of single-chip microcomputers that use high-performance silicon gate CMOS processes and have a on-chip M16C/60 series CPU core. The microcomputers are housed in 48-pin plastic mold QFP package. These single-chip microcomputers have both high function instructions and high instruction efficiency and feature a one-megabyte address space and the capability to execute instructions at high speed.

1.1 Applications

Automotive and industrial control systems, other automobile, other

1.2 Performance Overview

Table 1.1 gives an overview of the M16C/1N group performance specification.

Table 1.1 Performance overview

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		62.5 ns (when $f(X_{IN})=16\text{MHz}$)
Memory size	ROM	See Table 1.2 Performance overview
	RAM	See Table 1.2 Performance overview
I/O port		P0 to P5: 37 lines
Multifunction timer	T1	8 bits x 1
	TX, TY, TZ	8 bits x 3
	TC	16 bits x 1
Serial I/O (UART or clock synchronous)		x 2
A/D converter (maximum resolution: 10 bits)		x 12 channels (Expandable up to 14 channels)
D/A converter		8 bits x 1
CAN controller		1 channel, 2.0B active
Watchdog timer		15 bits x 1 (with prescaler)
Interrupts		15 internal causes, 8 external causes, 4 software causes
Clock generating circuits		3 internal circuits
Power supply voltage		4.2 V to 5.5V (when $f(X_{IN})=16\text{MHz}$)
Power consumption		70mW($V_{CC}=5.0\text{V}$, $f(X_{IN})=16\text{MHz}$)
I/O characteristics	I/O withstand voltage	5V
	Output current	5mA (10mA:LED drive port)
Device configuration		CMOS silicon gate
Package		48-pin LQFP

1.3 Block Diagram

Figure 1.1 shows block diagram of the M16C/1N group.

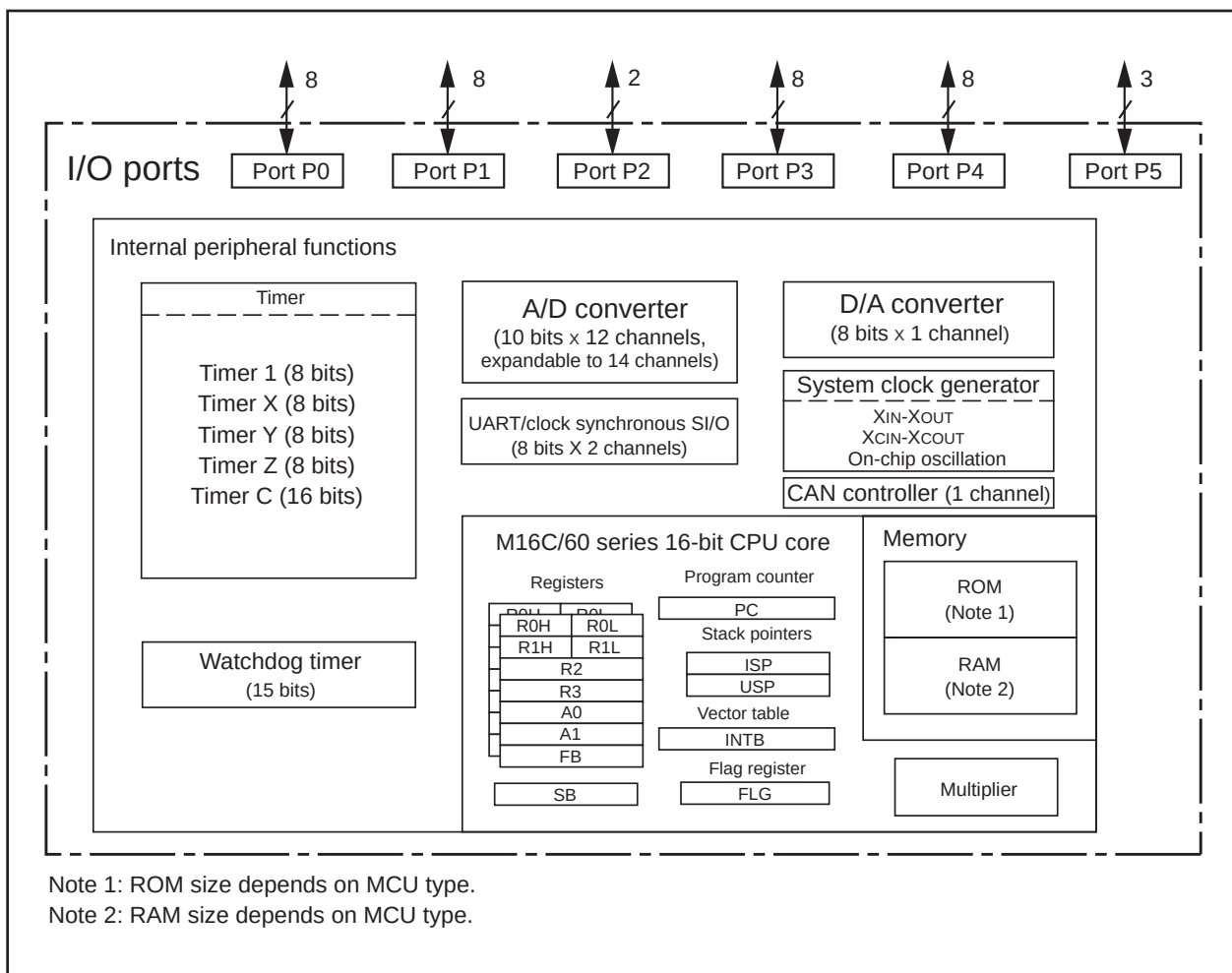


Figure 1.1 Block diagram

1.4 Performance Overview

Table 1.2 shows performance overview.

Table 1.2 Performance overview

As of June 2004

Type No.	ROM	RAM	Package	Remarks
M301N2M4T-XXXFP(D)	32Kbytes	1Kbytes	48P6Q-A	Mask ROM
M301N2M8T-XXXFP(D)	64Kbytes	3Kbytes		Flash memory
M301N2F8TFP(D)				
M301N2F8FP(D)				

(D): Under development

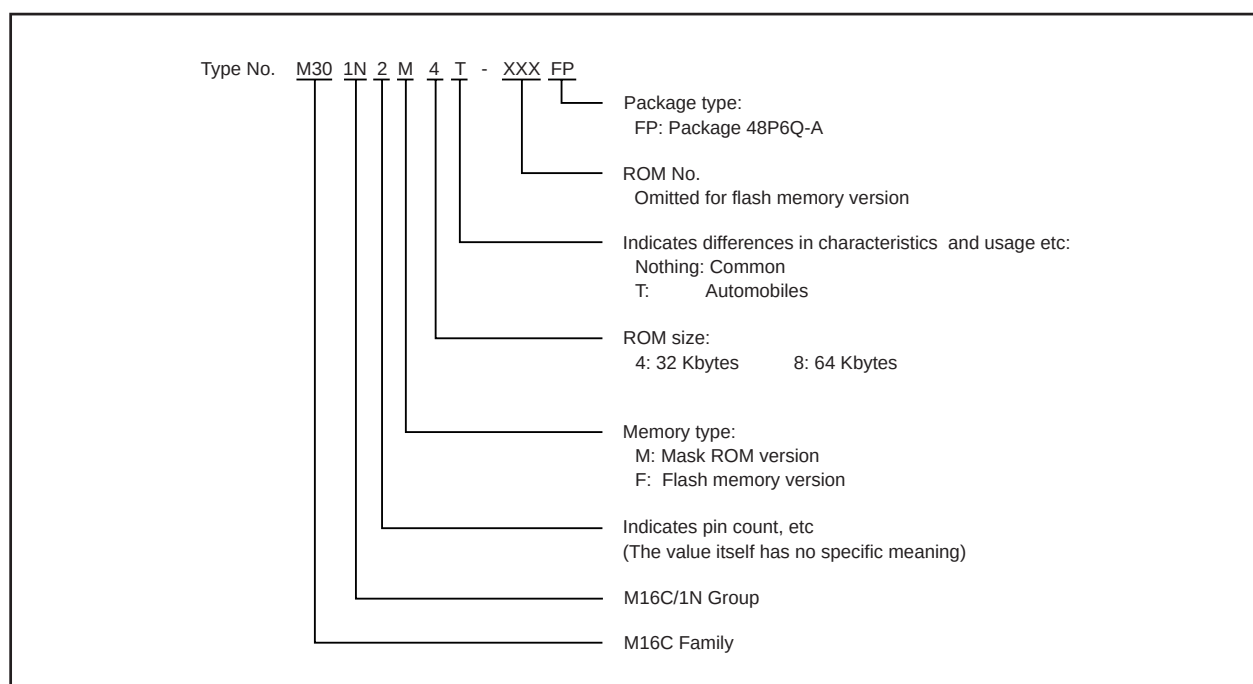


Figure 1.2 Type No., memory size, and package

1.5 Pin Configuration

Figure 1.3 shows pin configurations (top view) of the M16C/1N group.

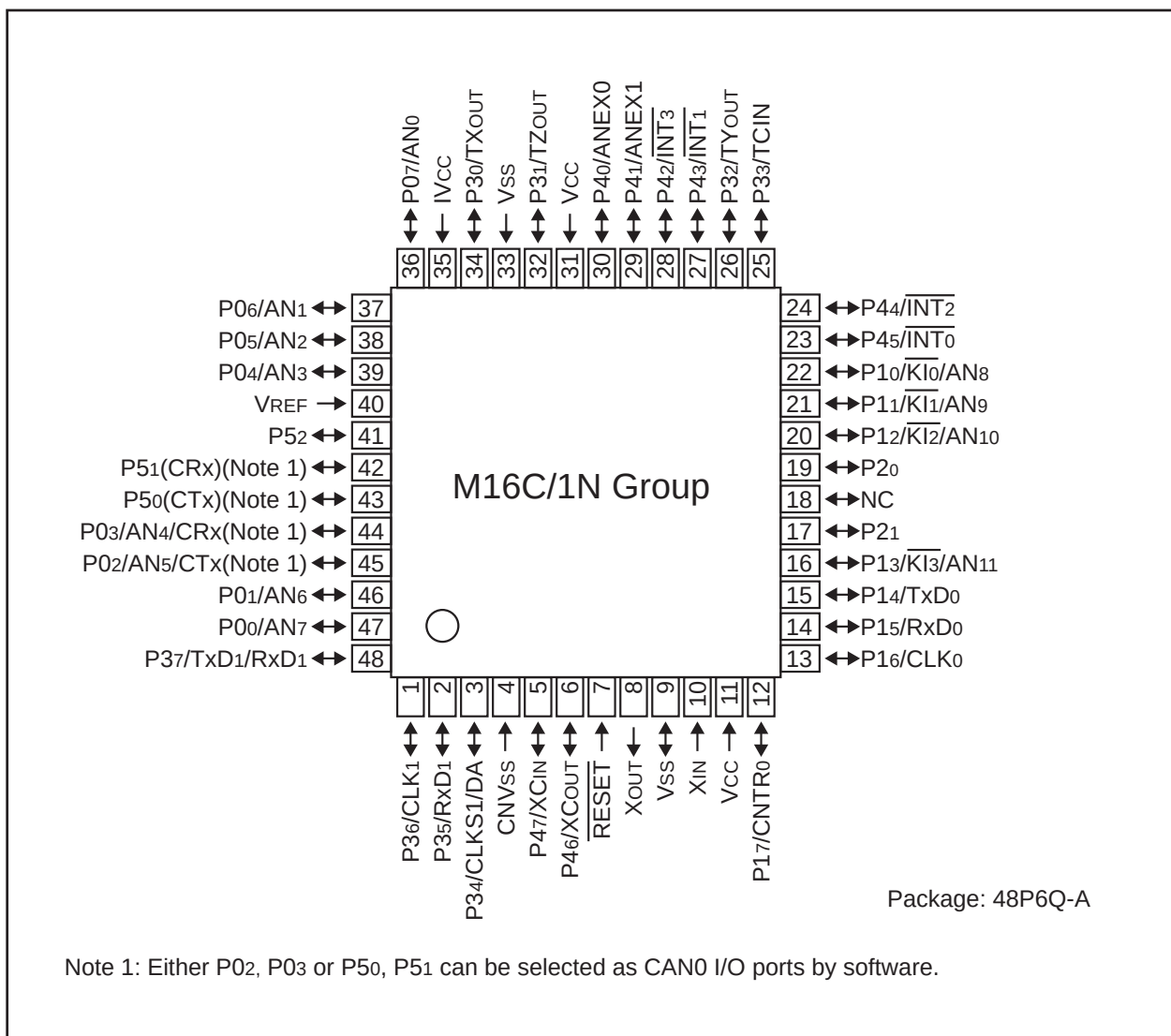


Figure 1.3 Pin configuration diagram (top view)

1.6 Pin Description

Table 1.3 shows the pin description.

Table 1.3 Pin Description

Pin name	Signal name	I/O type	Function
VCC, VSS	Power supply input	Input	Supply 4.2 to 5.5 V to the VCC pin. Supply 0 V to the VSS pin.
IVCC	IVCC	Input	Connect a capacitor (0.1 μ F) between this pin and VSS.
CNVSS	CNVSS	Input	Connect it to the VSS pin via resistance (about 5 k Ω).
$\overline{\text{RESET}}$	Reset input	Input	A "L" on this input resets the microcomputer.
XIN	Clock input	Input	These pins are provided for the main clock oscillation circuit. Connect a ceramic resonator or crystal between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XOUT	Clock output	Output	
VREF	Reference voltage input	Input	This pin is a reference voltage input for the A/D converter.
P0 ₀ to P0 ₇	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor. These pins are shared with analog input pins. P0 ₂ and P0 ₃ function as CAN0 I/O pins by using software.
P1 ₀ to P1 ₇	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. P1 ₀ to P1 ₃ are shared with analog inputs and key input interrupts. P1 ₄ to P1 ₆ are shared with serial I/O pins. P1 ₇ is shared with timer input. Can be used as an LED drive port.
P2 ₀ to P2 ₁	I/O port P2	Input/output	This is a 2-bit I/O port equivalent to P0.
P3 ₀ to P3 ₇	I/O port P3	Input/output	This is a 8-bit I/O port equivalent to P0. P3 ₀ to P3 ₃ are shared with timer input/output. P3 ₄ to P3 ₇ are shared with serial I/O. P3 ₄ is shared with analog outputs.
P4 ₀ to P4 ₇	I/O port P4	Input/output	This is a 8-bit I/O port equivalent to P0. P4 ₀ to P4 ₁ are shared with analog inputs. P4 ₂ to P4 ₅ are shared with interrupt inputs. P4 ₆ to P4 ₇ are shared with the I/O pin of the clock oscillation circuit for the clock.
P5 ₀ to P5 ₂	I/O port P5	Input/output	This is a 3-bit I/O port equivalent to P0. P5 ₀ and P5 ₁ function as CAN0 I/O pins by using software.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

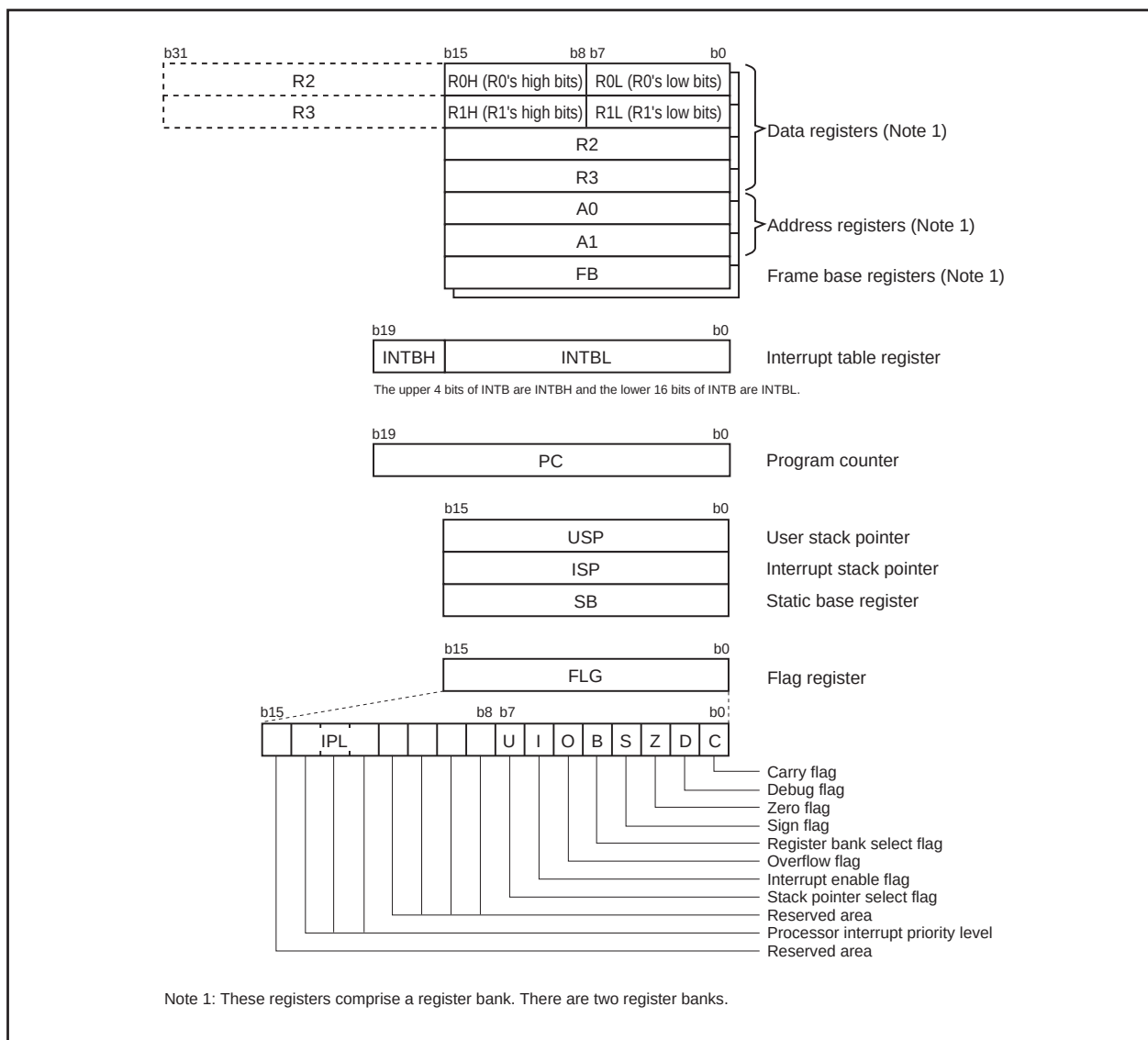


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is set to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is set to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map. The address space extends the 1M bytes from address 00000₁₆ to FFFFF₁₆. From FFFFF₁₆ down is ROM. For example, in the M301N2M4T-XXXFP, there is 32K bytes of internal ROM from F8000₁₆ to FFFFF₁₆. The vector table for fixed interrupts such as the reset are mapped to FFFDC₁₆ to FFFFF₁₆. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From 00400₁₆ up is RAM. For example, in the M301N2M4T-XXXFP, there is 1K byte of internal RAM from 00400₁₆ to 007FF₁₆. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 00000₁₆ to 003FF₁₆. This area accommodates the control registers for peripheral devices such as I/O ports, A/D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to FFE00₁₆ to FFFDB₁₆. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

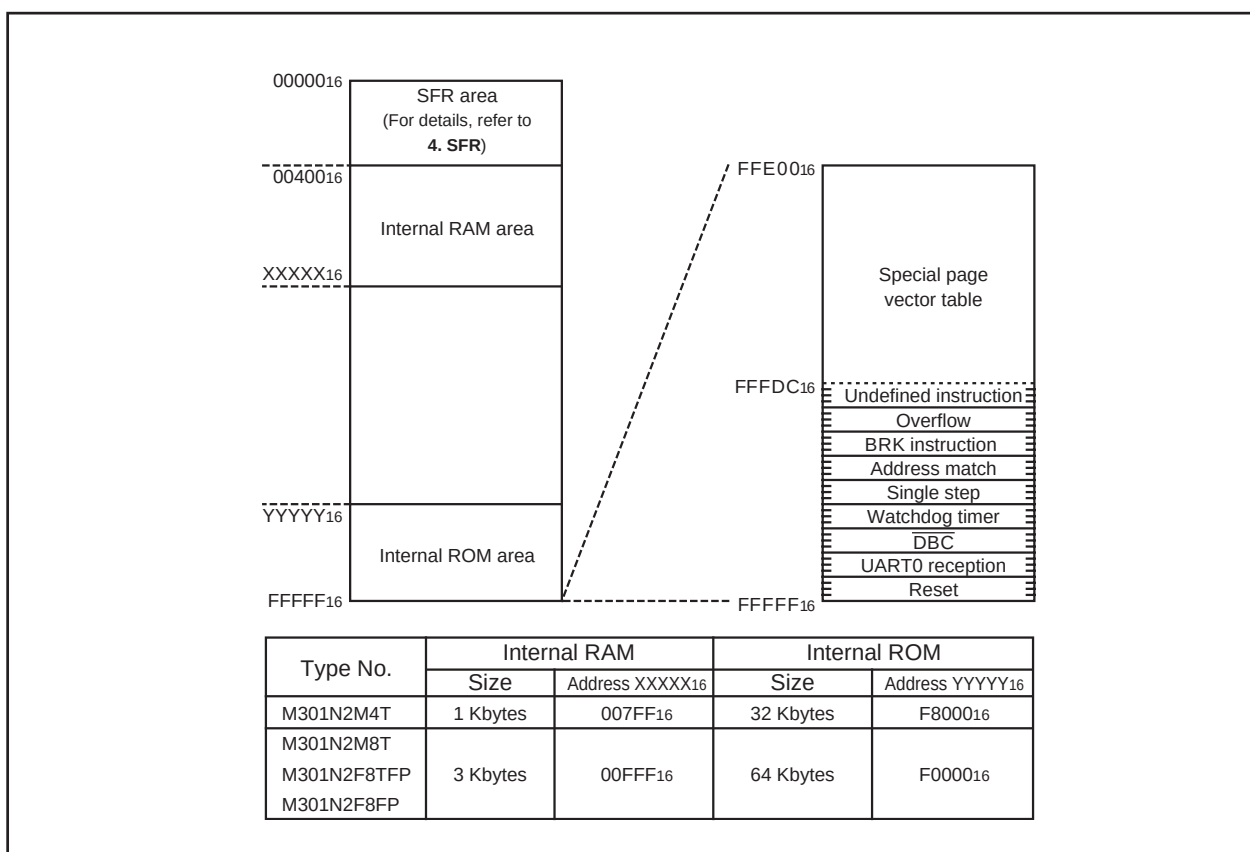


Figure 3.1 Memory map

4. Special Function Registers (SFR)

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	XXXX0X00 ₂
0005 ₁₆	Processor mode register 1	PM1	00XXXX0X0 ₂
0006 ₁₆	System clock control register 0	CM0	48 ₁₆
0007 ₁₆	System clock control register 1	CM1	20 ₁₆
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XXXXX000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register	CM2	04 ₁₆
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	000XXXXX ₂
0010 ₁₆	Address match interrupt register 0	RMAD0	00000000 ₂
0011 ₁₆			00000000 ₂
0012 ₁₆			XXXX0000 ₂
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00000000 ₂
0015 ₁₆			00000000 ₂
0016 ₁₆			XXXX0000 ₂
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	INT0 input filter select register	INT0F	XXXXX000 ₂
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆	CAN0 wakeup interrupt control register	C01WKIC	XXXXX000 ₂
0046 ₁₆	CAN0 state/error interrupt control register	C01ERRIC	XXXXX000 ₂
0047 ₁₆			
0048 ₁₆	CAN0 reception successful interrupt control register	C0RECIC	XXXXX000 ₂
0049 ₁₆	CAN0 transmission successful interrupt control register	C0TRMIC	XXXXX000 ₂
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX000 ₂
004E ₁₆	A/D conversion interrupt control register	ADIC	XXXXX000 ₂
004F ₁₆			
0050 ₁₆			
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000 ₂
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000 ₂
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000 ₂
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000 ₂
0055 ₁₆	Timer 1 interrupt control register	T1IC	XXXXX000 ₂
0056 ₁₆	Timer X interrupt control register	TXIC	XXXXX000 ₂
0057 ₁₆	Timer Y interrupt control register	TYIC	XXXXX000 ₂
0058 ₁₆	Timer Z interrupt control register	TZIC	XXXXX000 ₂
0059 ₁₆	CNTR0 interrupt control register	CNTR0IC	XXXXX000 ₂
005A ₁₆	TCIN interrupt control register	TCINIC	XXXXX000 ₂
005B ₁₆	Timer C interrupt control register	TCIC	XXXXX000 ₂
005C ₁₆	INT3 interrupt control register	INT3IC	XXXXX000 ₂
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X000 ₂
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X000 ₂
005F ₁₆	INT2 interrupt control register	INT2IC	XX00X000 ₂
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

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X : Undefined

Address	Register	Symbol	After reset
0080 ₁₆	Timer Y, Z mode register	TYZMR	000000X0 ₂
0081 ₁₆	Prescaler Y	PREY	FF ₁₆
0082 ₁₆	Timer Y secondary	TYSC	FF ₁₆
0083 ₁₆	Timer Y primary	TYPR	FF ₁₆
0084 ₁₆	Timer Y, Z waveform output control register	PUM	00 ₁₆
0085 ₁₆	Prescaler Z	PREZ	FF ₁₆
0086 ₁₆	Timer Z secondary	TZSC	FF ₁₆
0087 ₁₆	Timer Z primary	TZPR	FF ₁₆
0088 ₁₆	Prescaler 1	PRE1	XX ₁₆
0089 ₁₆	Timer 1	T1	XX ₁₆
008A ₁₆	Timer Y, Z output control register	TYZOC	XXXXXX000 ₂
008B ₁₆	Timer X mode register	TXMR	00000000 ₂
008C ₁₆	Prescaler X	PREX	FF ₁₆
008D ₁₆	Timer X	TX	FF ₁₆
008E ₁₆	Timer count source set register	TCSS	00 ₁₆
008F ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX ₂
0090 ₁₆	Timer C counter	TC	XX ₁₆
0091 ₁₆			XX ₁₆
0092 ₁₆			
0093 ₁₆			
0094 ₁₆			
0095 ₁₆			
0096 ₁₆	External input enable register	INTEN	00 ₁₆
0097 ₁₆			
0098 ₁₆	Key input enable register	KIEN	00 ₁₆
0099 ₁₆			
009A ₁₆	Timer C control register 0	TCC0	0XX00000 ₂
009B ₁₆	Timer C control register 1	TCC1	XXXXXX11 ₂
009C ₁₆	Time measurement register	TM	XX ₁₆
009D ₁₆			XX ₁₆
009E ₁₆			
009F ₁₆			
00A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
00A1 ₁₆	UART0 bit rate generator	U0BRG	XX ₁₆
00A2 ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆
00A3 ₁₆			XX ₁₆
00A4 ₁₆	UART0 transmit/receive control register 0	U0C0	08 ₁₆
00A5 ₁₆	UART0 transmit/receive control register 1	U0C1	XXXX0010 ₂
00A6 ₁₆	UART0 receive buffer register	U0RB	XX ₁₆
00A7 ₁₆			XX ₁₆
00A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
00A9 ₁₆	UART1 bit rate generator	U1BRG	XX ₁₆
00AA ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆
00AB ₁₆			XX ₁₆
00AC ₁₆	UART1 transmit/receive control register 0	U1C0	08 ₁₆
00AD ₁₆	UART1 transmit/receive control register 1	U1C1	XXXX0010 ₂
00AE ₁₆	UART1 receive buffer register	U1RB	XX ₁₆
00AF ₁₆			XX ₁₆
00B0 ₁₆	UART transmit/receive control register 2	UCON	X0000000 ₂
00B1 ₁₆			
00B2 ₁₆			
00B3 ₁₆			
00B4 ₁₆			
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

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X : Undefined

Address	Register	Symbol	After reset
00C0 ₁₆	A/D register	AD	XX ₁₆
00C1 ₁₆			XX ₁₆
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆	A/D control register 2	ADCON2	XXXX0000 ₂
00D5 ₁₆			
00D6 ₁₆	A/D control register 0	ADCON0	00000XXX ₂
00D7 ₁₆	A/D control register 1	ADCON1	00 ₁₆
00D8 ₁₆	D/A register	DA	XX ₁₆
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆	D/A control register	DACON	XXXXXX0X0 ₂
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆	Port P0 register	P0	XX ₁₆
00E1 ₁₆	Port P1 register	P1	XX ₁₆
00E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
00E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
00E4 ₁₆	Port P2 register	P2	XX ₁₆
00E5 ₁₆	Port P3 register	P3	XX ₁₆
00E6 ₁₆	Port P2 direction register	PD2	XXXXXXXX00 ₂
00E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
00E8 ₁₆	Port P4 register	P4	XX ₁₆
00E9 ₁₆	Port P5 register	P5	XX ₁₆
00EA ₁₆	Port P4 direction register	PD4	00 ₁₆
00EB ₁₆	Port P5 direction register	PD5	XXXXXX000 ₂
00EC ₁₆			
00ED ₁₆			
00EE ₁₆			
00EF ₁₆			
00F0 ₁₆			
00F1 ₁₆			
00F2 ₁₆			
00F3 ₁₆			
00F4 ₁₆			
00F5 ₁₆			
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆	CAN0 I/O port select register	CIOSR	XXXXXXXX0 ₂
00F9 ₁₆			
00FA ₁₆			
00FB ₁₆			
00FC ₁₆	Pull-up control register 0	PUR0	00X00000 ₂
00FD ₁₆	Pull-up control register 1	PUR1	XXXXXXXX000 ₂
00FE ₁₆	Port P1 drive capacity control register	DRR	00 ₁₆
00FF ₁₆			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

Address	Register	Symbol	After reset
0100 ₁₆			
0101 ₁₆			
0102 ₁₆			
0103 ₁₆			
0104 ₁₆			
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 (Note 2)	FMR4	01000000 ₂
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 (Note 2)	FMR1	0000XX0X ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	XX000001 ₂
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
0215 ₁₆			
0216 ₁₆			
0217 ₁₆			
0218 ₁₆			
0219 ₁₆			
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 message control register 0	C0MCTL0	00 ₁₆
0221 ₁₆	CAN0 message control register 1	C0MCTL1	00 ₁₆
0222 ₁₆	CAN0 message control register 2	C0MCTL2	00 ₁₆
0223 ₁₆	CAN0 message control register 3	C0MCTL3	00 ₁₆
0224 ₁₆	CAN0 message control register 4	C0MCTL4	00 ₁₆
0225 ₁₆	CAN0 message control register 5	C0MCTL5	00 ₁₆
0226 ₁₆	CAN0 message control register 6	C0MCTL6	00 ₁₆
0227 ₁₆	CAN0 message control register 7	C0MCTL7	00 ₁₆
0228 ₁₆	CAN0 message control register 8	C0MCTL8	00 ₁₆
0229 ₁₆	CAN0 message control register 9	C0MCTL9	00 ₁₆
022A ₁₆	CAN0 message control register 10	C0MCTL10	00 ₁₆
022B ₁₆	CAN0 message control register 11	C0MCTL11	00 ₁₆
022C ₁₆	CAN0 message control register 12	C0MCTL12	00 ₁₆
022D ₁₆	CAN0 message control register 13	C0MCTL13	00 ₁₆
022E ₁₆	CAN0 message control register 14	C0MCTL14	00 ₁₆
022F ₁₆	CAN0 message control register 15	C0MCTL15	00 ₁₆
0230 ₁₆	CAN0 control register	C0CTLR	X0000001 ₂
0231 ₁₆			XX0X0000 ₂
0232 ₁₆	CAN0 status register	C0STR	00 ₁₆
0233 ₁₆			X0000001 ₂
0234 ₁₆	CAN0 slot status register	C0SSTR	0000 ₁₆
0235 ₁₆			0000 ₁₆
0236 ₁₆	CAN0 interrupt control register	C0ICR	0000 ₁₆
0237 ₁₆			0000 ₁₆
0238 ₁₆	CAN0 extended ID register	C0IDR	0000 ₁₆
0239 ₁₆			0000 ₁₆
023A ₁₆	CAN0 configuration register	C0CONR	XX ₁₆
023B ₁₆			XX ₁₆
023C ₁₆	CAN0 receive error count register	C0RECR	00 ₁₆
023D ₁₆	CAN0 transmit error count register	C0TECR	00 ₁₆
023E ₁₆			
023F ₁₆			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Note 2: These registers are available on flash memory versions only.

X : Undefined

Address	Register	Symbol	After reset
0240 ₁₆			
0241 ₁₆			
0242 ₁₆			
0243 ₁₆			
0244 ₁₆	CAN0 acceptance filter support register	C0AFS	XX ₁₆
0245 ₁₆			XX ₁₆
0246 ₁₆			
0247 ₁₆			
0248 ₁₆			
0249 ₁₆			
024A ₁₆			
024B ₁₆			
024C ₁₆			
024D ₁₆			
024E ₁₆			
024F ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆			
025E ₁₆			
025F ₁₆	CAN0 clock select register	CCLKR	X000XXXX ₂
0260 ₁₆	CAN0 slot 0: Identifier / DLC		XX ₁₆
0261 ₁₆			XX ₁₆
0262 ₁₆			XX ₁₆
0263 ₁₆			XX ₁₆
0264 ₁₆			XX ₁₆
0265 ₁₆	CAN0 slot 0: Data Field		XX ₁₆
0266 ₁₆			XX ₁₆
0267 ₁₆			XX ₁₆
0268 ₁₆			XX ₁₆
0269 ₁₆			XX ₁₆
026A ₁₆			XX ₁₆
026B ₁₆			XX ₁₆
026C ₁₆			XX ₁₆
026D ₁₆	CAN0 slot 0: Time Stamp		XX ₁₆
026E ₁₆			XX ₁₆
0270 ₁₆	CAN0 slot 1: Identifier / DLC		XX ₁₆
0271 ₁₆			XX ₁₆
0272 ₁₆			XX ₁₆
0273 ₁₆			XX ₁₆
0274 ₁₆			XX ₁₆
0275 ₁₆	CAN0 slot 1: Data Field		XX ₁₆
0276 ₁₆			XX ₁₆
0277 ₁₆			XX ₁₆
0278 ₁₆			XX ₁₆
0279 ₁₆			XX ₁₆
027A ₁₆			XX ₁₆
027B ₁₆			XX ₁₆
027C ₁₆			XX ₁₆
027D ₁₆	CAN0 slot 1: Time Stamp		XX ₁₆
027E ₁₆			XX ₁₆
027F ₁₆			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

Address	Register	Symbol	After reset
0280 ₁₆	CAN0 slot 2: Identifier / DLC		XX ₁₆
0281 ₁₆			XX ₁₆
0282 ₁₆			XX ₁₆
0283 ₁₆			XX ₁₆
0284 ₁₆			XX ₁₆
0285 ₁₆			XX ₁₆
0286 ₁₆	CAN0 slot 2: Data Field		XX ₁₆
0287 ₁₆			XX ₁₆
0288 ₁₆			XX ₁₆
0289 ₁₆			XX ₁₆
028A ₁₆			XX ₁₆
028B ₁₆			XX ₁₆
028C ₁₆			XX ₁₆
028D ₁₆			XX ₁₆
028E ₁₆	CAN0 slot 2: Time Stamp		XX ₁₆
028F ₁₆			XX ₁₆
0290 ₁₆	CAN0 slot 3: Identifier / DLC		XX ₁₆
0291 ₁₆			XX ₁₆
0292 ₁₆			XX ₁₆
0293 ₁₆			XX ₁₆
0294 ₁₆			XX ₁₆
0295 ₁₆			XX ₁₆
0296 ₁₆	CAN0 slot 3: Data Field		XX ₁₆
0297 ₁₆			XX ₁₆
0298 ₁₆			XX ₁₆
0299 ₁₆			XX ₁₆
029A ₁₆			XX ₁₆
029B ₁₆			XX ₁₆
029C ₁₆			XX ₁₆
029D ₁₆			XX ₁₆
029E ₁₆	CAN0 slot 3: Time Stamp		XX ₁₆
029F ₁₆			XX ₁₆
02A0 ₁₆	CAN0 slot 4: Identifier / DLC		XX ₁₆
02A1 ₁₆			XX ₁₆
02A2 ₁₆			XX ₁₆
02A3 ₁₆			XX ₁₆
02A4 ₁₆			XX ₁₆
02A5 ₁₆			XX ₁₆
02A6 ₁₆	CAN0 slot 4: Data Field		XX ₁₆
02A7 ₁₆			XX ₁₆
02A8 ₁₆			XX ₁₆
02A9 ₁₆			XX ₁₆
02AA ₁₆			XX ₁₆
02AB ₁₆			XX ₁₆
02AC ₁₆			XX ₁₆
02AD ₁₆			XX ₁₆
02AE ₁₆	CAN0 slot 4: Time Stamp		XX ₁₆
02AF ₁₆			XX ₁₆
02B0 ₁₆	CAN0 slot 5: Identifier / DLC		XX ₁₆
02B1 ₁₆			XX ₁₆
02B2 ₁₆			XX ₁₆
02B3 ₁₆			XX ₁₆
02B4 ₁₆			XX ₁₆
02B5 ₁₆			XX ₁₆
02B6 ₁₆	CAN0 slot 5: Data Field		XX ₁₆
02B7 ₁₆			XX ₁₆
02B8 ₁₆			XX ₁₆
02B9 ₁₆			XX ₁₆
02BA ₁₆			XX ₁₆
02BB ₁₆			XX ₁₆
02BC ₁₆			XX ₁₆
02BD ₁₆			XX ₁₆
02BE ₁₆	CAN0 slot 5: Time Stamp		XX ₁₆
02BF ₁₆			XX ₁₆

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

Address	Register	Symbol	After reset
02C0 ₁₆	CAN0 slot 6: Identifier / DLC		XX ₁₆
02C1 ₁₆			XX ₁₆
02C2 ₁₆			XX ₁₆
02C3 ₁₆			XX ₁₆
02C4 ₁₆			XX ₁₆
02C5 ₁₆			XX ₁₆
02C6 ₁₆	CAN0 slot 6: Data Field		XX ₁₆
02C7 ₁₆			XX ₁₆
02C8 ₁₆			XX ₁₆
02C9 ₁₆			XX ₁₆
02CA ₁₆			XX ₁₆
02CB ₁₆			XX ₁₆
02CC ₁₆			XX ₁₆
02CD ₁₆			XX ₁₆
02CE ₁₆	CAN0 slot 6: Time Stamp		XX ₁₆
02CF ₁₆			XX ₁₆
02D0 ₁₆	CAN0 slot 7: Identifier / DLC		XX ₁₆
02D1 ₁₆			XX ₁₆
02D2 ₁₆			XX ₁₆
02D3 ₁₆			XX ₁₆
02D4 ₁₆			XX ₁₆
02D5 ₁₆			XX ₁₆
02D6 ₁₆	CAN0 slot 7: Data Field		XX ₁₆
02D7 ₁₆			XX ₁₆
02D8 ₁₆			XX ₁₆
02D9 ₁₆			XX ₁₆
02DA ₁₆			XX ₁₆
02DB ₁₆			XX ₁₆
02DC ₁₆			XX ₁₆
02DD ₁₆			XX ₁₆
02DE ₁₆	CAN0 slot 7: Time Stamp		XX ₁₆
02DF ₁₆			XX ₁₆
02E0 ₁₆	CAN0 slot 8: Identifier / DLC		XX ₁₆
02E1 ₁₆			XX ₁₆
02E2 ₁₆			XX ₁₆
02E3 ₁₆			XX ₁₆
02E4 ₁₆			XX ₁₆
02E5 ₁₆			XX ₁₆
02E6 ₁₆	CAN0 slot 8: Data Field		XX ₁₆
02E7 ₁₆			XX ₁₆
02E8 ₁₆			XX ₁₆
02E9 ₁₆			XX ₁₆
02EA ₁₆			XX ₁₆
02EB ₁₆			XX ₁₆
02EC ₁₆			XX ₁₆
02ED ₁₆			XX ₁₆
02EE ₁₆	CAN0 slot 8: Time Stamp		XX ₁₆
02EF ₁₆			XX ₁₆
02F0 ₁₆	CAN0 slot 9: Identifier / DLC		XX ₁₆
02F1 ₁₆			XX ₁₆
02F2 ₁₆			XX ₁₆
02F3 ₁₆			XX ₁₆
02F4 ₁₆			XX ₁₆
02F5 ₁₆			XX ₁₆
02F6 ₁₆	CAN0 slot 9: Data Field		XX ₁₆
02F7 ₁₆			XX ₁₆
02F8 ₁₆			XX ₁₆
02F9 ₁₆			XX ₁₆
02FA ₁₆			XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆			XX ₁₆
02FD ₁₆			XX ₁₆
02FE ₁₆	CAN0 slot 9: Time Stamp		XX ₁₆
02FF ₁₆			XX ₁₆

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

Address	Register	Symbol	After reset
0300 ₁₆	CAN0 slot 10: Identifier / DLC		XX ₁₆
0301 ₁₆			XX ₁₆
0302 ₁₆			XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆			XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	CAN0 slot 10: Data Field		XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆			XX ₁₆
0309 ₁₆			XX ₁₆
030A ₁₆			XX ₁₆
030B ₁₆			XX ₁₆
030C ₁₆			XX ₁₆
030D ₁₆			XX ₁₆
030E ₁₆	CAN0 slot 10: Time Stamp		XX ₁₆
030F ₁₆			XX ₁₆
0310 ₁₆	CAN0 slot 11: Identifier / DLC		XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆			XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆			XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆	CAN0 slot 11: Data Field		XX ₁₆
0317 ₁₆			XX ₁₆
0318 ₁₆			XX ₁₆
0319 ₁₆			XX ₁₆
031A ₁₆			XX ₁₆
031B ₁₆			XX ₁₆
031C ₁₆			XX ₁₆
031D ₁₆			XX ₁₆
031E ₁₆	CAN0 slot 11: Time Stamp		XX ₁₆
031F ₁₆			XX ₁₆
0320 ₁₆	CAN0 slot 12: Identifier / DLC		XX ₁₆
0321 ₁₆			XX ₁₆
0322 ₁₆			XX ₁₆
0323 ₁₆			XX ₁₆
0324 ₁₆			XX ₁₆
0325 ₁₆			XX ₁₆
0326 ₁₆	CAN0 slot 12: Data Field		XX ₁₆
0327 ₁₆			XX ₁₆
0328 ₁₆			XX ₁₆
0329 ₁₆			XX ₁₆
032A ₁₆			XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆			XX ₁₆
032D ₁₆			XX ₁₆
032E ₁₆	CAN0 slot 12: Time Stamp		XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆	CAN0 slot 13: Identifier / DLC		XX ₁₆
0331 ₁₆			XX ₁₆
0332 ₁₆			XX ₁₆
0333 ₁₆			XX ₁₆
0334 ₁₆			XX ₁₆
0335 ₁₆			XX ₁₆
0336 ₁₆	CAN0 slot 13: Data Field		XX ₁₆
0337 ₁₆			XX ₁₆
0338 ₁₆			XX ₁₆
0339 ₁₆			XX ₁₆
033A ₁₆			XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆			XX ₁₆
033D ₁₆			XX ₁₆
033E ₁₆	CAN0 slot 13: Time Stamp		XX ₁₆
033F ₁₆			XX ₁₆

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

Address	Register	Symbol	After reset
0340 ₁₆	CAN0 slot 14: Identifier / DLC		XX ₁₆
0341 ₁₆			XX ₁₆
0342 ₁₆			XX ₁₆
0343 ₁₆			XX ₁₆
0344 ₁₆			XX ₁₆
0345 ₁₆			XX ₁₆
0346 ₁₆	CAN0 slot 14: Data Field		XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆			XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆			XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆			XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	CAN0 slot 14: Time Stamp		XX ₁₆
034F ₁₆			XX ₁₆
0350 ₁₆	CAN0 slot 15: Identifier / DLC		XX ₁₆
0351 ₁₆			XX ₁₆
0352 ₁₆			XX ₁₆
0353 ₁₆			XX ₁₆
0354 ₁₆			XX ₁₆
0355 ₁₆			XX ₁₆
0356 ₁₆	CAN0 slot 15: Data Field		XX ₁₆
0357 ₁₆			XX ₁₆
0358 ₁₆			XX ₁₆
0359 ₁₆			XX ₁₆
035A ₁₆			XX ₁₆
035B ₁₆			XX ₁₆
035C ₁₆			XX ₁₆
035D ₁₆			XX ₁₆
035E ₁₆	CAN0 slot 15: Time Stamp		XX ₁₆
035F ₁₆			XX ₁₆
0360 ₁₆	CAN0 Global mask	COGMR	XX ₁₆
0361 ₁₆			XX ₁₆
0362 ₁₆			XX ₁₆
0363 ₁₆			XX ₁₆
0364 ₁₆			XX ₁₆
0365 ₁₆			XX ₁₆
0366 ₁₆	CAN0 local mask A	COLMAR	XX ₁₆
0367 ₁₆			XX ₁₆
0368 ₁₆			XX ₁₆
0369 ₁₆			XX ₁₆
036A ₁₆			XX ₁₆
036B ₁₆			XX ₁₆
036C ₁₆	CAN0 local mask B	COLMBR	XX ₁₆
036D ₁₆			XX ₁₆
036E ₁₆			XX ₁₆
036F ₁₆			XX ₁₆
0370 ₁₆			XX ₁₆
0371 ₁₆			XX ₁₆
03B4 ₁₆			
03B5 ₁₆			
03B6 ₁₆			
03B7 ₁₆			
03B8 ₁₆			
03B9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆			

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

5. Electrical Characteristics

Table 5.1 Absolute maximum ratings

Symbol	Parameter		Condition	Rated value	Unit
V _{CC}	Supply voltage			- 0.3 to 6.5	V
V _I	Input voltage	RESET, V _{REF} , X _{IN} P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ , P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂ , CNVss (Note 1)		- 0.3 to V _{CC} + 0.3	V
V _O	Output voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ , P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂ , X _{OUT}		- 0.3 to V _{CC} + 0.3	V
		IV _{CC}		- 0.3 to 2.8V	V
P _d	Power dissipation		T _{opr} = 25 °C	300	mW
T _{opr}	Operating ambient temperature			- 40 to 85 (Note 2)	°C
T _{stg}	Storage temperature			- 65 to 150	°C

Note 1: CNVss pin of flash memory version: -0.3 to 6.5 V

Note 2: When flash memory version is program/erase mode: 0 to 60 °C

Table 5.2 Recommended operating conditions
(Unless otherwise noted: Vcc = 4.2V to 5.5V, Topr = -40 to 85°C)

Symbol	Parameter		Standard			Unit
			Min	Typ.	Max.	
Vcc	Supply voltage		4.2	5.0	5.5	V
Vss	Supply voltage			0		V
VIH	HIGH input voltage	P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52, XIN, RESET, CNVss	0.8Vcc		Vcc	V
VIL	LOW input voltage	P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52, XIN, RESET, CNVss	0		0.2Vcc	V
IOH (peak)	HIGH peak output current	P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52			- 10.0	mA
IOH (avg)	HIGH average output current	P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52			- 5.0	mA
IOL (peak)	LOW peak output current	P00 to P07, P20, P21, P30 to P37, P40 to P47, P50 to P52			10.0	mA
		P10 to P17	HIGH POWER		20.0	mA
			LOW POWER		10.0	
IOL (avg)	LOW average output current	P00 to P07, P20, P21, P30 to P37, P40 to P47, P50 to P52			5.0	mA
		P10 to P17	HIGH POWER		10.0	mA
			LOW POWER		5.0	
f (XIN)	Main clock input oscillation frequency (Note 3)		Vcc=4.2V to 5.5V	0	16	MHz
f (XCIN)	Subclock oscillation frequency			32.768	50	kHz

Note 1: The average output current is an average value measured over 100ms.

Note 2: Keep output current as follows:

The sum of port P00 to P03, P13 to P17, P21, P34 to P37, P46, P47, P50 to P52 IOL (peak) is under 60 mA. The sum of port P00 to P03, P13 to P17, P21, P34 to P37, P46, P47, P50 to P52 IOH (peak) is under 60 mA. The sum of port P04 to P07, P10 to P12, P20, P30 to P33, P40 to P45 IOL (peak) is under 60 mA. The sum of port P04 to P07, P10 to P12, P20, P30 to P33, P40 to P45 IOH (peak) is under 60 mA.

Note 3: Relationship between main clock oscillation frequency and supply voltage is shown as below.

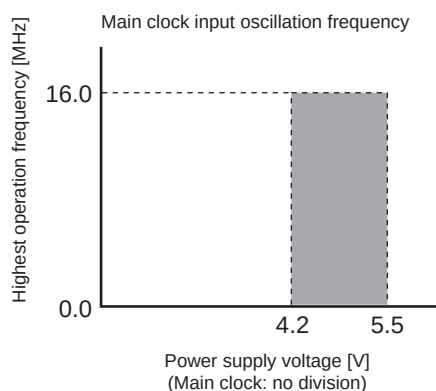


Table 5.3 Electrical characteristics (1)**(Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at Topr = -40 to 85°C, f(X_{IN}) = 16MHz)**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂	I _{OH} = - 5 mA	3.0			V
			I _{OH} = - 200 μA	4.7			
V _{OH}	HIGH output voltage	X _{OUT}	HIGH POWER	3.0			V
			LOW POWER	3.0			
V _{OH}	HIGH output voltage	X _{COUT}	HIGH POWER		2.5		V
			LOW POWER		1.6		
V _{OL}	LOW output voltage	P0 ₀ to P0 ₇ , P2 ₀ , P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂	I _{OL} = 5 mA			2.0	V
			I _{OL} = 200 μA			0.45	
V _{OL}	LOW output voltage	P1 ₀ to P1 ₇	HIGH POWER			2.0	V
			LOW POWER			2.0	
V _{OL}	LOW output voltage	X _{OUT}	HIGH POWER			2.0	V
			LOW POWER			2.0	
V _{OL}	LOW output voltage	X _{COUT}	HIGH POWER		0		V
			LOW POWER		0		
V _{T+} -V _{T-}	Hysteresis	CNTR ₀ , TCIN, INT ₀ to INT ₃ , CLK ₀ , CLK ₁ , P4 ₅ Rx D ₀ , Rx D ₁ , K ₁₀ to K ₁₃ , CRX ₀		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		1.8	V
I _{IH}	HIGH input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ , P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂ , X _{IN} , RESET, CNV _{SS}	V _I = 5V			5.0	μA
I _{IL}	LOW input current	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ , P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂ , X _{IN} , RESET, CNV _{SS}	V _I = 0V			-5.0	μA
R _{PULLUP}	Pull-up resistor	P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ , P2 ₁ , P3 ₀ to P3 ₇ , P4 ₀ to P4 ₇ , P5 ₀ to P5 ₂	V _I = 0V	30.0	50.0	167.0	kΩ
R _{fxIN}	Feedback resistor	X _{IN}			1.0		MΩ
R _{fxCIN}	Feedback resistor	X _{CIN}			15.0		MΩ
V _{RAM}	RAM retention voltage		When clock is stopped	2.0			V
ROSC	Oscillation frequency of On-chip oscillator	Mask ROM		300	600	1200	kHz
		Flash memory					

Table 5.4 Electrical characteristics (2)(Unless otherwise noted: $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_{opr} = 25^{\circ}C$, $f(X_{IN}) = 16MHz$)

Symbol	Parameter	Measuring condition			Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current	I/O pin has no load	Mask ROM	f(Xin) = 16 MHz Square wave, no division		12.0	22.0	mA
			Flash memory			14.0	24.0	mA
			Mask ROM	On-chip oscillator mode No division		300		μA
			Flash memory			800		μA
			Mask ROM	On-chip oscillator mode When a WAIT instruction is executed		60		μA
			Flash memory			100		μA
			Mask ROM	f(Xcin) = 32 kHz Square wave		20		μA
			Flash memory			450		μA
			Mask ROM	f(Xcin) = 32 kHz When a WAIT instruction is executed		2		μA
			Flash memory			2		μA
			Mask ROM	Topr = 25 °C when clock is stopped		0.8	3	μA
			Flash memory			0.8	3	μA

Table 5.5 Power supply timing circuit characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Timer for internal power supply stabilization during powering-on	$V_{CC} = 4.2$ to $5.5 V$			2	ms
td(R-S)	Stop release time				150	μs
td(W-S)	Wait release time during low power dissipation mode				150	μs
td(M-L)	Timer for internal power supply stabilization when main clock oscillation starts				150	μs

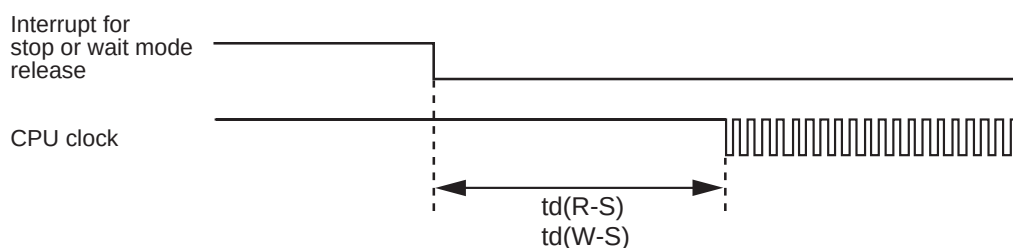


Table 5.6 Flash memory version electrical characteristics
(Unless otherwise noted: Vcc = 4.2 to 5.5 V, Topr= 0 to 60°C)

Symbol	Parameter	Standard			Unit
		Min.	Typ. (Note 1)	Max.	
-	Erase/write cycle (Note 2)	100 (Note 3)			cycle
-	Word programming time		75	600	μs
-	Block erasing time	2Kbyte block	0.2	9	s
		8Kbyte block	0.4	9	s
		16Kbyte block	0.7	9	s
		32Kbyte block	1.2	9	s
td(SR-ES)	Transition time from erasure operation to erase-suspend			20	ms
-	Data retention	10			year

Note1: Vcc=5.0V, Topr=25°C

Note2: Definition of Programming and erasure times

The Programming and erasure times are defined to be per-block erasure times. For example a case where a 2K-byte block is programmed in 1,024 operations by writing one word at a time and erased thereafter. Performing multiple programs to the same address before an erase operation is prohibited.

Note 3: Minimum number of programming/erasure for which operation is guaranteed.

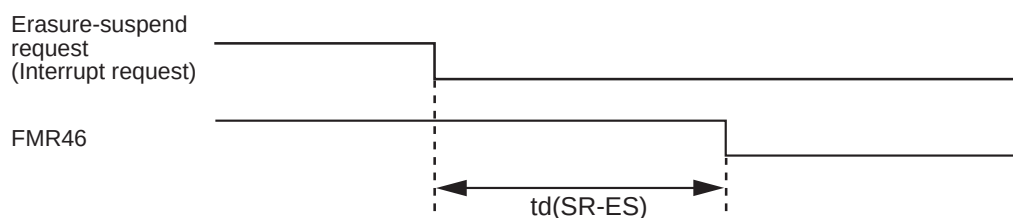


Table 5.7 A/D conversion characteristics**(Unless otherwise noted: $V_{CC} = V_{REF} = 5V$, $V_{SS} = 0V$ at $T_{opr} = 25^{\circ}C$, $f(X_{IN}) = 16MHz$)**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		$V_{REF} = V_{CC}$			10	Bits
—	Absolute accuracy	Sample & hold function not available	$V_{REF} = V_{CC} = 5V$			± 3	LSB
		Sample & hold function available(10bit)	$V_{REF} = V_{CC} = 5V$ AN ₀ to AN ₁₁ input ANEX ₀ , ANEX ₁ input, external op-amp connected mode			± 3	LSB
						± 7	LSB
		Sample & hold function available(8bit)	$V_{REF} = V_{CC} = 5V$			± 2	LSB
R _{LADDER}	Ladder resistance		$V_{REF} = V_{CC}$	10		40	kΩ
t _{CONV}	Conversion time(10bit)		$f(X_{IN})=10MHz$, $\emptyset_{AD}=f_{AD}=10MHz$	3.3			μs
t _{CONV}	Conversion time(8bit)		$f(X_{IN})=10MHz$, $\emptyset_{AD}=f_{AD}=10MHz$	2.8			μs
t _{SAMP}	Sampling time		$f(X_{IN})=10MHz$, $\emptyset_{AD}=f_{AD}=10MHz$	0.3			μs
V _{REF}	Reference voltage		$f(X_{IN})=10MHz$, $\emptyset_{AD}=f_{AD}=10MHz$	2		V _{CC}	V
V _{IA}	Analog input voltage		$f(X_{IN})=10MHz$, $\emptyset_{AD}=f_{AD}=10MHz$	0		V _{REF}	V

Note 1: Divide the f_{AD} if f(X_{IN}) exceeds 10MHz, and make AD operation clock frequency (∅_{AD}) equal to or lower than 10MHz.

Table 5.8 D/A conversion characteristics**(Unless otherwise noted: $V_{CC} = V_{REF} = 5V$, $V_{SS} = 0V$ at $T_{opr} = 25^{\circ}C$, $f(X_{IN}) = 16MHz$)**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy					1.0	%
t _{su}	Setup time					3	μs
R _o	Output resistance			4	10	20	kΩ
I _{VREF}	Reference power supply input current		(Note 1)			1.5	mA

Note 1: The A/D converter's ladder resistance is not included.

When D/A register contents are not "00₁₆", the current I_{VREF} always flows even though V_{REF} may have been set to be unconnected by the A/D control register.

5.1 Timing requirements

(Unless otherwise noted: $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_{opr} = -40$ to $85^{\circ}C$)

Table 5.9 X_{IN} input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	X _{IN} input cycle time	62.5		ns
$t_{wH(XIN)}$	X _{IN} input HIGH pulse width	30		ns
$t_{wL(XIN)}$	X _{IN} input LOW pulse width	30		ns

Table 5.10 CNTR₀ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR ₀ input cycle time	100		ns
$t_{wH(CNTR0)}$	CNTR ₀ input HIGH pulse width	40		ns
$t_{wL(CNTR0)}$	CNTR ₀ input LOW pulse width	40		ns

Table 5.11 TCIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	400(Note 1)		ns
$t_{wH(TCIN)}$	TCIN input HIGH pulse width	200(Note 2)		ns
$t_{wL(TCIN)}$	TCIN input LOW pulse width	200(Note 2)		ns

Note 1: Use the greater value, either (1/digital filter clock frequency X 6) or min. value.

Note 2: Use the greater value, either (1/digital filter clock frequency X 3) or min. value.

Table 5.12 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CLK)}$	CLK _i input cycle time	200		ns
$t_{w(CKH)}$	CLK _i input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLK _i input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxD _i output delay time		80	ns
$t_{h(C-Q)}$	TxD _i hold time	0		ns
$t_{su(D-C)}$	RxD _i input setup time	30		ns
$t_{h(C-D)}$	RxD _i input hold time	90		ns

Table 5.13 External interrupt $\overline{INT_i}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input HIGH pulse width	250(Note 1)		ns
$t_{w(INL)}$	$\overline{INT_i}$ input LOW pulse width	250(Note 2)		ns

Note 1: When the $\overline{INT_0}$ input filter select bit selects the digital filter, use the $\overline{INT_0}$ input HIGH pulse width to the greater value, either (1/digital filter clock frequency X 3) or min. value.

Note 2: When the $\overline{INT_0}$ input filter select bit selects the digital filter, use the $\overline{INT_0}$ input LOW pulse width to the greater value, either (1/digital filter clock frequency X 3) or min. value.

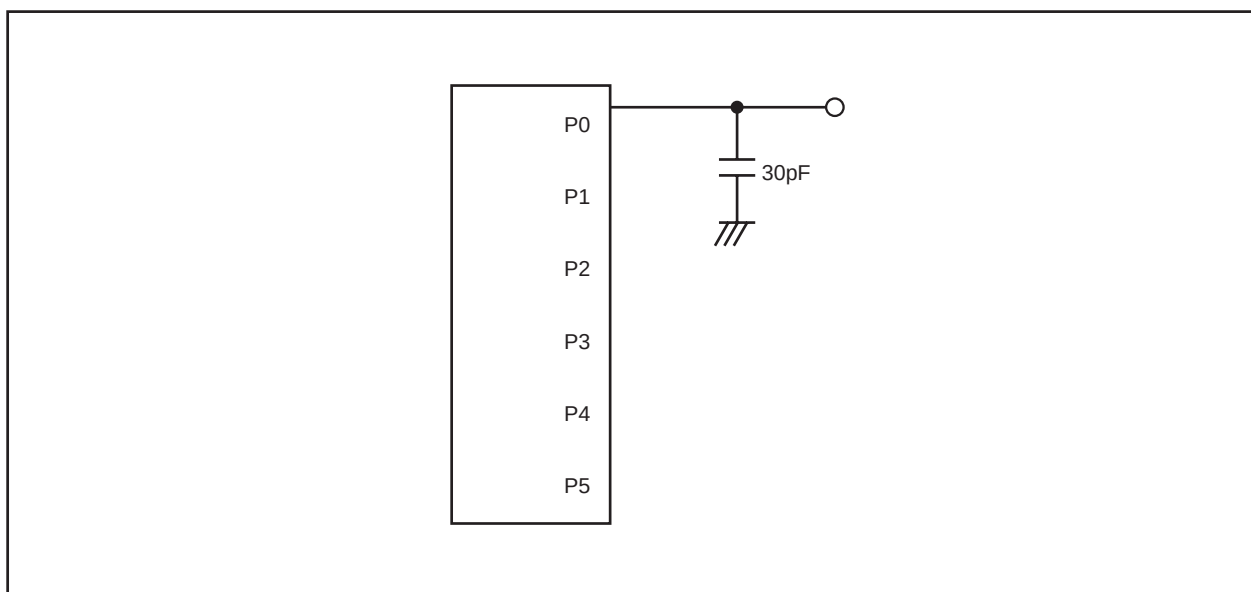
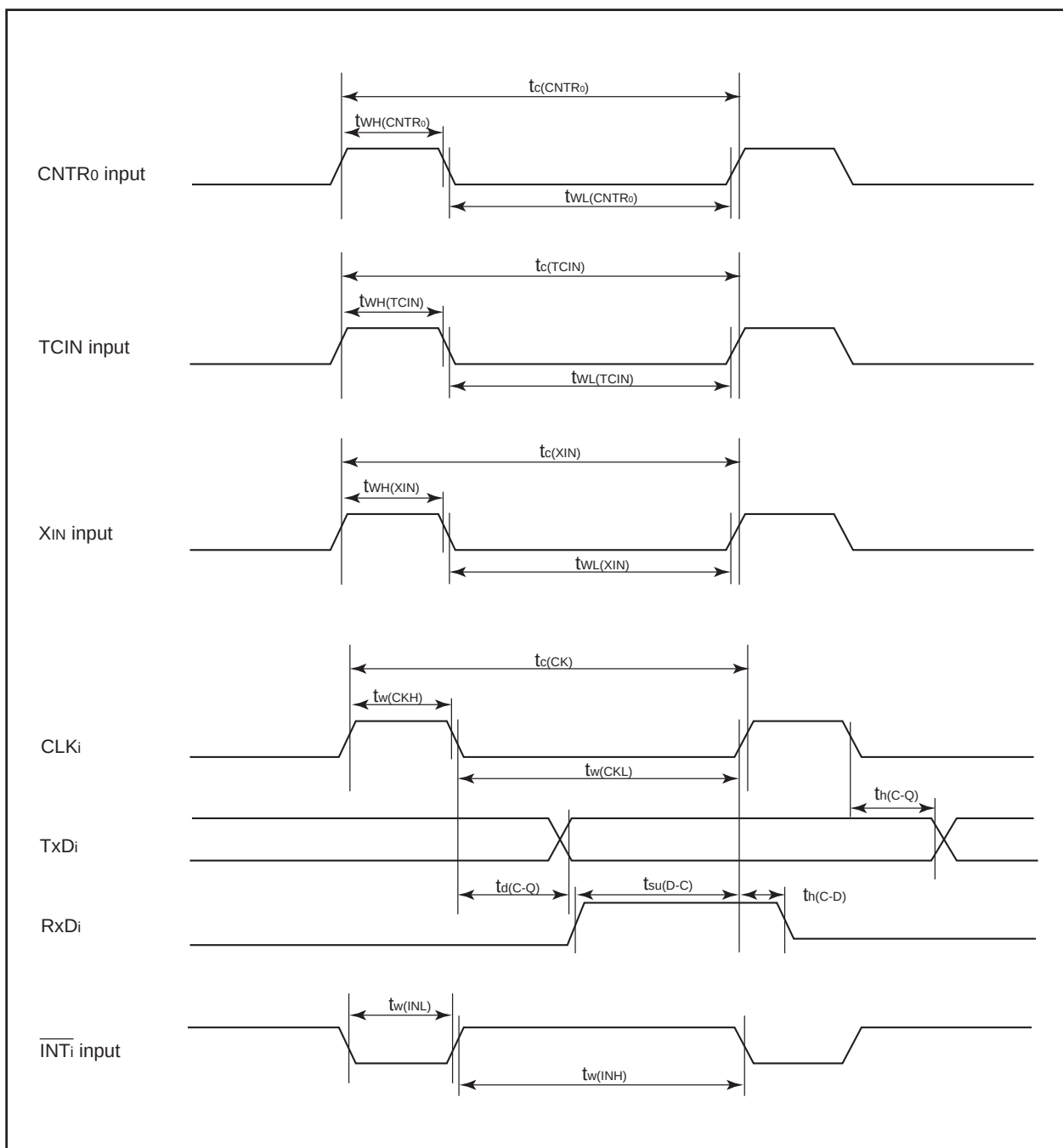


Figure 5.1 Port P0 to P5 measurement circuit

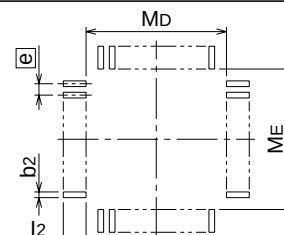
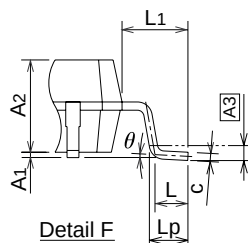
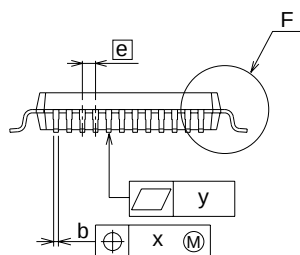
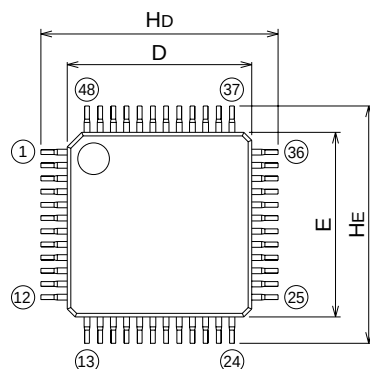
Figure 5.2 $V_{CC}=5V$ timing diagram

Package Dimension

48P6Q-A Recommended

Plastic 48pin 7X7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	—	—	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.5	—
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	8°
b2	—	0.225	—
l2	1.0	—	—
MD	—	7.4	—
ME	—	7.4	—

REVISION HISTORY	M16C/1N Group Data Sheet
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Rev.	Date	Description	
		Page	Summary
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