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MOTOROLA

MC34058
MC34059

Advance Information

Hex EIA-485 Transceiver with Three-State Outputs

HEX EIA–485 TRANSCEIVER with THREE–STATE OUTPUTS

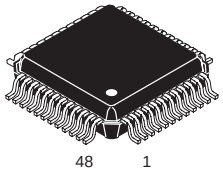
SEMICONDUCTOR TECHNICAL DATA

The Motorola MC34058/9 Hex Transceiver is composed of six driver/receiver combinations designed to comply with the EIA–485 standard. Features include three–state outputs, thermal shutdown for each driver, and current limiting in both directions. This device also complies with EIA–422 and CCITT Recommendations V.11 and X.27.

The devices are optimized for balanced multipoint bus transmission at rates to 20 MBPS (MC34059). The driver outputs/receiver inputs feature a wide common mode voltage range, allowing for their use in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions.

The MC34058/9 is available in a space saving 7.0 mm 48 lead surface mount quad package designed for optimal heat dissipation.

- Meets EIA–485 Standard for Party Line Operation
- Meets EIA–422A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: 0°C to +70°C
- Common Mode Driver Output/Receiver Input Range: –7.0 to +12 V
- Positive and Negative Current Limiting
- Transmission Rates to 14 MBPS (MC34058) and 20 MBPS (MC34059)
- Driver Thermal Shutdown at 150°C Junction Temperature
- Thermal Shutdown Active Low Output
- Single +5.0 V Supply, ±10%
- Low Supply Current
- Compact 7.0 mm 48 Lead TQFP Plastic Package

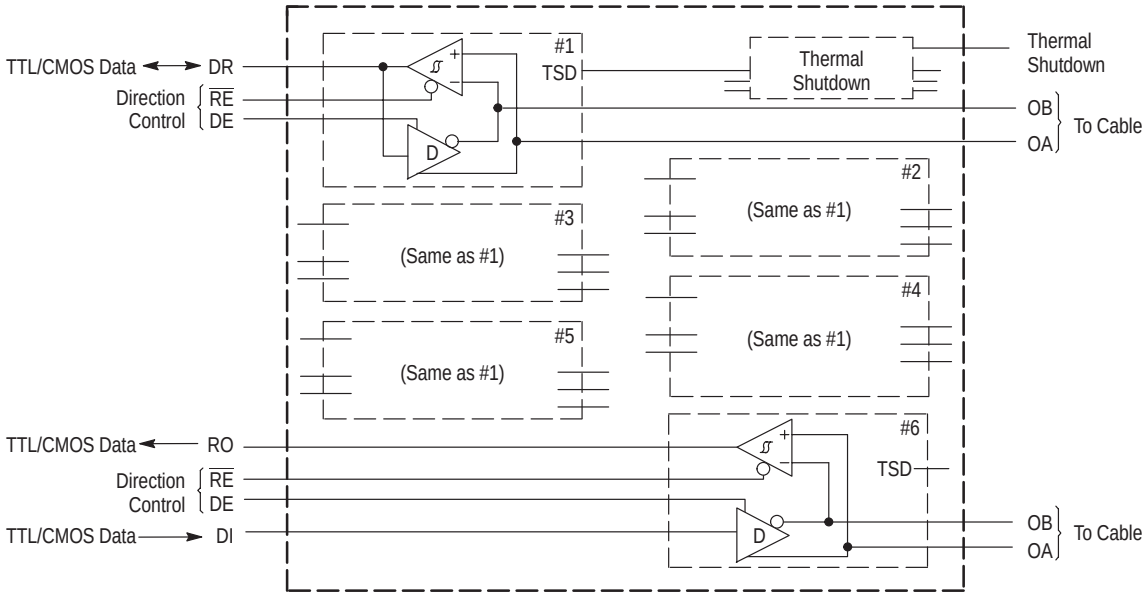


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34058FTA	T_A = 0° to +70°C	TQFP–48
MC34059FTA		

Representative Block Diagram



This device contains 1,399 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5, 7.0	Vdc
Input Voltage (Driver Data, Enables)	V_{in}	7.0	Vdc
Applied Driver Output Voltage When in Three–State Condition (V_{CC} = 5.0 V)	V_Z	–10, 14	Vdc
Applied Driver Output Voltage When V_{CC} = 0 V	V_X	±14	Vdc
Output Current	I_O	Self Limiting	–
Storage Temperature	T_{stg}	–65, 150	°C

NOTE: Devices should not be operated at these limits. The "Recommended Operating Conditions" provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS (All limits are not necessarily functional concurrently.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Voltage (All Inputs Except Receiver Inputs)	V_{in}	0	–	V_{CC}	Vdc
Driver Output Voltage in Three–State Condition, Receiver Inputs, or When V_{CC} = 0 V	V_{CM}	–7.0	–	12	Vdc
Driver Output Current (Normal Data Transmission)	I_O	–60	–	60	mA
Operating Ambient Temperature	T_A	0	–	70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V ± 10%)

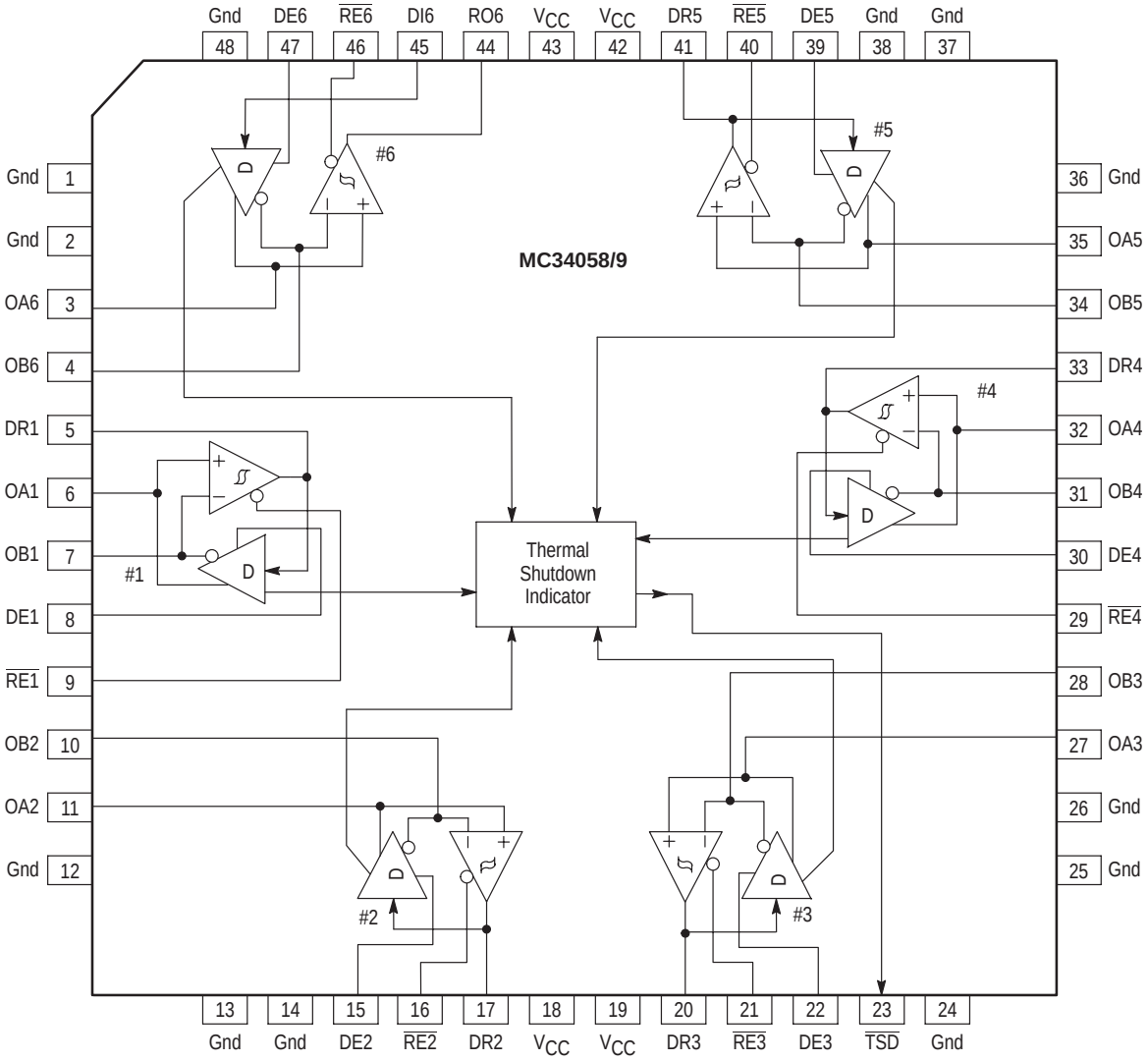
Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER CHARACTERISTICS					
Output Voltage					
Single Ended, I_O = 0	V_O	0	–	V_{CC}	Vdc
Differential, Open Circuit (I_O = 0)	$\|V_{OD1}\|$	1.5	–	–	Vdc
Differential, R_L = 54 Ω	$\|V_{OD2}\|$	1.5	–	–	Vdc
Change in Differential Voltage (Note 1), R_L = 54 Ω	$\|\Delta V_{OD2}\|$	–	–	200	mVdc
Differential, R_L = 100 Ω	$\|\Delta V_{OD2A}\|$	2.0	–	–	Vdc
Change in Differential Voltage (Note 1), R_L = 100 Ω	$\|V_{OD2A}\|$	–	–	200	mVdc
Common Mode Voltage, R_L = 54 Ω	V_{OCM}	–	–	3.0	Vdc
Common Mode Voltage Change, R_L = 54 Ω	$\|\Delta V_{OCM}\|$	–	–	200	mVdc
Output Current (Each Output)					mA
Short Circuit Current, –7.0 V ≤ V_O ≤ 12 V	I_{OS}	–250	–	250	
Driver Data Inputs					Vdc
Low Level Voltage	V_{ILD}	–	–	0.8	
High Level Voltage	V_{IHD}	2.0	–	–	
Clamp Voltage (I_{in} = –18 mA)	V_{IKD}	–1.5	–	–	
Thermal Shutdown Junction Temperature	T_{JTS}	–	150	–	°C
RECEIVER CHARACTERISTICS					
Input Threshold R_O = High	V_{th}	–	–	200	mVdc
R_O = Low		–200	–	–	
Input Loading (Driver Disabled)		–	0.36	1.0	U.L.
Hysteresis	V_H	–	100	–	mV
Output Voltage High (I_{OH} = –400 μA)	V_{OHR}	2.4	–	–	Vdc
Low (I_{OL} = 4.0 mA)	V_{OLR}	–	–	0.4	
Output Short Circuit Current	I_{OSR}	–	45	85	mA
Output Leakage Current When in Three–State Mode	I_{OLKR}	–	–	20	μA

NOTE: 1. Input switched from low to high.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 5.0 V ± 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
MISCELLANEOUS					
Enable Inputs					Vdc
Low Level Voltage	V_{ILE}	0	–	0.8	
High Level Voltage	V_{IHE}	2.0	–	V_{CC}	
Clamp Voltage (I_{in} = –18 mA)	V_{IKE}	–1.5	–	–	
Power Supply Current (Total Package, All Outputs Open, Enabled or Disabled)	I_{CC}	–	18	28	mA
Thermal Shutdown Output Voltage					Vdc
High	V_{OHT}	2.4	–	–	
Low	V_{OLT}	0	–	0.8	
TIMING CHARACTERISTICS – DRIVER					
Propagation Delay – Input to Single Ended Output					ns
Input to Output – Low–to–High	t_{PLH}	–	10	20	
Input to Output – High–to–Low	t_{PHD}	–	11	20	
Propagation Delay – Input to Differential Output					ns
Input Low–to–High	t_{PLHD}	–	15	23	
Input High–to–Low	t_{PHLD}	–	15	23	
Differential Output Transition Time	t_{DR}, t_{DF}	–	9.0	10.7	ns
Skew Timing MC34058					ns
$\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver	t_{SK1}	0	0.1	–	
Maximum – Minimum t_{PLHD} Within a Package	t_{SK2}	0	–	8.0	
Maximum – Minimum t_{PHLD} Within a Package	t_{SK3}	0	–	6.0	
Skew Timing MC34059					ns
$\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver	t_{SK7}	0	0.1	–	
Propagation Delay Difference Between Any Two Drivers (Same Package or Different Packages at Same V_{CC} and T_A)	t_{SK8}	–	<4.0	–	
Enable Timing					ns
Single Ended Outputs					
Enable to Active High Output	t_{PZH}	–	15	40	
Enable to Active Low Output	t_{PZL}	–	25	40	
Active High to Disable	t_{PHZ}	–	12	25	
Active Low to Disable	t_{PLZ}	–	10	25	
Differential Outputs					
Enable to Active Output	t_{PZD}	–	–	40	
Enable to Three–State Output	t_{PDZ}	–	–	25	
TIMING CHARACTERISTICS – RECEIVER					
Propagation Delay					ns
Input to Output – Low–to–High	t_{PLHR}	–	16	23	
Input to Output – High–to–Low	t_{PHLR}	–	16	23	
Skew Timing					ns
$\lvert t_{PLHR} - t_{PHLR} \rvert$ for Each Receiver	t_{SK4}	0	1.0	–	
Maximum – Minimum t_{PLHR} Within a Package	t_{SK5}	0	–	3.0	
Maximum – Minimum t_{PHLR} Within a Package	t_{SK6}	0	–	3.0	
Skew Timing	t_{SK9}	–	<5.0	–	ns
Propagation Delay Difference Between Any Two Receivers in Different Packages at Same V_{CC} and T_A (MC34059 Only)					
Enable Timing					ns
Single Ended Outputs					
Enable to Active High Output	t_{PZHR}	–	15	22	
Enable to Active Low Output	t_{PZLR}	–	25	30	
Active High to Disable	t_{PHZR}	–	12	25	
Active Low to Disable	t_{PLZR}	–	10	25	

Block Diagram and Pinout



PINOUT SUMMARY

OA	NonInverting Output/Input	DE	Driver Enable, Active High (TTL)
OB	Inverting Output/Input	$\overline{RE}$	Receiver Enable, Active Low (TTL)
DR	Driver Input/Receiver Output (TTL)	$\overline{TSD}$	Thermal Shutdown Indicator
DI6	#6 Driver Input (TTL)	V_{CC}	Connect 4 Pins to 5.0 V, ±10%
RO6	#6 Receiver Output (TTL)	Gnd	Connect 12 Pins to Circuit Ground

Figure 1. V_{OD} and V_{OS} Test Circuit

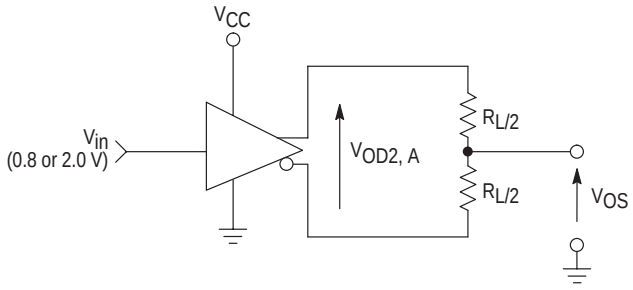


Figure 2. V_{OD} and V_{CM} Test Circuit

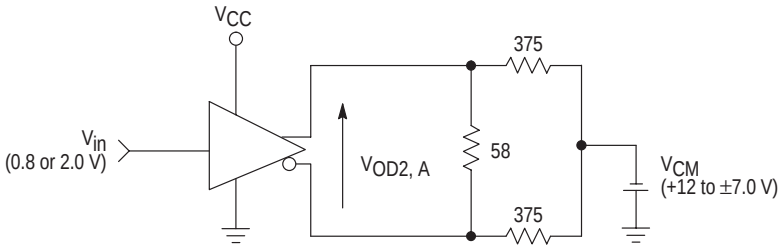


Figure 3. V_{OD} AC Test Conditions

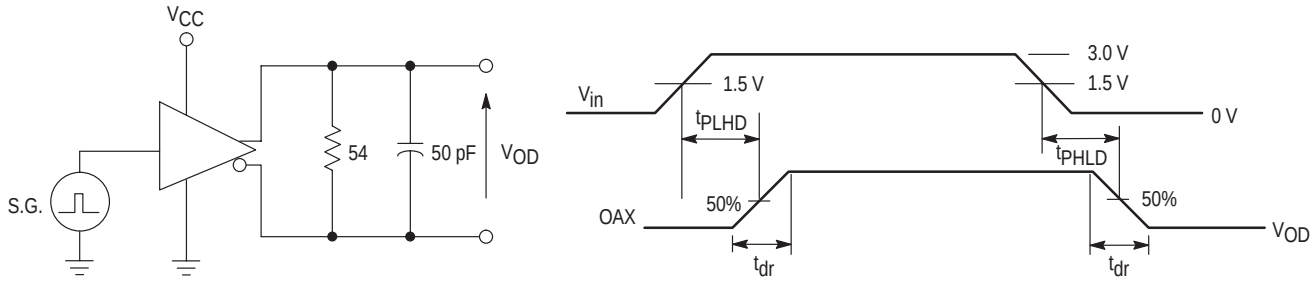


Figure 4. V_{OH} and V_{OL} AC Test Conditions

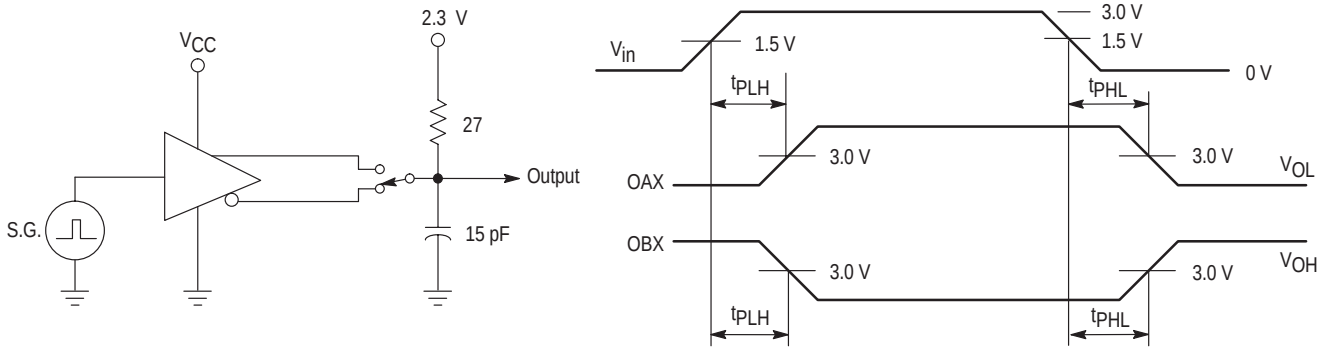


Figure 5. V_{OH} versus I_{OH}

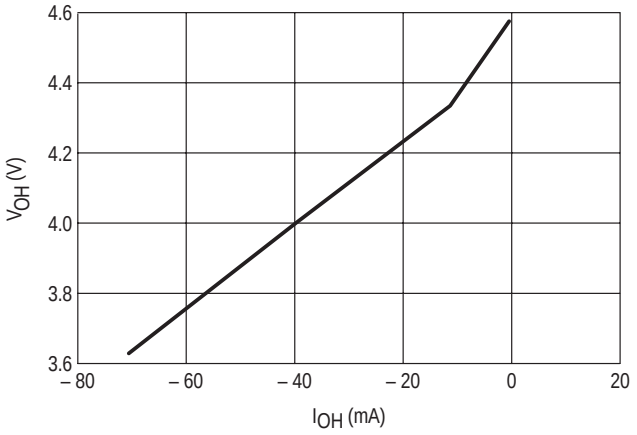


Figure 6. V_{OL} versus I_{OL}

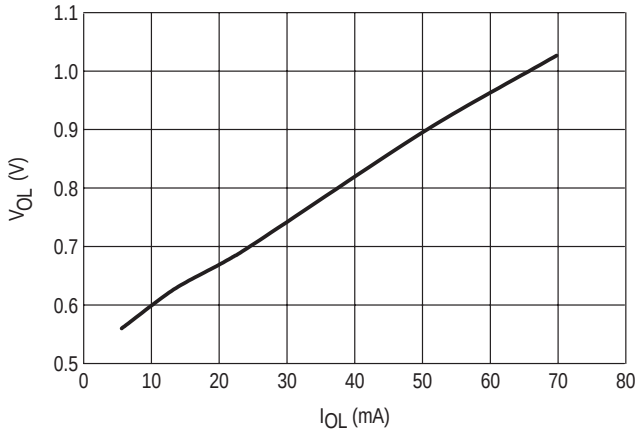


Figure 7. V_{OD} versus I_{OL}

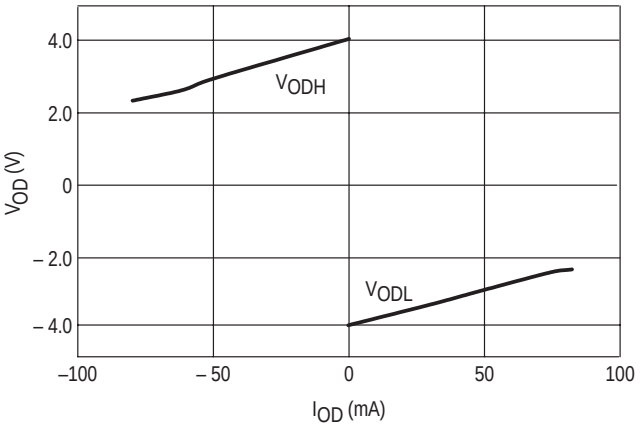
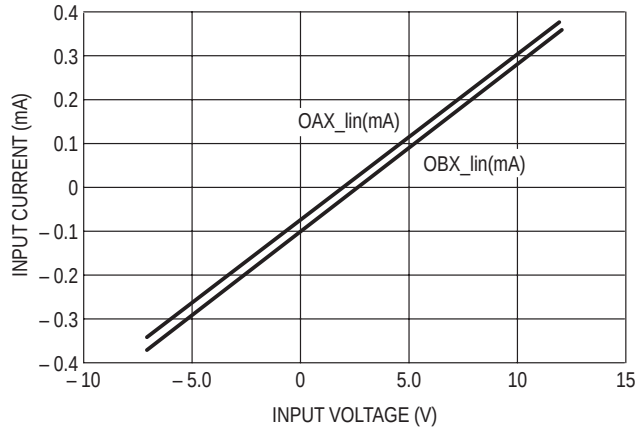


Figure 8. Input Characteristics of OAX and OAB



Description

The MC34058/9 is a differential line driver designed to comply with EIA–485 Standard for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA–422–A and CCITT Recommendations V.11 and X.27. Positive and negative current limiting of the drivers meet the EIA–485 requirement for protection from damage in the event that two or more drivers try to transmit simultaneously on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. Only a single power supply, 5.0 V ±10% is required.

Driver Inputs

The driver inputs and enable logic determine the state of the outputs in accordance with Table 1. The driver inputs have a nominal threshold of 1.2 V, and the voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground or above V_{CC}, excessive currents will flow and proper operation of the drivers will be affected. An open Pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The inputs are TTL type and their characteristics are unchanged by the state of the enable pins.

Driver Outputs

Each output (when active) will be a low or a high voltage, depending on the input state and the load current (see Tables 1, 2 and Figures 2 and 3). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

Table 1. Driver Truth Table

Driver Data Inputs	Enables		Outputs	
	DEX	REX	OAX	OBX
H	H	H	H	L
L	H	H	L	H
X	L	H	Z	Z
X	H	L	Not Defined	Not Defined

The outputs will be in a high impedance state when:
a) The Enable inputs are set according to Table 1;
b) The junction temperature exceeds the trip point of the thermal shutdown circuit. When in this condition, the output's source and sink capability are shut off, and a leakage current of less than 20 μA will flow. Disabled outputs may be taken to any voltage between –7.0 V and 12 V without damage to internal circuitry.

The drivers are protected from short circuits by two methods:
a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the 12 V to –7.0 V range, with respect to circuit ground. The short circuit current will flow until the fault is removed, or until the thermal shutdown activates. The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.
b) A thermal shutdown circuit disables the outputs when the junction temperature reaches +150°C, ± 20°C. The thermal shutdown circuit has a hysteresis of ~ 12°C to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. However, the remainder of the internal circuitry remains biased and the outputs will become active once again as the IC cools down.

Receiver Inputs

The receiver inputs and enable logic determine the state of the receiver outputs in accordance with Table 2. Each receiver input pair has a nominal differential threshold of at most 200 mV (Pin OAX with respect to OBX) and a common mode voltage range of –7.0 V and 12 V must be maintained for proper operation. A nominal hysteresis of 100 mV is typical. The receiver input characteristics are shown in Figure 8. When the inputs are in the high impedance state, they remain capable of the common mode voltage range of –7.0 V to 12 V.

Receiver Outputs

The receiver outputs are TTL type outputs and act in accordance with Table 2.

Enable Logic

Each driver output is active when the Driver Enable input is true according to Table 1. Each receiver output is active when the Receiver Enable input is true according to Table 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V and V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground or above V_{CC}, excessive currents will flow and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The enable inputs are TTL compatible. Since the same pins are used for driver input and receiver output, care must be taken to make sure that DEX and $\overline{REX}$ are not both enabled. This may result in corruption of both the transmitted and received data.

Table 2. Receiver Truth Table

Receiver Data Inputs	Enables		Outputs
OAX–OBX	DEX	$\overline{REX}$	DRX
≥ +200 mV	L	L	H
≤ –200 mV	L	L	L
X	L	H	Z
X	H	L	Not Defined

APPLICATIONS

The MC34058/9 was designed to meet EIA/TIA–422 and EIA/TIA–485 standards. EIA/TIA–422 specifies balanced point–to–point transmission with the provision for multiple receivers on the line. EIA/TIA–485 specifies balanced point–to–point transmission and allows for multiple drivers and receivers on the line. Refer to EIA/TIA documents for more details. Figure 9 shows a typical EIA/TIA–422 example. Figure 10 shows a typical EIA/TIA–485 example.

Figure 9. Typical EIA/TIA–422 Application

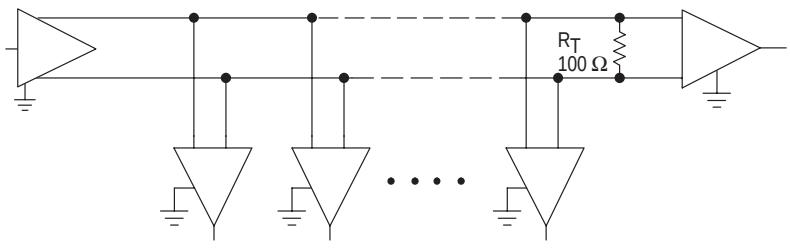
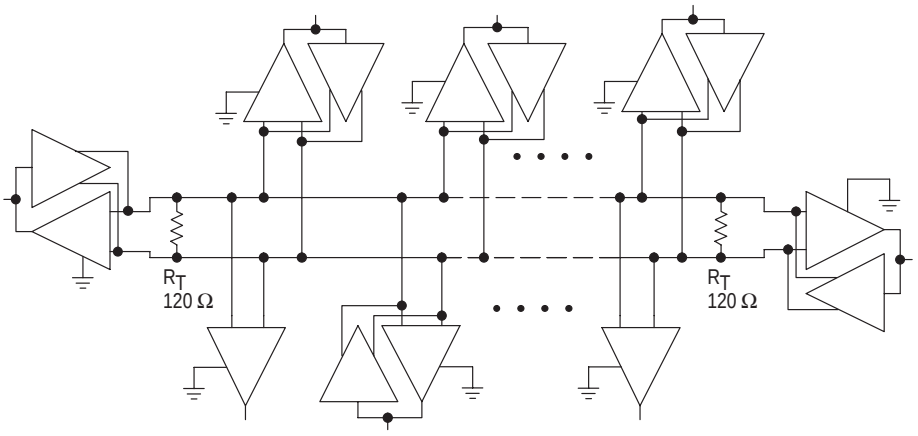
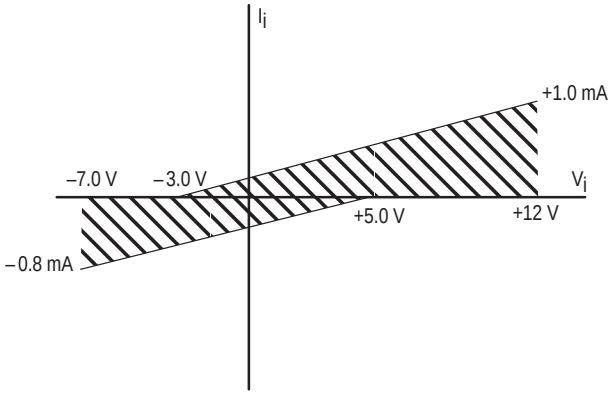


Figure 10. Typical EIA/TIA–485 Application



EIA/TIA–422 specifications require the ability to drive at least 10 receivers of input impedance of greater than or equal to 4.0 KΩ plus the 100 Ω termination resistor. This protocol was intended for unidirectional transmission. EIA/TIA–485 is capable of bidirectional transmission by allowing multiple drivers and receivers on the same twisted pair segment. The loading of the twisted pair segment can be up to 32 Unit Loads (U.L.) plus the two 120 Ω terminating resistors. The U.L. definition is shown in Figure 11.

Figure 11. TIA/EIA–485 Unit Load Definition



Calculating Power Dissipation for the MC34058/9 Hex–Transceiver.

The operational temperature range is listed as 0°C to 70°C to satisfy both EIA/TIA–485 and EIA/TIA–422 specifications. However, a lower ambient temperature may be required depending on the specific board layout and/or application.

Using a first order approximation for heat transfer, the maximum power which may be dissipated by the package is determined by (see Appendix A for more details);

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta ja} \quad \textbf{[1]}$$

where:

θja = package thermal resistance (see Appendix A)

T_{Jmax} = Maximum Junction Temperature. Since the thermal shutdown feature has a trip point of 150°C ± 20°, T_{Jmax} is selected to be +130°C.

T_A = Ambient Operating Temperature.

The power generated within the package is then;

$$PD = \left\{\left[\left(V_{CC} - V_{OH_1}\right)\cdot I_{OH_1}\right] + V_{OL_1}\cdot I_{OL_1}\right\} + \text{..}$$

$$\text{(each\_driver).. } + \left\{\left[\left(V_{CC} - V_{OH_6}\right)\cdot I_{OH_6}\right] + V_{OL_6}\cdot I_{OL_6}\right\} + V_{CC}\cdot I_{CCQ} \quad \textbf{[2]}$$

As indicated in the equation, the part of Equation 2 consisting of I_{OH} , V_{OH} , I_{OL} and V_{OL} must be calculated for each of the drivers and summed for the total power dissipation estimate. The last term can be considered the quiescent power required to keep the IC operational and is measured with the drivers idle and unloaded. The V_{OH} and V_{OL} terms can be determined from the output current versus output voltage curves which provide driver output characteristics.

Example 1 estimates thermal performance based on current requirements.

Example 1. Balanced and Unbalanced Operation

I_{OL} = 50 mA and I_{OH} = ±50 mA for each driver. V_{CC} = 5.0 V.
How many drivers can be used? (Typical power supply current I_{CCQ} = 18 mA.)

Solution:

I_{CCQ} = 0.018 A
The quiescent power is given by: $PQ = I_{CCQ} \cdot V_{CC}$, and is equal to PQ = 0.09 W.

Balanced Operation:

To determine the amount of power dissipated by each output stage we need to know the differential output voltage for the output current required. Figure 7 shows that for I_{OH} and I_{OL} differential of 50 mA, V_{ODH} and V_{ODL} are:

$V_{OD} = |3.0|$, and $I_{OL} = |I_{OH}| = I_{Out} = 0.050$ A.

And the power dissipated by each driver is given by;

$P_{DrvB} = I_{Out} \cdot \left(V_{CC} - V_{OD}\right)$ and equal to

$P_{DrvB} = 0.10$ W.

Unbalanced Operation:

To determine the amount of power dissipated by each output stage we need to know the single–ended output voltage for the output current required. Figures 5 and 6 shows that for an I_{OH} and I_{OL} of ±50 mA,

$V_{OH} = 3.9$ V $V_{OL} = 0.895$ V

And the power dissipated by each driver is calculated by;

$P_{DrvU} = \left(V_{CC} - V_{OH}\right) \cdot |I_{OH}| + V_{OL} \cdot I_{OL}$

and equal to

$P_{DrvU} = 0.10$ W.

(For this example, balanced operation is assumed.)

Summing the quiescent and driver power for 6 transceivers operating in a package produces;

$$P_{DTotal} = PQ + 6 \cdot P_{DrvB}, \text{ and equal to } P_{DTotal} = 0.69 \text{ W.}$$

For the MC34058/9, the thermal resistance is capable of a wide range. The ability of the package to dissipate power depends on board type and temperature, layout and ambient temperature (see Appendix A). For the purposes of this example the thermal resistance can range from 40°C/W to 100°C/W;

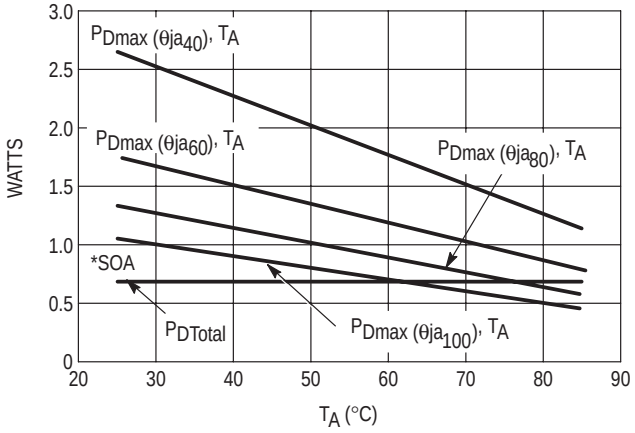
$$\theta ja = j,\ j = 40, 60, .. 100°C/W.$$

Varying the ambient operating temperature T_A = 25, 30, .. 85°C; specifying a maximum junction temperature to avoid thermal shutdown T_{Jmax} = 130°C; and using the first order approximation for maximum power dissipation;

$$P_{Dmax(\theta ja)},\ T_A = \frac{T_{Jmax} - T_A}{\theta ja}$$

produces a set curves that can be used to determine a Safe Operating Area for the specific application. P_{DTotal} is graphed with P_{Dmax} to provide a reference.

Graph of Maximum Power Dissipation Possible for a Particular θja and Ambient Temperature

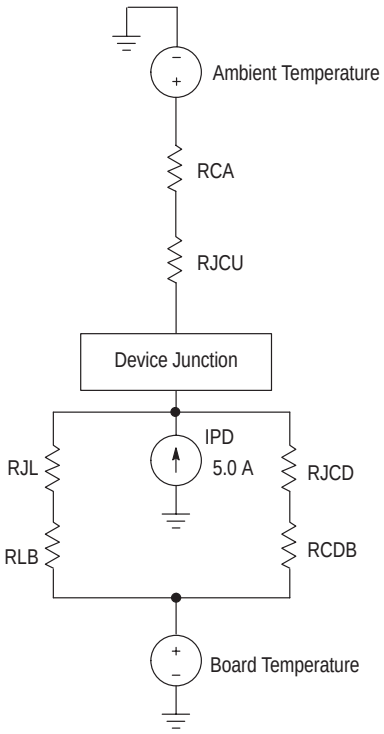


* Safe Operating Area (SOA), is an operating power, P_{DTotal}, less than P_{Dmax}.

So all the drivers in the package can be used if the thermal resistance and/or the ambient temperature is low enough.

Appendix A. Optimizing the Thermal Performance of the MC34058/9

Figure 12. Electrical Model of Package Heat Transfer



An equivalent electrical circuit for the thermal model for the MC34058/9 package is shown in Figure 12. It is a simplified model that shows the dominant means of heat transfer from the thermally enhanced 48–ld package used for the MC34058/9. The model is a first order approximation and is intended to emphasize the need to consider thermal issues when designing the IC into any system. It is however customary to use similar models and Equation 1 to estimate device junction temperatures.

Equation 1 is the common means of using the thermal resistance of a package to estimate junction temperature in a particular system.

$$T_J = \left(P_D \cdot \theta jx\right) + T_A \qquad \textbf{[1]}$$

The term θjx in Equation 1 is usually quoted as a øja value in °C/Watt. However, since the 48–ld package for the MC34058/9 has been thermally enhanced to take advantage of other heat sinking potentials, it must be modified. θjx must actually be considered a composite of all the heat transfer paths from the chip. That is, the three dominant and parallel paths shown in Figure 12. Of those three paths, potentially the most effective is the corner package leads. This is because these corner leads have been attached to the flag on which the silicon die is situated. These pins can be connected to circuit board ground to provide a more efficient conduction path for internal package heat. This path is modeled as the Rjl (junction–to–leads) and Rlb (leads–to–board) combination in Figure 12. This path provides the most effective way of removing heat from the device provided that there is a viable temperature potential (i.e. heat sinking source) to conduct towards. However, if it is not properly considered in the system design, the other paths, (Rjcd + Rcdb) and (Rjcu + Rca) attain greater importance and must be more carefully considered.

So Equation 1, modified to reflect a more complete heat transfer model becomes;

$$T_J = T_A \cdot \frac{\left(\frac{1}{\frac{1}{Rjcd} + \frac{1}{Rjlb}}\right)}{\left(\frac{1}{\frac{1}{Rjcd} + \frac{1}{Rjlb}}\right) + Rjca} + \ldots$$

$$\ldots\ T_B \cdot \frac{Rjca}{\left(\frac{1}{\frac{1}{Rjcd} + \frac{1}{Rjlb}}\right) + Rjca} + PDISS \cdot \theta ja \qquad \textbf{[2]}$$

where;

T_J= Junction Temperature

T_A = Ambient Temperature

T_B = Board Temperature

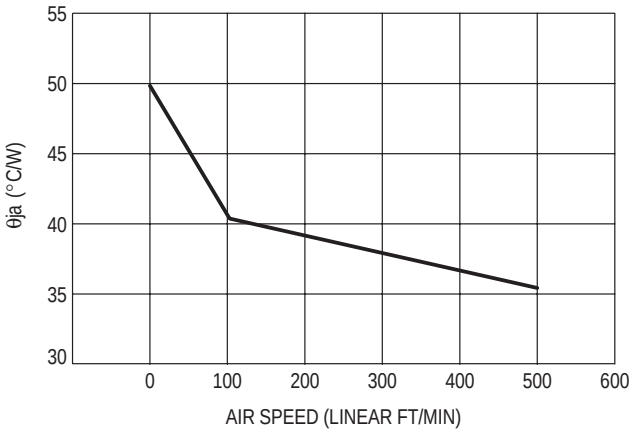
P_{DISS} = Device Power

and θja = Total Thermal Resistance and is composed the parallel combination of all the heat transfer paths from the package.

While Equation 2 is still only a first order approximation of the heat transfer paths of the MC34058/9, at least now it includes consideration for the most effective heat transfer path for the MC34058/9; the board to which the device is soldered. The modified equation also better serves to explain how external variables, namely the board and ambient temperatures, affect the thermal performance of the MC34058/9.

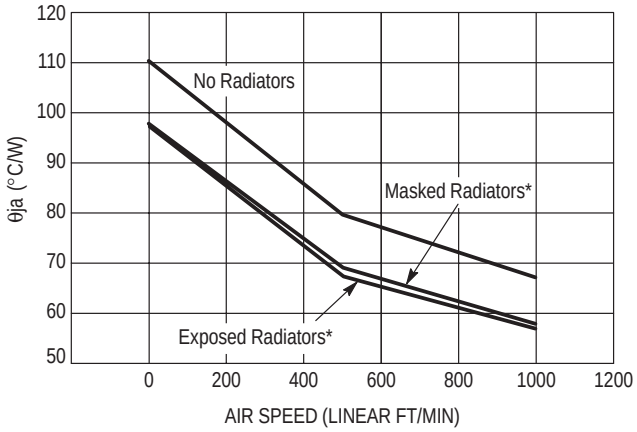
Methods of removing heat via the flag connected pins can be classified into two means; conduction and convection. Radiation is omitted as the contribution is small compared to the other means. Conduction is by far the best method to draw heat away from the MC34058/9 package. This is best accomplished by using a multilayer board with generous ground plane. In this case, the flag connected pins can be connected directly to the ground plane to maximize the heat transfer from the package. Figure 13 shows the results of thermal measurements of a board with an external ground plane (the actual ground area was approximately 6 1/4 in^2). The thermal leads are connected to the board ground plane per the recommended strategy.

Figure 13. Thermal Resistance (θja) for Board with Large External Ground Plane



θjc for the package on this board is 25 ±20% depending on the location of the package on the board.

Figure 14A. Thermal Resistance (θja) for Board Without Ground Plane



* Masked radiators were covered by a solder mask. Exposed radiators were bare copper.

Figure 14B. Layout Used for Thermal Resistance Measurements in Figure 14A

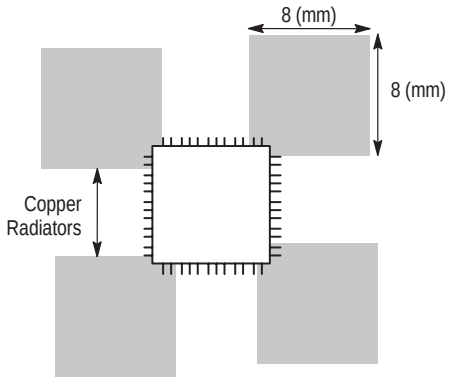


Figure 15. Placement of Thermal Vias to Enhance Heat Transfer to Ground Plane

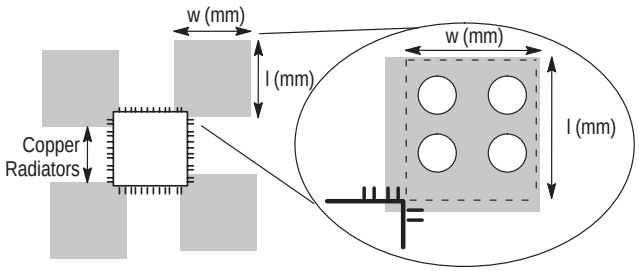


Figure 14A on the other hand shows the result of a single layer board without an internal ground plane. The graphs show that even though there are radiators of substantial area surrounding the package, substantial degredation of thermal performance is evident (Figure 14B shows the layout used for the measurements in Figure 14A). Comparing Figures 13 and 14A shows almost a 2:1 improvement for the strategy involving the external ground plane.

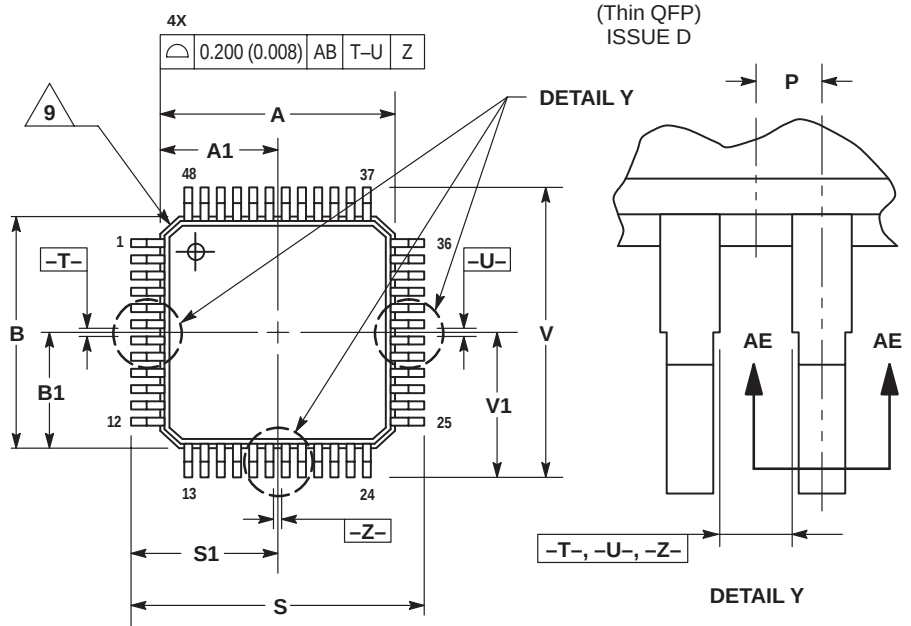
It is clear from Figures 13, 14A and Example 1, that if an application is to use all the device drivers, preparations to assure adequate thermal performance of the system must be taken.

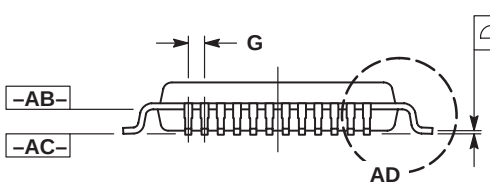
If an extensive external ground plane is unavailable, and only an internal ground plane is available, the thermal performance of the device can still be improved by providing thermal vias to connect the radiators to the internal ground plane. Figure 15 shows a proposed scheme for thermal vias (contact board manufactures for specifics about the thermal performance of their products and possible enhancements).

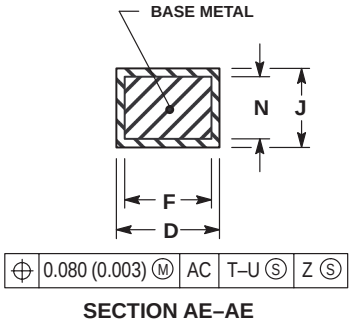
The thermal resistance for this structure on 1.0 oz. Copper connecting each of the four radiators to an internal ground plane and provide an estimated thermal resistance of approximately 5.0°C/W. The vias used in the estimate had 80 mil diameters, on 100 mil centers and a 1.0 mil copper thickness.

OUTLINE DIMENSIONS

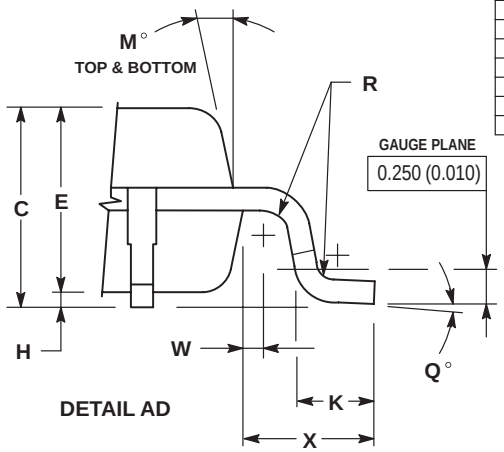
FTA SUFFIX
PLASTIC PACKAGE
CASE 932–02
(Thin QFP)
ISSUE D







SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1 °	5 °	1 °	5 °
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298