Numonyx® Axcell™ M29EW Datasheet

128-Mbit, 64-Mbit, 32-Mbit (x8 / x16, page read) 3 V supply flash memory

Features

- Supply voltage
  - — V_{CC} = 2.7 to 3.6 V for Program, Erase and Read
  - — V_{CCQ} = 1.65 to 3.6 V for I/O buffers
- Asynchronous Random/Page Read
  - — Page size: 8 words or 16 bytes
  - — Page access: 25 ns
  - — Random access: 60 ns (BGA); 70 ns (TSOP)
- Buffer Program
  - — 256-word program buffer
- Programming time
  - — 0.56µs per byte (1.8MB/s) typical when using 256-word buffer size in buffer program without V_{PPH}
  - — 0.31µs per byte (3.2MB/s) typical when using 256-word buffer size in buffer program with V_{PPH}
- Memory organization
  - — 128Mbit: 128 main blocks, 128 Kbytes each
  - — 64Mbit: 128 main blocks, 64 Kbytes each or eight 8-Kbyte boot blocks (top or bottom) and 127 main blocks, 64 Kbytes each
  - — 32Mbit: 64 main blocks, 64 Kbytes each or eight 8-Kbyte boot blocks (top or bottom) and 63 main blocks, 64 Kbytes each
- Program/Erase controller
  - — Embedded byte/word program algorithms
- Program/ Erase Suspend and Resume
  - — Read from any block during Program Suspend
  - — Read and Program another block during Erase Suspend
- Blank Check to verify an erased block
- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer
  - — Faster Buffered/Batch Programming
  - — Faster Block and Chip Erase
- V_{PP}/WP# pin protection
  - — V_{PPH} voltage on V_{PP} to accelerate programming performance
  - — Protects highest/lowest block (H/L uniform) or top/bottom two blocks (T/B boot)
- Software protection
  - — Volatile Protection
  - — Non-Volatile Protection
  - — Password Protection
  - — Password Access
- Extended Memory block
  - — 128-word/256-byte block for permanent, secure identification.
  - — Programmable and lockable by Numonyx factory or customer.
- Low power consumption
  - — Standby
- Minimum 100,000 Program/Erase cycles per block
- 65 nm technology
- Density and Packaging
  - — 56-Lead TSOP (128-Mbit, 64-Mbit)
  - — 48-Lead TSOP (64-Mbit, 32-Mbit)
  - — 64-Ball Fortified BGA (128-Mbit, 64-Mbit)
  - — 48-Ball BGA (64-Mbit, 32-Mbit)
- JESD47E compliant
- Green packages available
  - — RoHS Compliant
  - — Halogen Free

1 Description

The Numonyx® Axcell™ 128-Mbit, 64-Mbit and 32-Mbit M29EW flash memories, based on 65nm SBC (Single Bit per Cell) technology is the world's leading line of parallel NOR flash for embedded applications. They can be read, erased and reprogrammed; and these operations can be performed using a single low voltage (2.7 to 3.6 V) supply. Upon power-up, these memories default to their array read mode.

The main memory array is divided into 64-Kword/128-Kbyte blocks or 32-Kword/64-Kbyte blocks that can be erased independently so that valid data can be preserved while old data is purged. Program and Erase commands are written to the command interface of the memory. An on-chip Program/Erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error condition can be identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The M29EW supports Asynchronous Random Read and Page Read from all blocks of the memory array. It also features an internal program buffer which improves throughput by programming up to 256 words via one command sequence.

The M29EW contains a 128-word Extended Memory Block which overlaps addresses with array block 0. The user can program this additional space; then protect it to permanently secure its contents.

The device features different levels of hardware and software protection to secure blocks from unwanted modification (program or erase):

- Hardware protection:
  - V_{PP}/WP# provides hardware protection for the highest (M29EWH), lowest (M29EWL), top two (M29EWT) or bottom two (M29EWB) blocks of the main memory array.
- Software protection:
  - Volatile Protection
  - Non-Volatile Protection
  - Password Protection
  - Password Access

The M29EW is offered in TSOP56 (14 x 20 mm), TSOP48 (12 x 20 mm), Fortified BGA64 (11 x 13 mm, 1 mm pitch) and BGA48 (6 x 8 mm, 0.8 mm pitch) packages.

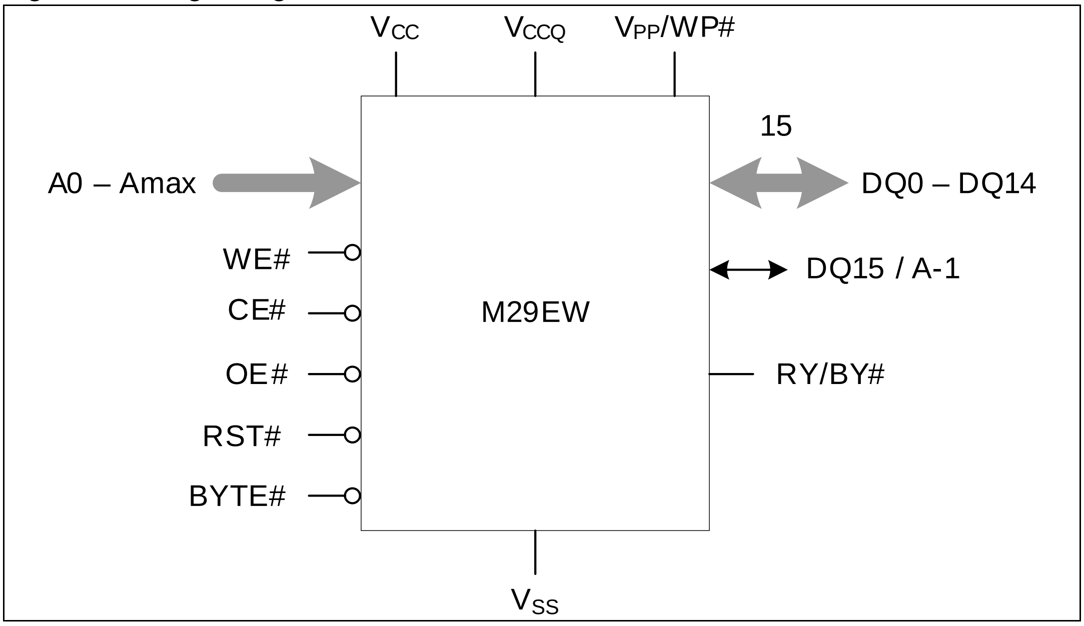
The memories are delivered with all bits erased (set to ‘1’).

Table 1. Signal descriptions

Name	Description	Direction
A0-Amax	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15/A–1	Data input/output or address input	I/O or input
CE#	Chip Enable	Input
OE#	Output Enable	Input
WE#	Write Enable	Input
RST#	Reset	Input
RY/BY#	Ready/Busy output	Output
BYTE#	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
V_{PP}/WP#(1)	V_{PP}/Write Protect	Input
V_{SS}	Ground	-
NC	Not connected	-

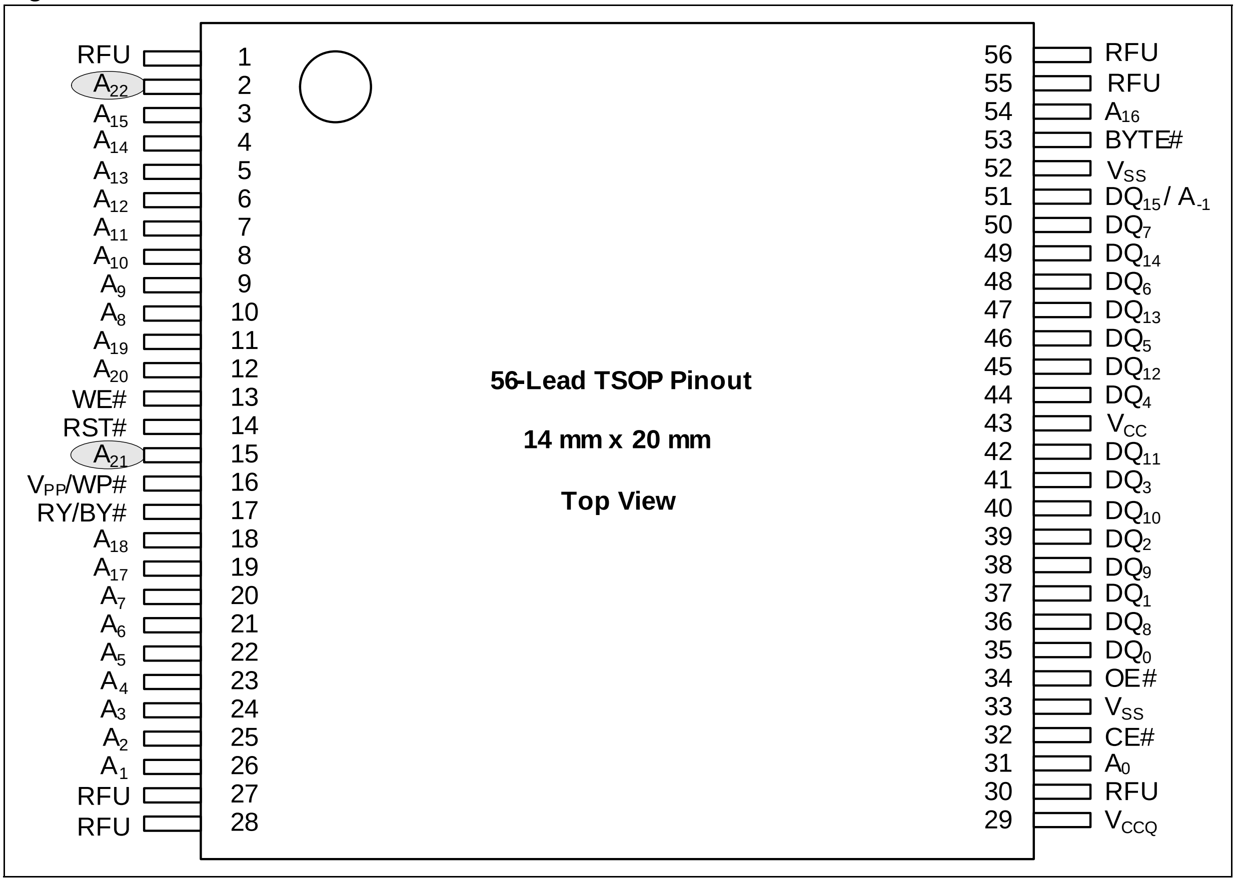
1. V_{PP}/WP# may be left unconnected as it is internally connected to a pull-up resistor, which enables Program/Erase operations.

Figure 1. Logic diagram



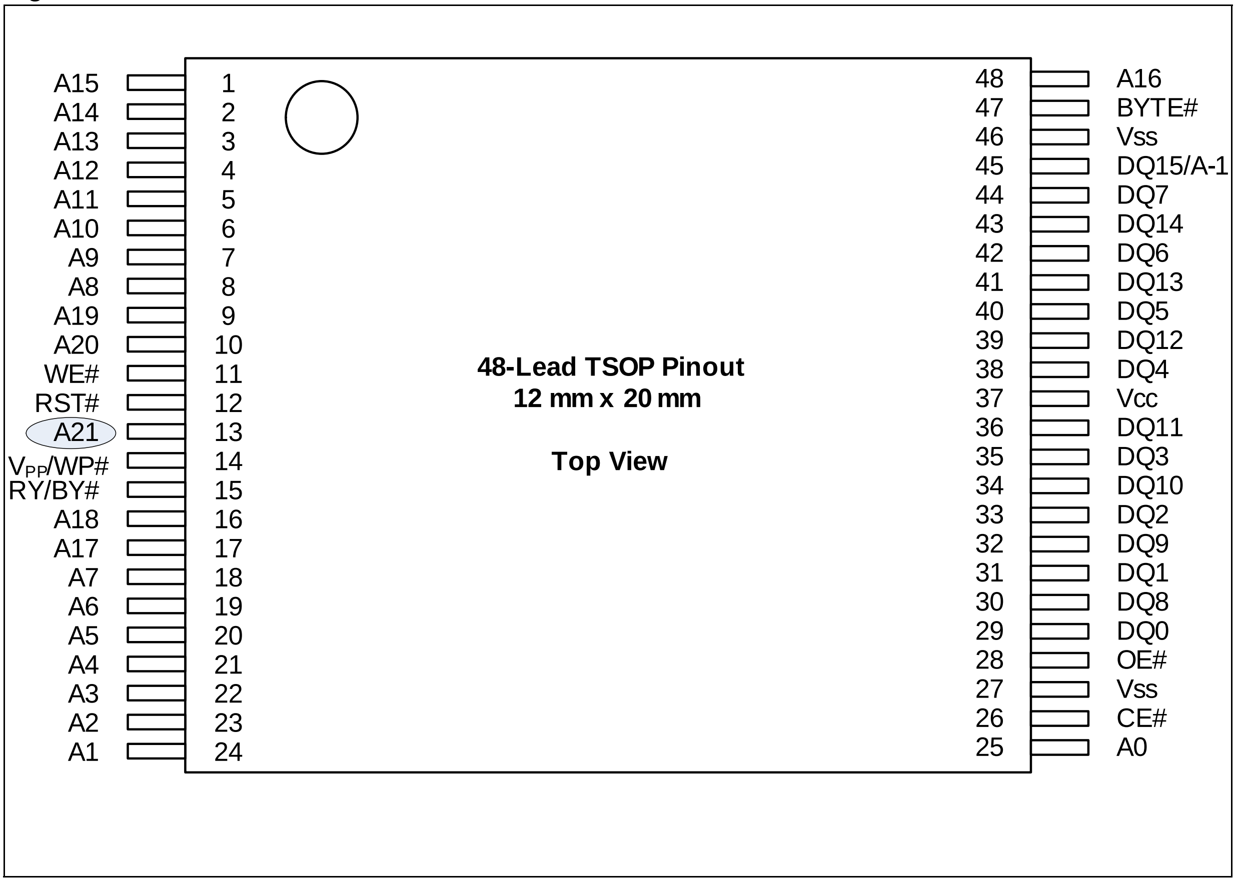
1. A22, A21 and A20 are maximum address pins for 128-Mbit, 64-Mbit and 32-Mbit density respectively.

Figure 2. 56-Lead TSOP connections



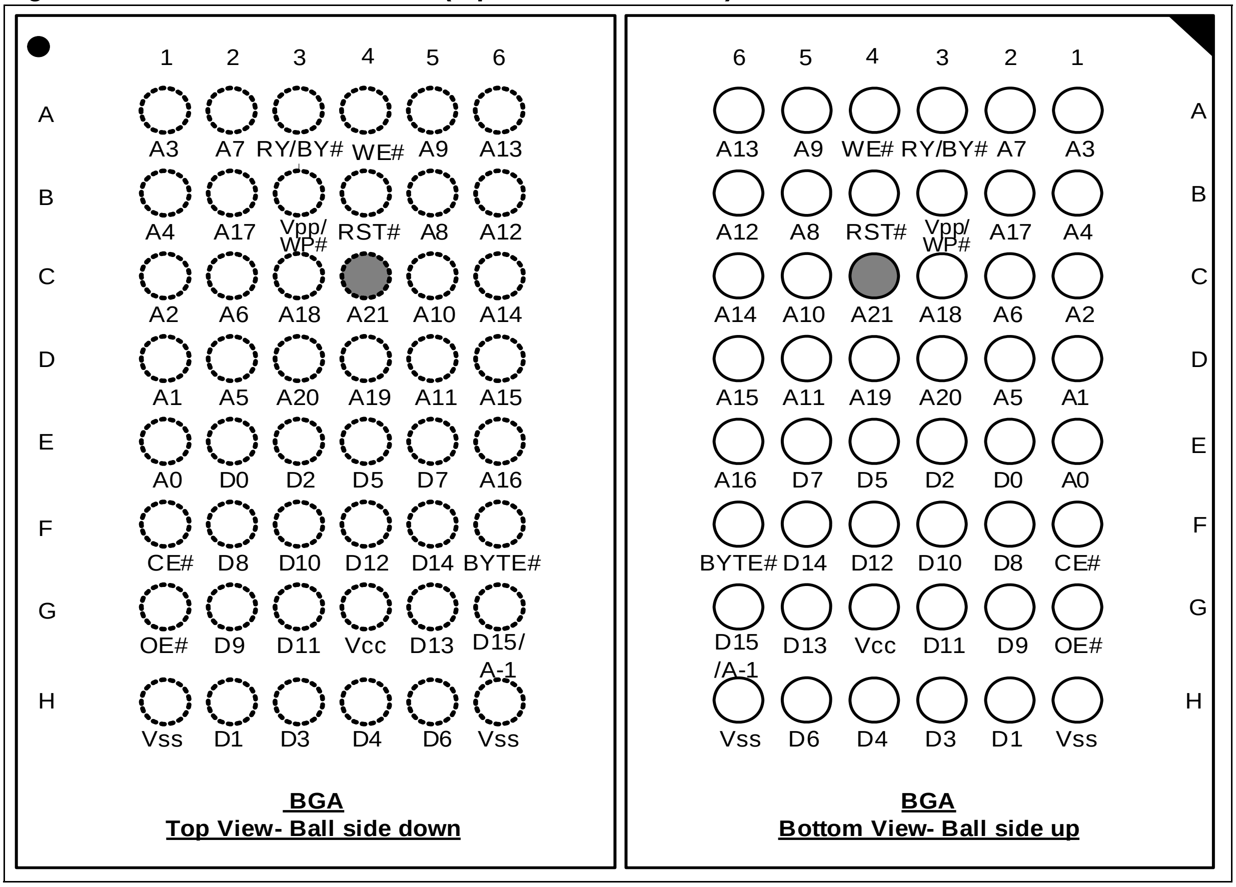
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density and above; otherwise, it is RFU.
3. A22 is valid for 128-Mbit density; otherwise, it is RFU.
4. RFU stands for Reserved for Future Use.

Figure 3. 48-Lead TSOP connections



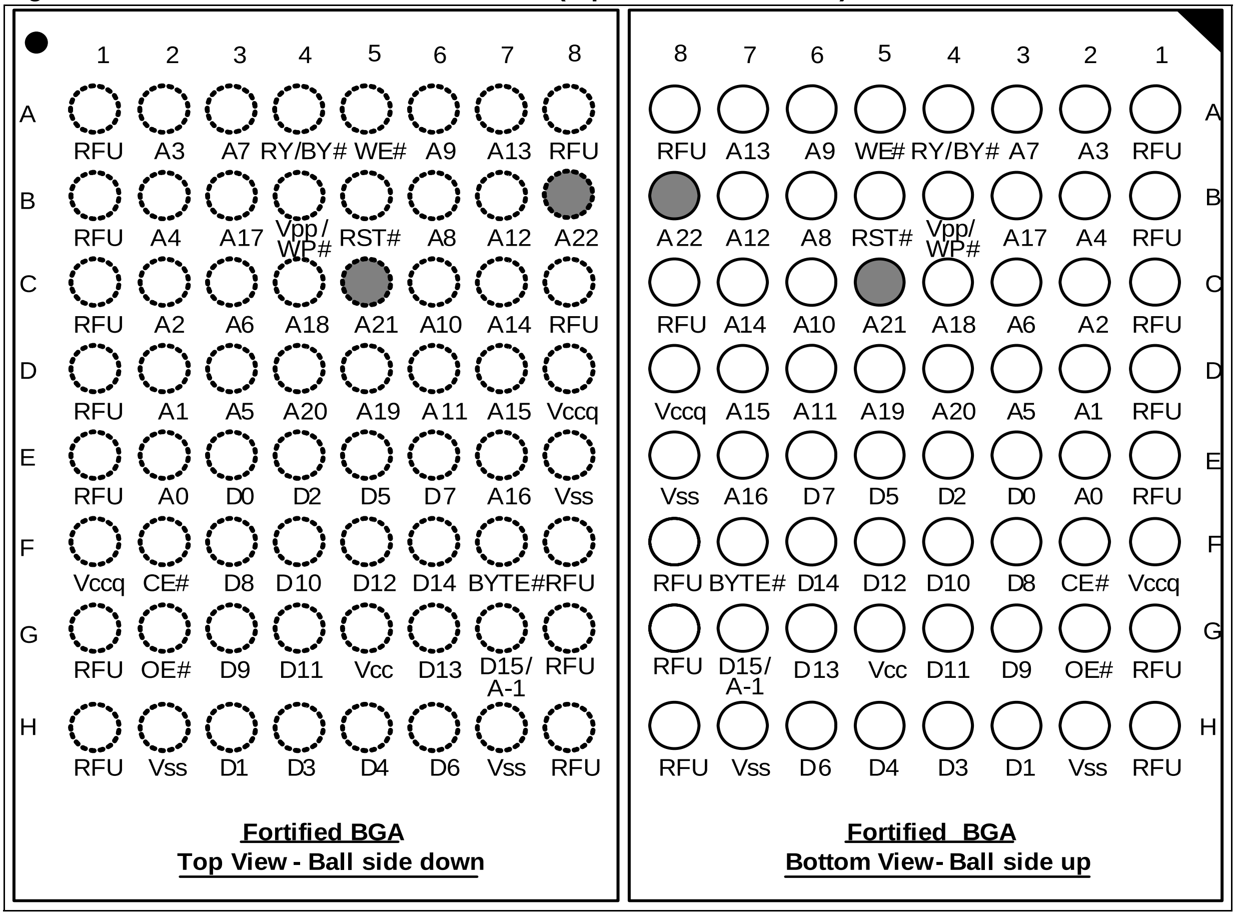
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density; otherwise, it is RFU.
3. RFU stands for Reserved for Future Use.

Figure 4. 48B BGA connections (top and bottom views)



1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density; otherwise, it is RFU.
3. RFU stands for Reserved for Future Use.

Figure 5. 64B Fortified BGA connections (top and bottom views)



1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64-Mbit density and above; otherwise, it is RFU.
3. A22 is valid for 128-Mbit density; otherwise, it is RFU.
4. RFU stands for Reserved for Future Use.

Figure 6. 128-Mbit Block addresses

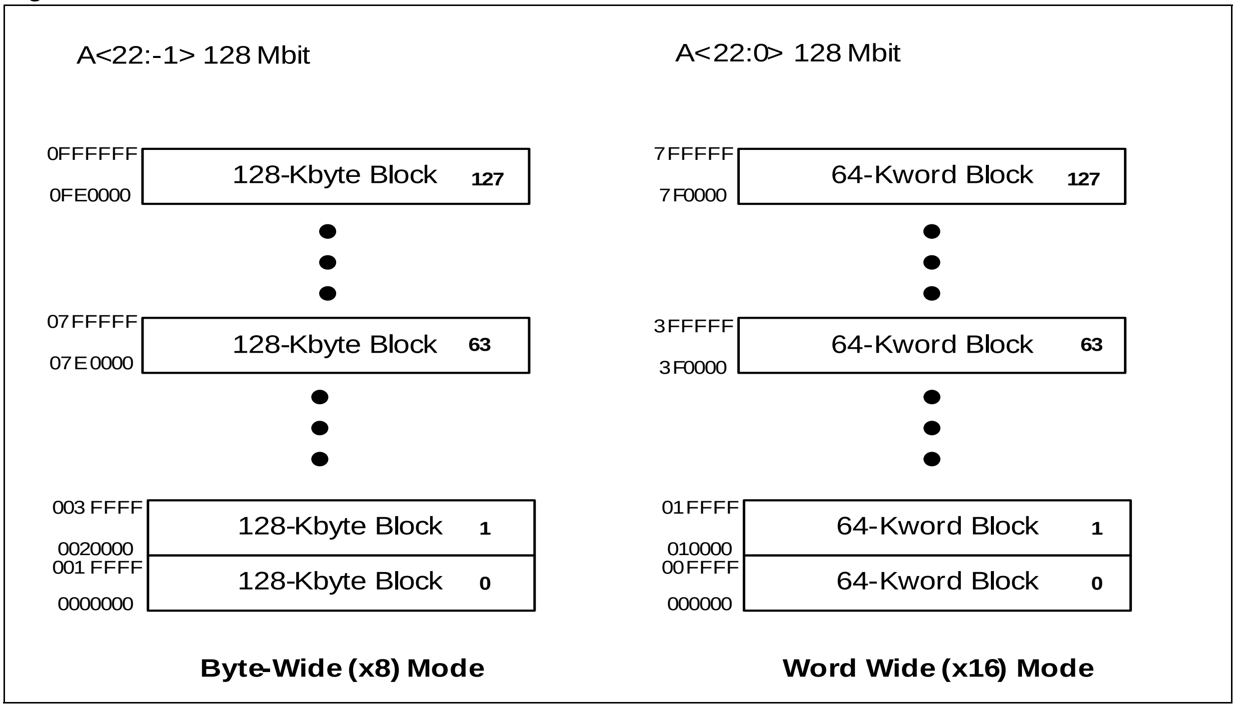


Figure 7. 64-Mbit and 32-Mbit Uniform Block addresses

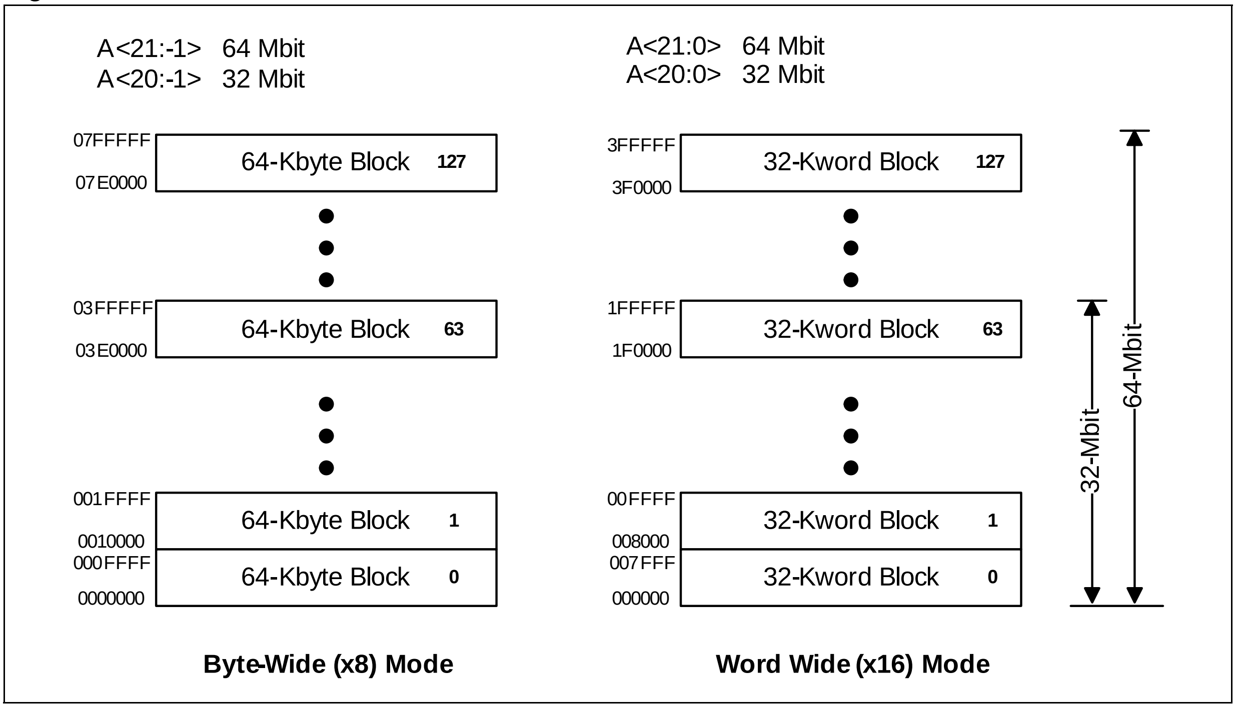
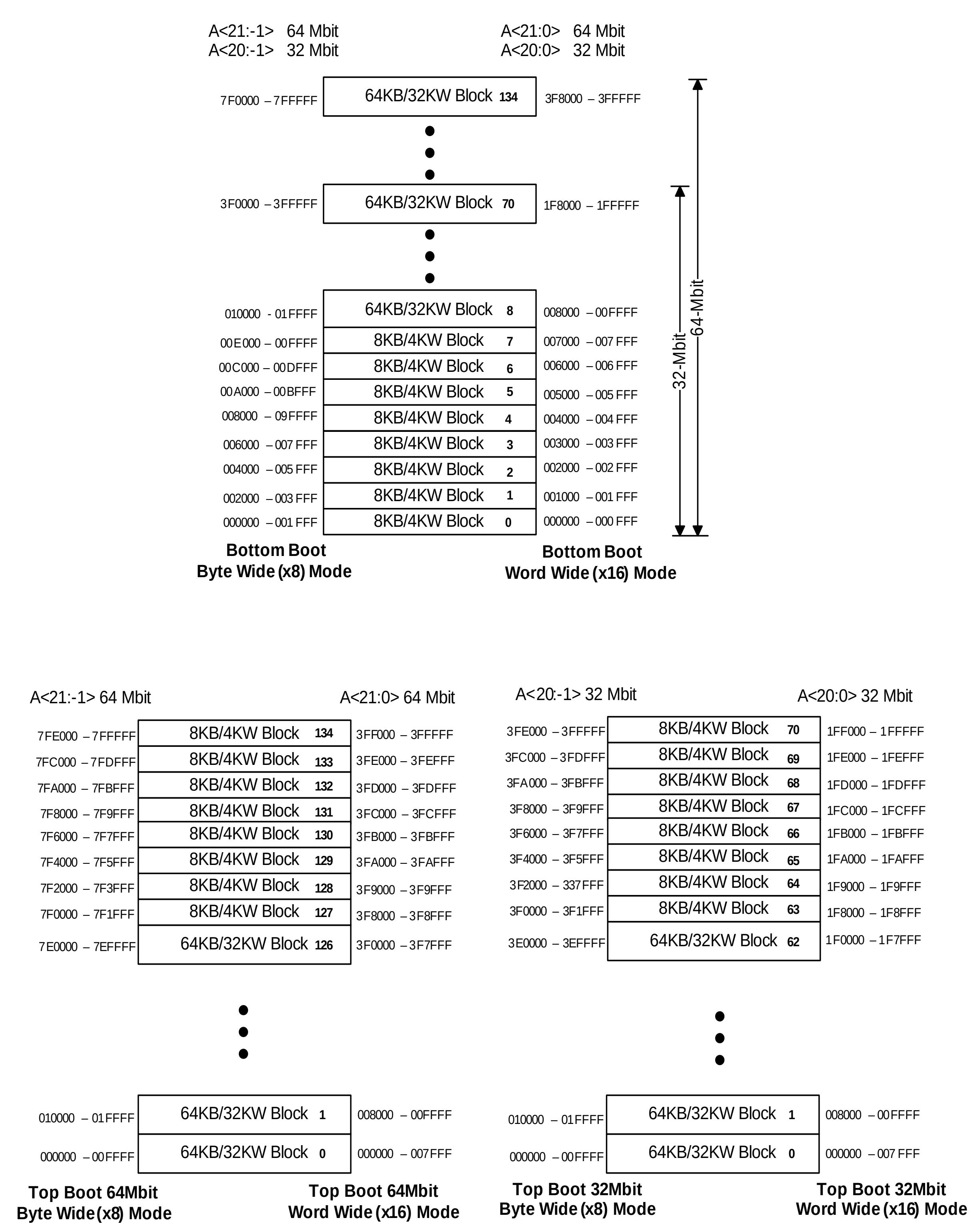


Figure 8. 64-Mbit and 32-Mbit Boot Block addresses



2 Signal Descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal descriptions*, for a brief overview of device signals.

2.1 Address inputs (A0-A22)

The Address inputs select the cells in the memory array, CFI space to access during Bus Read operations. During Bus Write operations they direct the commands sent to the command interface of the Program/Erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

During Bus Read operations, the data lines output the data stored at the selected address or register. During Bus Write operations, the data lines are used to input data or commands.

2.3 Data inputs/outputs (DQ8-DQ14)

During Bus Read operations, the data lines output the data stored at the selected address when BYTE# is High, V_{IH}. When BYTE# is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. Ignore these bits when reading the Status Register .

2.4 Data input/output or address input (DQ15/A–1)

When the device operates in x16 bus mode, this pin behaves as a Data input/output pin, together with DQ8-DQ14. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Throughout this document, when both references occur, consider the DQ15 function adding to the other data lines when in X16 mode and the A-1 function adding to the others addresses when in X8 mode, except when explicitly stated otherwise.

2.5 Chip Enable (CE#)

The Chip Enable pin, CE#, activates the memory when it's low, V_{IL}, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, the memory is deselected and power is reduced to standby level.

2.6 Output Enable (OE#)

The Output Enable pin, OE#, controls the Bus Read operation of the memory.

2.7 Write Enable (WE#)

The Write Enable pin, WE#, controls the Bus Write operation of the memory's command interface.

2.8 V_{PP}/Write Protect (V_{PP}/WP#)

The V_{PP}/WP# pin provides three functions: write protect function, programming acceleration, and the unlock bypass mode entry.

When V_{PP}/WP# is low, the write protect function provides hardware protection for the highest M29EWH block, the lowest M29EWL block, the top two M29EWT blocks, or the bottom two M29EW blocks (see *Section 1: Description*). Program and Erase operations on this block are ignored while V_{PP}/Write Protect is Low.

When V_{PP}/WP# pin is High, V_{IH}, the memory reverts to the previous protection status of the highest, lowest, top two or bottom two blocks . Program and Erase operations can now modify the data in this block unless the block is protected using other block protection method.

When V_{PP}/WP# pin is raised to V_{PPH} in read mode, the memory automatically enters the Unlock Bypass mode (see *Section 6.2.9*).

When V_{PP}/WP# returns to V_{IH} or V_{IL} normal operation resumes. See the description of the Unlock Bypass command in the command interface section.

When V_{PP}/WP# pin is raised to V_{PPH} during programming, it will accelerate the programming speed.

The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 31: Accelerated program timing waveforms*).

Never raise V_{PP}/WP# to V_{PPH} from any mode except in read mode or during programming, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/Write Protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during programming (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 22: DC characteristics*).

The V_{PP}/WP# pin may be left unconnected because it features an internal pull-up resistor.

Refer to *Table 2* for a summary of V_{PP}/WP# functions.

Table 2. V_{PP}/WP# functions

V_{PP}/WP#	Function
V_{IL}	Highest block protected or lowest block protected.
V_{IH}	Highest and lowest block unprotected unless software protection is activated (see *Section 4: Hardware Protection*).
V_{PPH}	Unlock bypass mode.
V_{PPH}	Programming speed acceleration.

2.9 Reset (RST#)

The Reset pin can be used to apply a Hardware Reset to the memory. A hardware reset is achieved by holding Reset Low, V_{IL}, for at least t_{PLPX}. After Reset goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL} (or t_{PHGL} or t_{RHGL}), whichever occurs last. See *Section 2.10: Ready/Busy output (RY/BY#)*, *Table 26: Reset AC characteristics*, *Figure 29* and *Figure 30* for more details.

2.10 Ready/Busy output (RY/BY#)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations Ready/Busy is Low, V_{OL} (see *Table 17: Status Register bits*). Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See *Table 26: Reset AC characteristics*, *Figure 29* and *Figure 30*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A low value will then indicate that one, or more, of the memories is busy. The 10K ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.

2.11 Byte/Word organization select (BYTE#)

The BYTE# pin is used to switch between the x8 and x16 Bus modes of the memory. When Byte/Word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (Read, Program and Erase). The command interface is disabled when V_{CC} is $\leq$ Lockout voltage, V_{LKO}. This prevents Bus Write operations from accidentally corrupting the data during power-up, power-down and power surges. The operation will abort, and the memory contents being altered will thus be invalid, if the V_{CC} drops below V_{LKO} while the Program/Erase controller is running.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 22: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins; it enables the I/Os to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins; both of which must be connected to the system ground.

3 Bus Operations

There are four standard bus operations that control the device. These are Bus Read (Random and Page modes), Bus Write, Output Disable, Standby.

See *Table 3: Bus operations, 8-bit mode* and *Table 4: Bus operations, 16-bit mode* for a summary. Typical glitches of less than 3ns on Chip Enable, Write Enable, and Reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus Read

Bus Read operations read from the memory cells, registers or CFI space. To speed up the read operation the memory array can be read in Page mode where data is internally read and stored in a page buffer. The page has a size of 8 words (or 16 bytes) and is addressed by the address inputs A2-A0 in x16 bus mode and A2-A0 plus DQ15/A–1 in x8 bus mode. The Extended Memory Blocks and CFI area do not support Page Read mode.

A valid Bus Read operation involves setting the desired address on the Address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data inputs/outputs will output the value, see *Figure 20: Random Read AC waveforms (8-bit mode)*, *Figure 23: Page Read AC waveforms (16-bit mode)*, and *Table 23: Read AC characteristics (Sheet of 2)*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write to the command interface. A valid Bus Write operation begins by setting the desired address on the Address inputs. The Address inputs are latched by the command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data inputs/outputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the entire Bus Write operation. See *Figure 24*, and *Figure 25*, Write AC waveforms, and *Table 24* and *Table 25*, Write AC characteristics, for details of the timing requirements.

3.3 Output Disable

The Data inputs/outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

Driving Chip Enable High in Read mode, causes the memory to enter Standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the Supply current to the Standby Supply current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.3$ V. For the Standby current level see *Table 22: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase Supply current, I_{CC3}, for Program or Erase operations until the operation completes.

3.5 Reset

During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when RST# is at V_{IL}. The power consumption is reduced to the standby level, independently from the Chip Enable, Output Enable or Write Enable inputs.

3.6 Auto Select mode

The Auto Select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the Extended Memory Block, and apply/remove Block protection. For example, this mode can be used by programming equipment to automatically match a device and the application code to be programmed.

At power-up, the device is in Read mode, and can then be put in Auto Select mode by issuing the Auto Select command (see *Section 6.1.2*).

The device cannot enter Auto Select mode when a program or erase operation is in progress (RY/BY# Low). However, Auto Select mode can be entered if the program or erase operation has been suspended by issuing a Program Suspend or Erase Suspend command (see *Section 6.1.7*).

The Auto Select mode is exited by performing a reset. The device is returned to Read mode, except if the Auto Select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the Erase or Program Suspend mode.

3.6.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 5: Read electronic signature - auto select mode - programmer method (8-bit mode)* and *Table 6: Read electronic signature - auto select mode - programmer method (16-bit mode)*.

These codes can also be accessed by issuing an Auto Select command (see *Section 6.1.2: Auto Select command*).

3.6.2 Verify Extended Memory Block protection indicator

The Extended Memory Block is either Numonyx pre-locked or customer-lockable.

The protection status of the Extended Memory Block (pre-locked or customer-lockable) can be accessed by reading the Extended Memory Block protection indicator. It can be read in Auto Select mode using either the programmer (see *Table 7* and *Table 8*) or the in-system method (see *Table 9* and *Table 10*).

The protection status of the Extended Memory Block is then output on bit DQ7 of the Data input/outputs (see *Table 3* and *Table 4*, Bus operations in 8-bit and 16-bit mode).

3.6.3 Verify block protection status

The protection status of a block can be determined by performing a read operation with control signals and addresses set as shown in *Table 7* and *Table 8*.

If the block is protected, then 01h (in x 8 mode) is output on Data input/outputs DQ0-DQ7, otherwise 00h is output.

3.6.4 Hardware Block Protect

Hardware protection of certain memory blocks is supported via the V_{PP}/WP# write protection function. When V_{PP}/WP# is V_{IL}, the highest (M29EWH), lowest (M29EWL), top two (M29EWT), or bottom two (M29EWB) blocks are protected ; these, and other blocks, may also be enabled with software protection.

Table 3. Bus operations, 8-bit mode

Operation(1)	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs	Data Inputs/Outputs	
						A[max:-1]	DQ[14:8]	DQ[7:0]
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Byte address	Hi-Z	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}(2)	Command address	Hi-Z	Data input(3)
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If WP# is Low, V_{IL}, the highest, lowest, top two or bottom two blocks (depending on line item) remain protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 4. Bus operations, 16-bit mode

Operation(1)	CE#	OE#	WE#	RST#	V_{PP}/WP#	Address Inputs	Data Inputs/Outputs
						A[max:0]	DQ[15:0]
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Word address	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}(2)	Command address	Data input(3)
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	X	Hi-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If WP# is Low, V_{IL}, the highest, lowest, top two or bottom two blocks (depending on line item) remain protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Read electronic signature - auto select mode - programmer method (8-bit mode)

Read cycle(1)	CE#	OE#	WE#	Address inputs							Data inputs/outputs	
				Amax-A11	A10-A4	A3	A2	A1	A0	A-1	DQ[14:8]	DQ[7:0]
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	89h
Device code (cycle 1)						V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh
Device code (cycle 2)						V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	21h (128-Mbit)
												10h (64-Mbit, boot)
												0Ch (64-Mbit, uniform)
												1Ah (32-Mbit, boot)
												1Dh (32-Mbit, uniform)
Device code (cycle 3)						V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	01h (128- and 64-Mbit uniform, 64- and 32-Mbit top)
												00h (64- and 32-Mbit bottom, 32-Mbit uniform)

1. X = V_{IL} or V_{IH}.

Table 6. Read electronic signature - auto select mode - programmer method (16-bit mode)

Read cycle(1)	CE#	OE#	WE#	Address inputs						Data inputs/outputs
				Amax-A11	A10-A4	A3	A2	A1	A0	DQ[15:0]
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0089h
Device code (cycle 1)						V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Device code (cycle 2)						V_{IH}	V_{IH}	V_{IH}	V_{IL}	2221h (128-Mbit)
										2210h (64-Mbit, boot)
										220Ch (64-Mbit, uniform)
										221Ah (32-Mbit, boot)
										221Dh (32-Mbit, uniform)
Device code (cycle 3)						V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h (128- and 64-Mbit uniform, 64- and 32-Mbit top)
										2200h (64- and 32-Mbit bottom, 32-Mbit uniform)

1. X = V_{IL} or V_{IH}.

Table 7. Block protection - auto select mode - programmer method (8-bit mode)

<table>
<tr><th colspan="2" rowspan="2">Operation(1)</th><th rowspan="2">CE#</th><th rowspan="2">OE#</th><th rowspan="2">WE#</th><th colspan="6">Address inputs</th><th colspan="2">Data inputs/outputs</th></tr>
<tr><th>Amax-A15</th><th>A14-A11</th><th>A10-A2</th><th>A1</th><th>A0</th><th>A-1</th><th>DQ[14:8]</th><th>DQ[7:0]</th></tr>
<tr><td rowspan="4">Verify Extended Memory Block protection indicator (bit DQ7)</td><td>M29EWL 128-Mbit</td><td rowspan="5">V_{IL}</td><td rowspan="5">V_{IL}</td><td rowspan="5">V_{IH}</td><td rowspan="4">X</td><td rowspan="5">X</td><td rowspan="5">V_{IL}</td><td rowspan="5">V_{IH}</td><td rowspan="4">V_{IH}</td><td rowspan="5">X</td><td rowspan="5">X</td><td>89h (Numonyx pre-locked)
09h (customer-lockable)</td></tr>
<tr><td>M29EWH 128-Mbit</td><td>99h (Numonyx pre-locked)
19h (customer-lockable)</td></tr>
<tr><td>M29EWL/B 64-Mbit 32-Mbit</td><td>8Ah (Numonyx pre-locked)
0Ah (customer-lockable)</td></tr>
<tr><td>M29EWH/T 64-Mbit 32-Mbit</td><td>9Ah (Numonyx pre-locked)
1Ah (customer-lockable)</td></tr>
<tr><td colspan="2">Verify block protection status</td><td>BBA(2)</td><td>V_{IL}</td><td>01h (protected)
00h (unprotected)</td></tr>
</table>

1. X = V_{IL} or V_{IH}.
2. BBA = Block Base Address. For 128-Mbit, BBA should be Amax-A16 and A15 is X.

Table 8. Block protection - auto select mode - programmer method (16-bit mode)

<table>
<tr><th colspan="2" rowspan="2">Operation(1)</th><th rowspan="2">CE#</th><th rowspan="2">OE#</th><th rowspan="2">WE#</th><th colspan="5">Address inputs</th><th>Data inputs/outputs</th></tr>
<tr><th>Amax-A15</th><th>A14-A11</th><th>A10-A2</th><th>A1</th><th>A0</th><th>DQ[15:0]</th></tr>
<tr><td rowspan="4">Verify Extended Memory Block indicator (bit DQ7)</td><td>M29EWL 128-Mbit</td><td rowspan="5">V_{IL}</td><td rowspan="5">V_{IL}</td><td rowspan="5">V_{IH}</td><td rowspan="4">X</td><td rowspan="5">X</td><td rowspan="5">V_{IL}</td><td rowspan="5">V_{IH}</td><td rowspan="4">V_{IH}</td><td>0089h (Numonyx pre-locked)
0009h (customer-lockable)</td></tr>
<tr><td>M29EWH 128-Mbit</td><td>0099h (Numonyx pre-locked)
0019h (customer-lockable)</td></tr>
<tr><td>M29EWL/B 64-Mbit 32-Mbit</td><td>008Ah (Numonyx pre-locked)
000Ah (customer-lockable)</td></tr>
<tr><td>M29EWH/T 64-Mbit 32-Mbit</td><td>009Ah (Numonyx pre-locked)
001Ah (customer-lockable)</td></tr>
<tr><td colspan="2">Verify block protection status</td><td>BBA(2)</td><td>V_{IL}</td><td>0001h (protected)
0000h (unprotected)</td></tr>
</table>

1. X = V_{IL} or V_{IH}. BBA = Block Base Address.
2. BBA = Block Base Address. For 128-Mbit, BBA should be Amax-A16 and A15 is X.

4 Hardware Protection

The M29EW features a V_{PP}/WP# pin that protects the highest, lowest, top two or bottom two blocks. Refer to *Section 2: Signal Descriptions* for a detailed description of the signal.

5 Software Protection

The M29EW has four different software protection modes:

- Volatile Protection
- Non-Volatile Protection
- Password Protection
- Password Access

On first use all parts default to operate in non-volatile Protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable Non-Volatile Protection Mode Lock bit, or the Password Protection Mode Lock bit of the Lock Register (see *Section 7.1: Lock Register*). Programming the Non-Volatile Protection Mode Lock bit or the Password Protection Mode Lock bit, to '0' will permanently activate the Non-volatile or the Password Protection mode, respectively. These two bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The Non-volatile and Password Protection modes both provide non-volatile Protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile Protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 5* and *Table 6*) or by issuing an Auto Select command (see *Table 16: Block Protection Status*).

For the lowest and highest blocks, an even higher level of block protection can be achieved by locking the blocks using the non-volatile Protection and then by holding the V_{PP}/WP# pin Low.

Password Access is a security enhancement offered on the M29EW device. This feature protects information stored in the main-array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password Access may be combined with Non-Volatile and/or Volatile Protection to create a multi-tiered solution.

Please contact your Numonyx Sales representative for further details concerning Password Access feature.

5.1 Volatile Protection mode

The volatile Protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile Protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile Protection bits, NVPBs, cleared (erased to ‘1’) (see *Section 5.2: Non-Volatile Protection mode* and *Section 6.3.5: Non-Volatile Protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to ‘0’) or cleared (erased to ‘1’), thus placing associated blocks in the protected or unprotected state respectively. The VPBs can be set (programmed to ‘0’) or cleared (erased to ‘1’) as often as needed.

When the parts are first shipped, or after a power-up or hardware reset, the VPBs default to be cleared.

Refer to *Section 6.3.7* for a description of the volatile Protection mode command set.

5.2 Non-Volatile Protection mode

5.2.1 Non-Volatile Protection bits

A non-volatile Protection bit (NVPB) is assigned to each block.

When a NVPB is set to ‘0’, the associated block is protected, preventing any program or erase operations in this block.

The NVPB bits can be set individually by issuing a NVPB Program command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The NVPBs cannot be cleared individually, they can only be all cleared at the same time by issuing a Clear all Non-Volatile Protection bits command.

The NVPBs can be protected all at a time by setting a volatile bit, the NVPB Lock bit (see *Section 5.2.2: Non-Volatile Protection Bit Lock bit*).

If one of the non-volatile protected blocks needs to be unprotected (corresponding NVPB set to ‘1’), a few more steps are required:

1. First, the NVPB Lock bit must be ‘1’ by either putting the device through a power cycle, or hardware reset.
2. The NVPBs can then be changed to reflect the desired settings.
3. The NVPB Lock bit must be set to ‘0’ once again to lock the NVPBs by associated command. The device operates normally again.

Note: 1 To achieve the best protection, it is recommended to execute the NVPB Lock Bit Program command early in the boot code and to protect the boot code by holding V_{PP}/WP# Low, V_{IL}.

2 The NVPBs and VPBs have the same function when V_{PP}/WP# pin is High, V_{IH}, as they do when V_{PP} /WP# pin is at the voltage for program acceleration (V_{PPH}).

Refer to *Table 16: Block Protection Status* and *Figure 9: Software protection scheme* for details on the block protection mechanism, and to *Section 6.3.5* for a description of the Non-Volatile Protection mode command set.

5.2.2 Non-Volatile Protection Bit Lock bit

The Non-Volatile Protection Bit Lock bit (NVPB Lock bit) is a global volatile bit for all NVPBs.

When set (programmed to '0'), it prevents changing the state of the NVPBs. When reset to '1', the NVPBs can be set and reset using the NVPB Program command and Clear all NVPBs command, respectively.

There is only one NVPB Lock bit per device.

Refer to *Section 6.3.6* for a description of the NVPB Lock bit command set.

Note: 1 No software command unlocks this bit unless the device is in password protection mode; in standard non-volatile Protection mode, it can be cleared only by taking the device through a hardware reset or a power-up.

2 The NVPB Lock bit must be set (programmed to '0') only after all NVPBs are configured to the desired settings.

5.3 Password Protection mode

The password protection mode provides an even higher level of security than the Non-Volatile Protection mode by requiring a 64-bit password for unlocking the device NVPB Lock bit.

In addition to this password requirement, the NVPB Lock bit is set '0' after power-up and reset to maintain the device in password protection mode. Successful execution of the Password Unlock command by entering the correct password clears the NVPB Lock bit, allowing for block NVPBs to be modified.

If the password provided is incorrect, the NVPB Lock bit remains locked and the state of the NVPBs cannot be modified.

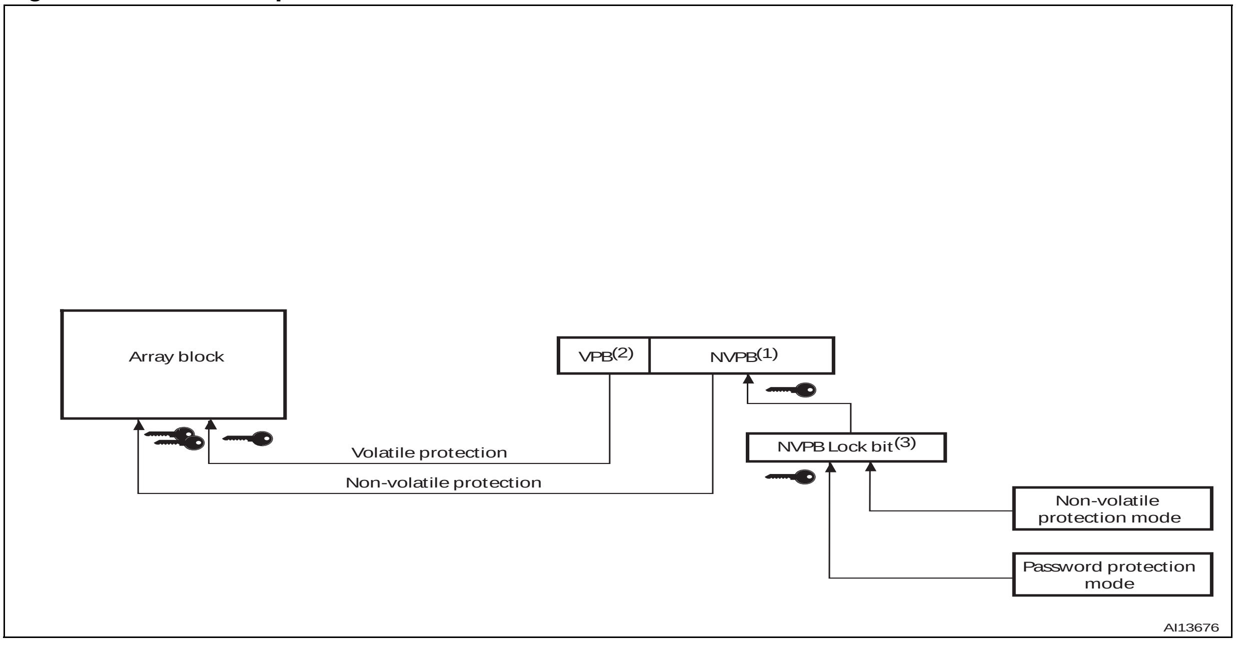
To place the device in password protection mode, the following steps are required:

1. Prior to activating the password protection mode, it is necessary to set a 64-bit password and to verify it (see *Password Program command* and *Password Read command*). Password verification is only allowed before the password protection mode is activated.
2. The password protection mode is then activated by programming the Password Protection Mode Lock bit to '0'. This operation is not reversible and once the bit is programmed it cannot be erased, the device permanently remains in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 16: Block Protection Status* and *Figure 9: Software protection scheme* for details on the block protection scheme.

Refer to *Section 6.3.4* for a description of the Password Protection mode command set.

Note: There is no means to verify the password after Password Protection mode is enabled. If the password is lost after enabling the Password Protection mode, there is no way to clear the NVPB Lock bit.

Figure 9. Software protection scheme



1. NVPBs default to ‘1’ (block unprotected) when shipped from Numonyx. A block is protected or unprotected when its NVPB is set to ‘0’ and ‘1’, respectively. NVPBs are programmed individually and cleared collectively.
2. VPB default status depends on ordering option. A block is protected or unprotected when its VPB is set to ‘0’ and ‘1’, respectively. VPBs can be programmed and cleared individually.
3. The NVPB Lock bit is volatile and default to ‘1’ (NVPB bits unlocked) after power-up or hardware reset. NVPB bits are locked by setting the NVPB Lock bit to ‘0’. Once programmed to ‘0’, the NVPB Lock bit can only be reset to ‘1’ by taking the device through a power-up or hardware reset.

6 Command Interface

All Bus Write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode.

6.1 Standard commands

See either *Table 9*, or *Table 10*, depending on the configuration that is being used, for a summary of the standard commands.

6.1.1 Read/Reset command

The device enters read mode of main array memory after a reset or power-up sequence.

The Read/Reset command returns the memory to Read mode. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to Read mode. If the Read/Reset command is issued during the time-out of a Block erase operation, the memory will take up to 10 µs to abort. During the abort period no valid data can be read from the memory.

The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

6.1.2 Auto Select command

The Auto Select command puts the device in Auto Select mode, once in Auto Select mode, the system can read the manufacturer code, the device code, the protection status of each block (Block Protection status) and the Extended Memory Block protection indicator.

Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued Bus Read operations to specific addresses output the manufacturer code, the device code, the Extended Memory Block protection indicator and a block protection status (see *Table 9* and *Table 10* in conjunction with *Table 5*, *Table 6*, *Table 7*, and *Table 8*). The memory remains in Auto Select mode until a Read/Reset or CFI Query command is issued.

6.1.3 Read CFI Query command

The memory contains an information area, named CFI data structure, which contains a description of various electrical and timing parameters, density information and functions supported by the memory. See *Appendix B*, *Table 36*, *Table 37*, *Table 38, Table 39* and *Table 40* for details on the information contained in the Common Flash Interface (CFI) memory area.

The Read CFI Query command is used to put the memory in Read CFI Query mode. Once in Read CFI Query mode, Bus Read operations to the memory will output data from the Common Flash Interface (CFI) memory area. One Bus Write cycle is required to issue the Read CFI Query command. This command is valid only when the device is in the Read Array or Auto Select mode.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Auto Select mode). A second Read/Reset command is required to put the device in Read Array mode from Auto Select mode.

6.1.4 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase command and start the Program/Erase controller.

If some block are protected, then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical Chip Erase times are given in *Table 28*. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data inputs/outputs. See *Section 7.2: Status Register* for more details.

After the Chip Erase operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Chip Erase command sets all of the bits in unprotected blocks of the memory to ‘1’. All previous data is lost.

The Chip Erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the entire chip.

6.1.5 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to ‘1’. All previous data in the selected blocks is lost.

Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. After the command sequence is written, a Block Erase time-out occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Once the Program/Erase controller has started, it is not possible to select any more blocks. Each additional block must therefore be selected within the time-out period of the last block. The time-out timer restarts when an additional block is selected. After the sixth Bus Write operation, a Bus Read operation outputs the Status Register. See *Figure 24: Write Enable Controlled Program waveforms (8-bit mode)* and *Figure 25: Write Enable Controlled Program waveforms (16-bit mode)* for details on how to identify if the Program/Erase controller has started the Block Erase operation.

After the Block Erase operation has completed, the memory returns to the Read mode, unless an error has occurred. When an error occurs, Bus Read operations will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory ignores all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the time-out period. Typical Block Erase time and Block Erase time-out are given in *Table 28*.

The Block Erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the blocks aborted.

6.1.6 Blank Check command

The Blank Check operation determines whether a specified block is blank (i.e. completely erased). Without Blank Check, Block Erase would be the only other way to ensure a block is completely erased. Blank Check can be used to determine whether or not a prior erase operation was successful; this includes erase operations that may have been interrupted by power-loss. The Blank Check operation checks for cells that are programmed as well as cells that are over-erased. If any cells are programmed or over-erased, Blank Check will return a failure status, indicating that the block is not blank. If a Blank Check operation returns a passing status, the block is guaranteed blank (all 1's) and ready to program. The erase algorithm will do Blank Check for the target block firstly. If it's blank (all 1's) then the actual erase operation will be skipped. Otherwise, the actual erase operation will continue. This could benefit the overall cycle performance when erase happens on a blank block.

Blank check can occur in only one block at a time, and no operations other than Status Register Reads are allowed during Blank Check (e.g. reading array data, program, erase etc). Blank Check is not supported during any suspended operations. The status register can be examined for Blank Check progress and errors by reading any address within the device.

After the Blank Check operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs, Bus Read operations to the memory continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

6.1.7 Erase Suspend command

The Erase Suspend command can be used to temporarily suspend a Block Erase operation. One Bus Write operation is required to issue the command together with the block address.

After the command sequence is written, a minimum Block Erase time-out occurs (see *Table 28*). During the time-out period, additional block addresses and block erase commands can be written.

The Program/Erase controller suspends the erase operation within the Erase Suspend Latency time of the Erase Suspend command being issued. However, when the Erase Suspend command is written during the Block Erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

Once the Program/Erase controller has stopped, the memory operates in Read mode and the Erase is suspended.

During Erase Suspend it is possible to read and execute Program or Write to Buffer Program operations in blocks that are not suspended; both read and program operations behave as normal on these blocks. Reading from blocks that are suspended will output the Status Register. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. In this case the Status Register is not read and no error condition is given.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

During Erase Suspend a Bus Read operation to the Extended Memory Block will output the Extended Memory Block data. Once in the Extended Memory Block mode, the Exit Extended Memory Block command must be issued before the erase operation can be resumed.

The Erase Suspend command is ignored if written during Chip Erase operations.

Refer to *Table 28: Programming and Erase Performance* for the values of Block Erase time-out and Block Erase Suspend latency time.

If the Erase Suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to erase again the blocks suspended.

6.1.8 Erase Resume command

The Erase Resume command is used to restart the Program/Erase controller after an Erase Suspend.

The device must be in Read Array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

6.1.9 Program Suspend command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any block. When the Program Suspend command is issued during a program operation, the device suspends the program operation within the Program Suspend latency time (see *Table 28: Programming and Erase Performance*) and updates the Status Register bits.

After the program operation has been suspended, the system can read array data from any address. However, data read from program-suspended addresses is not valid.

The Program Suspend command may also be issued during a program operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Extended Memory Block area (one-time program area), the user must use the proper command sequences to enter and exit this region.

The system may also issue the Auto Select command sequence when the device is in the Program Suspend mode. The system can read as many Auto Select codes as required. When the device exits the Auto Select mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Auto Select command sequence for more information.

If the Program Suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to program again the words or bytes aborted.

6.1.10 Program Resume command

After the Program Resume command is issued, the device reverts to programming. The controller can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to *Figure 24: Write Enable Controlled Program waveforms (8-bit mode)* and *Figure 25: Write Enable Controlled Program waveforms (16-bit mode)* for details.

The system must issue a Program Resume command, to exit the Program Suspend mode and to continue the programming operation.

Further issuing of the Resume command is ignored. Another Program Suspend command can be written after the device has resumed programming.

6.1.11 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase controller.

Programming can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.9: Program Suspend command* and *Section 6.1.10: Program Resume command*).

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

After programming has started, Bus Read operations output the Status Register content. See *Figure 24: Write Enable Controlled Program waveforms (8-bit mode)* and *Figure 25:*

Write Enable Controlled Program waveforms (16-bit mode) for more details. Typical program times are given in *Table 28: Programming and Erase Performance*.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs, Bus Read operations to the memory continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

One of the Erase commands must be used to set all the bits in a block or in the whole memory from ‘0’ to ‘1’.

The Program operation is aborted by performing a reset or powering-down the device. In this case data integrity cannot be ensured, and it is recommended to reprogram the word or byte aborted.

Table 9. Standard commands, 8-bit mode

Command		Length	Bus operations(1)											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0	-	-	-	-	-	-	-	-	-	-
		3	AAA	AA	555	55	X	F0	-	-	-	-	-	-
Auto Select	Manufacturer code	3	AAA	AA	555	55	AAA	90	(2)(3)	(2)(3)	-	-	-	-
	Device code													
	Extended Memory Block protection indicator													
	Block protection status													
Program(4)		4	AAA	AA	555	55	AAA	A0	PA	PD	-	-	-	-
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase		6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30
Erase/Program Suspend		1	X	B0	-	-	-	-	-	-	-	-	-	-
Erase/Program Resume		1	X	30	-	-	-	-	-	-	-	-	-	-
Read CFI Query		1	AA	98	-	-	-	-	-	-	-	-	-	-
Blank Check setup		6	AAA	AA	555	55	BAd	EB	BAd	76	BAd	00	BAd	00
Blank Check confirm and read		2	BAd	29	BAd	(2)	-	-	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = Any address in the Block. All values in the table are in hexadecimal.
2. These cells represent Read cycles. The other cells are Write cycles.
3. The Auto Select addresses and data are given in *Table 5: Read electronic signature - auto select mode - programmer method (8-bit mode)*, and *Table 7: Block protection - auto select mode - programmer method (8-bit mode)*, except for A9 that is 'Don't care'.
4. In Unlock Bypass, the first two unlock cycles are no more needed (see *Table 11: Fast Program commands, 8-bit mode* and *Table 12: Fast Program commands, 16-bit mode*).

Table 10. Standard commands, 16-bit mode

Command		Length	Bus operations[(1)] 1st Add	1st Data	2nd Add	2nd Data	3rd Add	3rd Data	4th Add	4th Data	5th Add	5th Data	6th Add	6th Data
Read/Reset		1	X	F0	-	-	-	-	-	-	-	-	-	-
		3	555	AA	2AA	55	X	F0	-	-	-	-	-	-
Auto Select	Manufacturer code	3	555	AA	2AA	55	555	90	(2)(3)	(2)(3)	-	-	-	-
	Device code													
	Extended Memory Block protection indicator													
	Block protection status													
Program[(4)]		4	555	AA	2AA	55	555	A0	PA	PD	-	-	-	-
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase		6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30
Erase/Program Suspend		1	X	B0	-	-	-	-	-	-	-	-	-	-
Erase/Program Resume		1	X	30	-	-	-	-	-	-	-	-	-	-
Read CFI Query		1	55	98	-	-	-	-	-	-	-	-	-	-
Blank Check setup		6	555	AA	2AA	55	BAd	EB	BAd	76	BAd	00	BAd	00
Blank Check confirm and read		2	BAd	29	BAd	(2)	-	-	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = any address in the Block. All values in the table are in hexadecimal.
2. These cells represent Read cycles. The other cells are Write cycles.
3. The Auto Select addresses and data are given in *Table 6: Read electronic signature - auto select mode - programmer method (16-bit mode)*, and *Table 8: Block protection - auto select mode - programmer method (16-bit mode)*, except for A9 that is 'Don't care'.
4. In Unlock Bypass, the first two unlock cycles are no more needed (see *Table 11* and *Table 12* Fast Program commands, 8-bit and 16-bit mode).

6.2 Fast Program commands

The M29EW offers a set of Fast Program commands to improve the programming throughput:

– Double Byte/Word Program (for 32-Mbit and 64-Mbit devices)
– Quadruple Byte/Word Program (for 32-Mbit and 64-Mbit devices)
– Octuple Byte Program (for 32-Mbit and 64-Mbit devices)
– Write to Buffer Program
– Enhanced Buffer Program (x16 128-Mbit device only)
– Unlock Bypass

The *Table 11: Fast Program commands, 8-bit mode on page 46* and the *Table 12: Fast Program commands, 16-bit mode on page 47* show a summary of the Fast Program commands.

When V_{PPH} is applied to the V_{PP}/WP# pin during Write to Buffer Program and Enhanced Buffer Program, it will accelerate the programming speed. (see *Figure 31: Accelerated program timing waveforms*)

When V_{PPH} is applied to the V_{PP}/WP# pin in read mode, the memory automatically enters Unlock Bypass mode (see *Section 6.2.9: Unlock Bypass command*).

Note: For double byte/word program, quadruple byte/word program and octuple byte program, only V_{PPL} could be applied to the VPP/WP# pin.

After programming has started, Bus Read operations in the memory output the Status Register content. Write to Buffer Program command can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.9: Program Suspend command* and *Section 6.1.10: Program Resume command*).

After the fast program operation has completed, the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ‘0’ to ‘1’.

Typical program times are given in *Table 28: Programming and Erase Performance*.

6.2.1 Double Byte/Word Program command

The Double Byte/Word Program command for 32-Mbit and 64-Mbit devices is used to write a page of two adjacent bytes/words in parallel. The two bytes/words must differ only for the address A-1 or A0, respectively. Three bus write cycles are necessary to issue the Double Byte/Word Program command:

1. The first bus cycle sets up the Double Byte/Word Program command.
2. The second bus cycle latches the Address and the Data of the first byte/word to be programmed.
3. The third bus cycle latches the Address and the Data of the second byte/word to be programmed and starts the Program/Erase Controller.

See *Table 11: Fast Program commands, 8-bit mode* and *Table 12: Fast Program commands, 16-bit mode* for command details.

6.2.2 Quadruple Byte/Word Program command

The Quadruple Byte/Word Program command for 32-Mbit and 64-Mbit devices is used to write a page of four adjacent bytes/words in parallel. The four bytes/words must differ for addresses A0, DQ15/A-1 in x8 mode or addresses A1, A0 in x16 mode. Five bus write cycles are necessary to issue the Quadruple Byte/Word Program command:

1. The first bus cycle sets up the Quadruple Byte/Word Program command.
2. The second bus cycle latches the Address and the Data of the first byte/word to be programmed.
3. The third bus cycle latches the Address and the Data of the second byte/word to be programmed.
4. The fourth bus cycle latches the Address and the Data of the third byte/word to be programmed.
5. The fifth bus cycle latches the Address and the Data of the fourth byte/word to be programmed and starts the Program/Erase Controller.

See *Table 11: Fast Program commands, 8-bit mode* and *Table 12: Fast Program commands, 16-bit mode* for command details.

6.2.3 Octuple Byte Program command

The Octuple Byte Program command for 32-Mbit and 64-Mbit devices is used to write a page of eight adjacent bytes in parallel. The eight bytes must differ for addresses A1, A0, DQ15/A-1 in x8 mode only. Nine bus write cycles are necessary to issue the Octuple Byte Program command:

1. The first bus cycle sets up the Octuple Byte Program command.
2. The second bus cycle latches the Address and the Data of the first byte to be programmed.
3. The third bus cycle latches the Address and the Data of the second byte to be programmed.
4. The fourth bus cycle latches the Address and the Data of the third byte to be programmed.
5. The fifth bus cycle latches the Address and the Data of the fourth byte to be programmed.
6. The sixth bus cycle latches the Address and the Data of the fifth byte to be programmed.
7. The seventh bus cycle latches the Address and the Data of the sixth byte/word to be programmed.
8. The eighth bus cycle latches the Address and the Data of the seventh byte/word to be programmed.
9. The ninth bus cycle latches the Address and the Data of the eighth byte/word to be programmed and starts the Program/Erase Controller.

See *Table 11: Fast Program commands, 8-bit mode* and *Table 12: Fast Program commands, 16-bit mode* for command details.

6.2.4 Write to Buffer Program command

The Write to Buffer Program command makes use of the device's 256-word program buffer to speed up programming. A maximum of 256 words can be loaded into the program buffer in word mode. In byte mode, the maximum buffer size is 256-byte (128-word) due to the limitation of 8 pins. The Write to Buffer Program command dramatically reduces system programming time compared to the standard non-buffered Program command.

Note: The maximum number of bytes in write buffer in CFI region (refer to offset 2Ah, Table 39: Device geometry definition on page 93) is set to 08h (256 bytes) for backward compatible reasons. No software change is required on the existing applications in both x8 and x16 mode. However, the system performance can be optimized by implement the maximum 256-word buffer size, contact your sales representatives for questions.

When issuing a Write to Buffer Program command, the V_{PP}/WP# pin can be either held High, V_{IH}, or raised to V_{PPH} (programming acceleration).

See *Table 28* for details on typical Write to Buffer Program times in both cases.

Five successive steps are required to issue the Write to Buffer Program command:

1. The Write to Buffer Program command starts with two unlock cycles.
2. The third bus write cycle sets up the Write to Buffer Program command. The set-up code can be addressed to any location within the targeted block.
3. The fourth bus write cycle sets up the number of words/bytes to be programmed. Value N is written to the same block address, where N+1 is the number of words/bytes to be programmed. N+1 must not exceed the size of the program buffer, otherwise the operation will abort. In x8 mode, the maximum N should be no more than 256.
4. The fifth cycle loads the first address and data to be programmed.
5. Use N bus write cycles to load the address and data for each word/byte into the program buffer. Addresses must lie within the range from the start address+1 to the start address + N-1. Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 256-word boundary (A[7:0] = 000h). All the addresses used in the Write to Buffer Program operation must lie within the 256-word boundary. Any crossing boundary buffer program will result in a program abort. See *Figure 10* for details of the available program buffer size.

To program the content of the program buffer, this command must be followed by a Write to Buffer Program Confirm command.

If an address is written several times during a Write to Buffer Program operation, the address/data counter will be decremented at each data load operation and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will abort the Write to Buffer Program.

The Status Register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a Write to Buffer Program operation.

It is possible to detect Program operation fails when changing programmed data from '0' to '1', that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous value and the current value.

See *Figure 11: Write to Buffer Program fletcher and pseudo code*, for a suggested flow chart on using the Write to Buffer Program command.

6.2.5 Enhanced Buffer Program

The Enhanced Buffer Program command, available only on x16 mode 128-Mbit device, makes use of the device's 256-word write buffer to speed up programming. 256 words can be loaded into the write buffer. Each write buffer has the same A22-A8 addresses. The Enhanced Buffer Program command dramatically reduces system programming time.

When issuing a Enhanced Buffer Program command, the V_{PP}/WP# pin can be either held High, V_{IH}, or raised to V_{PPH} (programming acceleration).

The Enhanced Buffer Program has the same programming speed as a 256-word write to buffer program speed. See *Table 28* for details.

Three successive steps are required to issue the Enhanced Buffer Program command:

- The Enhanced Buffered Program command starts with two unlock cycles.
- The third bus write cycle sets up the Enhanced Buffered Program command. The setup code can be addressed to any location within the targeted block.
- The fourth bus write cycle loads the first address and data to be programmed. There a total of 256 address and data loading cycles.

To program the content of the write buffer, the Enhanced Buffer Program command must be followed by an Enhanced Buffer Program Confirm command. The command ends with an internal Enhanced Buffer Program confirm cycle.

Note that address/data cycles must be loaded in an increasing address order (A[7:0] from 00h to FFh) and completely (all 256 words). Invalid address combinations or failing to follow the correct sequence of bus write cycles will result in Enhanced Buffer Program abort.

The status register bits DQ1, DQ5, DQ6, and DQ7 can be used to monitor the device status during an Enhanced Buffer Program operation.

An external supply (12 V) can be used to improve programming efficiency.

It is possible to detect program operation fails when changing programmed data from “0” to “1”.

Note: Enhanced Buffered Program commands are available for x 16 mode only.

Figure 10. Boundary condition of program buffer size

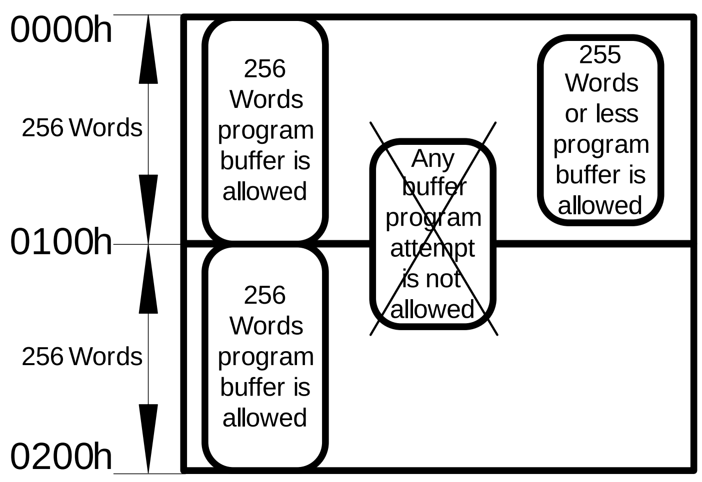
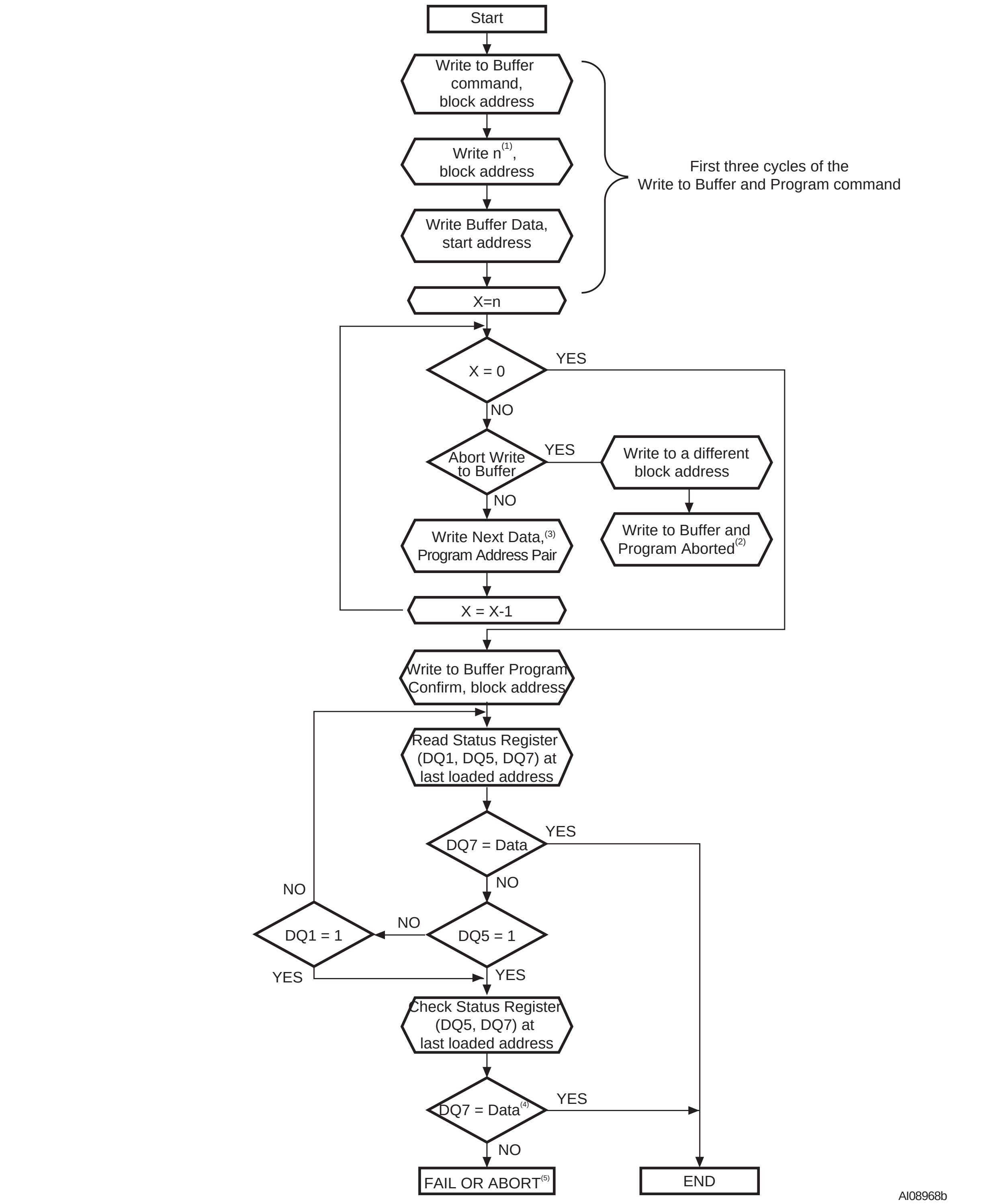


Figure 11. Write to Buffer Program fletcher and pseudo code



1. n+1 is the number of addresses to be programmed.
2. A Write to Buffer Program Abort and Reset must be issued to return the device in Read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However when

loading program buffer address with data, all addresses must fall within the selected program buffer page.

4. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
5. If this flow chart location is reached because DQ5='1', then the Write to Buffer Program command failed. If this flow chart location is reached because DQ1='1', then the Write to Buffer Program command aborted. In both cases, the appropriate reset command must be issued to return the device in Read mode: a Reset command if the operation failed, a Write to Buffer Program Abort and Reset command if the operation aborted.
6. See *Table 9* and *Table 10*, for details on Write to Buffer Program command sequence.

6.2.6 Buffered Program Abort and Reset command

A Buffered Program Abort and Reset command must be issued to abort the Buffer Program operation and reset the device in Read mode.

The buffer programming sequence can be aborted in the following ways:

– Load a value that is greater than the page buffer size during the number of locations to program step in the Write to Buffer Program command.
– Write to an address in a block different than the one specified during the write-buffer-load command.
– Write an address/data pair to a different write-buffer-page than the one selected by the starting address during the program buffer data loading stage of the operation.
– Write data other than the Confirm command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = $\overline{DQ7}$ (for the last address location loaded), DQ6 = toggle, and DQ5 = 0 (all of which are Status Register bits). A Buffered Program Abort and Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Buffered Program Abort and Reset command sequence is required when using Buffer Programming features in Unlock Bypass mode.

6.2.7 Write to Buffer Program Confirm command

The Write to Buffer Program Confirm command is used to confirm a Write to Buffer Program command and to program the N+1 words/bytes loaded in the program buffer by this command.

6.2.8 Enhanced Buffer Program Confirm command

The Enhanced Buffer Program Confirm command is used to confirm an Enhanced Buffer Program command and to program the 256 words loaded in the buffer.

6.2.9 Unlock Bypass command

The Unlock Bypass command is used to place the device in Unlock Bypass mode. When the device enters the Unlock Bypass mode, the two initial unlock cycles required in the standard program command sequence are no more needed, and only two write cycles are required to program data, instead of the normal four cycles (see *Note 4* below *Table 9* and *Table 10*). This results in a faster total programming time.

Unlock Bypass command is consequently used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

When in Unlock Bypass mode, only the Unlock Bypass Program, Unlock Bypass Block Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid:

- The Unlock Bypass Program command can be issued to program addresses within the memory.
- The Unlock Bypass Block Erase command can then be issued to erase one or more memory blocks.
- The Unlock Bypass Chip Erase command can be issued to erase the whole memory array.
- The Unlock Bypass Write to Buffer Program command can be issued to speed up programming operation.
- The Unlock Bypass Reset command can be issued to return the memory to Read mode.

In Unlock Bypass mode the memory can be read as if in Read mode.

6.2.10 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write operations, the final write operation latches the address and data and starts the Program/Erase controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted, a Bus Read operation to the memory outputs the Status Register. See the program command in *Table 11.: Fast Program commands, 8-bit mode* and *Table 12.: Fast Program commands, 16-bit mode* for more details.

6.2.11 Unlock Bypass Block Erase command

The Unlock Bypass Block Erase command can be used to Erase one or more memory blocks at a time. The command requires two Bus Write operations instead of six using the standard Block Erase command. The final Bus Write operation latches the address of the block and starts the Program/Erase controller.

To erase multiple block (after the first two Bus Write operations have selected the first block in the list), each additional block in the list can be selected by repeating the second Bus Write operation using the address of the additional block.

The Unlock Bypass Block Erase command behaves in the same way as the Block Erase command: the operation cannot be aborted, and a Bus Read operation to the memory outputs the Status Register (see *Section 6.1.5: Block Erase command* for details).

6.2.12 Unlock Bypass Chip Erase command

The Unlock Bypass Chip Erase command can be used to erase all memory blocks at a time. The command requires two Bus Write operations only instead of six using the standard Chip Erase command. The final Bus Write operation starts the Program/Erase controller.

The Unlock Bypass Chip Erase command behaves in the same way as the Chip Erase command: the operation cannot be aborted, and a Bus Read operation to the memory outputs the Status Register (see *Section 6.1.4: Chip Erase command* for details).

6.2.13 Unlock Bypass Write to Buffer Program command

The Unlock Bypass Write to Buffer command can be used to program the memory in Fast Program mode. The command requires two Bus Write operations less than the standard Write to Buffer Program command.

The Unlock Bypass Write to Buffer Program command behaves in the same way as the Write to Buffer Program command: the operation cannot be aborted and a Bus Read operation to the memory outputs the Status Register (see *Section 6.2.4: Write to Buffer Program command* for details).

The Write to Buffer Program Confirm command is used to confirm an Unlock Bypass Write to Buffer Program command and to program the N+1 words/bytes loaded in the program buffer by this command.

6.2.14 Unlock Bypass Enhanced Buffer Program command

The Unlock Bypass Enhanced Buffer Program command can be used to program the memory in fast program mode. The command requires two address/data loading cycles less than the regular Enhanced Buffer Program command (see *Table 12: Fast Program commands, 16-bit mode* for the details).

The Unlock Bypass Enhanced Buffer Program command behaves identically to the Enhanced Buffer Program operation using the Enhanced Buffer Program command. The operation cannot be aborted and a bus read operation to the memory outputs the status register (see *Chapter 6.2.8: Enhanced Buffer Program Confirm command* for the behavior details).

The Enhanced Buffer Program Confirm command is used to confirm an Unlock Bypass Enhanced Buffer Program command and to program the 256 words loaded in the buffer.

6.2.15 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass mode.

Table 11. Fast Program commands, 8-bit mode

Command	Length	Bus Write operations(1)									
		1st		2nd		3rd		4th		5th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Double Byte Program	3	AAA	50	PA2(2)	PD	-	-	-	-	-	-
Quadruple Byte Program	5	AAA	56	PA4(3)	PD	-	-	-	-	-	-
Octuple byte Program	9	AAA	8B	PA8(4)	PD	-	-	-	-	-	-
Write to Buffer Program	N+5	AAA	AA	555	55	BAd	25	BAd	N(5)	PA(6)	PD
Write to Buffer Program Confirm	1	BAd(7)	29	-	-	-	-	-	-	-	-
Buffered Program Abort and Reset	3	AAA	AA	555	55	AAA	F0	-	-	-	-
Unlock Bypass mode entry	3	AAA	AA	555	55	AAA	20	-	-	-	-
Unlock Bypass Program	2	X	A0	PA	PD	-	-	-	-	-	-
Unlock Bypass Block Erase	2+	X	80	BAd	30	-	-	-	-	-	-
Unlock Bypass Chip Erase	2	X	80	X	10	-	-	-	-	-	-
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N(5)	PA(6)	PD	-	-	-	-
Unlock Bypass Reset	2	X	90	X	00	-	-	-	-	-	-

1. X = Don’t care, PA = Program Address, PD = Program Data, BAd = Any address in the Block. All values in the table are in hexadecimal.
2. Amax-A0 address pins should remian unchanged. Address A-1 selects between adjacent bytes.
3. Amax-A1 address pin should remain unchanged. A0 and A-1 pins are used to select four adjacent bytes. This address should be used four times.
4. Amax-A2 address pin should remain unchanged. A1, A0 and A-1 pins are used to select eight adjacent bytes. This address should be used eight times.
5. The maximum number of cycles in the buffer program command sequence is 261. The maximum number of cycles in the unlock bypass buffer program command sequence is 259. N+1 is the number of bytes to be programmed during the Write to Buffer Program operation.
6. Amax-A7 address pins should be consistently unchanged. Addresses A[6:-1] select a byte within the N+1 byte page.
7. BAd must be identical to the address loaded during the Write to Buffer Program 3rd and 4th cycles.

Table 12. Fast Program commands, 16-bit mode

Command	Length	Bus Write operations[1]									
		1st		2nd		3rd		4th		5th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Double Word Program	3	555	50	PA2[2]	PD	-	-	-	-	-	-
Quadruple Word Program	5	555	56	PA4[3]	PD	-	-	-	-	-	-
Write to Buffer Program	N+5	555	AA	2AA	55	BAd	25	BAd	N[4]	PA[5]	PD
Write to Buffer Program Confirm	1	BAd[6]	29	-	-	-	-	-	-	-	-
Enhanced Buffer Program	N+5	555	AA	2AA	55	BAd	33	BAd	N[4]	PA[5]	PD
Enhanced Buffer Program Confirm	1	BAd[6]	29	-	-	-	-	-	-	-	-
Buffered Program Abort and Reset	3	555	AA	2AA	55	555	F0	-	-	-	-
Unlock Bypass mode entry	3	555	AA	2AA	55	555	20	-	-	-	-
Unlock Bypass Program	2	X	A0	PA	PD	-	-	-	-	-	-
Unlock Bypass Block Erase	2+	X	80	BAd	30	-	-	-	-	-	-
Unlock Bypass Chip Erase	2	X	80	X	10	-	-	-	-	-	-
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N[4]	PA[5]	PD	-	-	-	-
Unlock Bypass Enhanced Buffer Program	N+3	BAd	33	BAd	N[4]	PA[5]	PD	-	-	-	-
Unlock Bypass Reset	2	X	90	X	00	-	-	-	-	-	-

1. X = Don't care, PA = Program Address, PD = Program Data, BAd = Any address in the Block. All values in the table are in hexadecimal.
2. Amax-A1 address pin should remain unchanged. A0 pin is used to select two adjacent words.
3. Amax-A2 address pin should remian unchanged. A1 and A0 pins are used to select four adjacent words. This address should be used four times.
4. The maximum number of cycles in the buffer program command sequence is 261. The maximum number of cycles in the unlock bypass buffer program command sequence is 259. N+1 is the number of bytes to be programmed during the Write to Buffer Program operation.
5. Amax-A9 address pins should be consistently unchanged. A0-A8 pins are used to select a word within the N+1 word page.
6. BAd must be identical to the address loaded during the Write to Buffer Program 3rd and 4th cycles.

6.3 Protection commands

Blocks can be protected individually against accidental program, erase or read operations. The device block protection scheme is shown in *Figure 9: Software protection scheme*. See either *Table 13*, or *Table 14*, depending on the configuration that is being used, for a summary of the Block Protection commands.

Block protection commands are available both in 8-bit and 16-bit configuration.

The protections of both memory blocks and Extended Memory Block protection are configured through the Lock register (see *Section 7.1: Lock Register*).

6.3.1 Enter Extended Memory Block command

The M29EW has one extra 128-word Extended Memory Block that can only be accessed using the Enter Extended Memory Block command.

Three Bus Write cycles are required to issue the Enter Extended Memory Block command. Once the command has been issued the device enters the Extended Memory Block mode where all Bus Read or Program operations are conducted on the Extended Memory Block. Once the device is in the Extended Memory Block mode, the Extended Memory Block is addressed by using the addresses occupied by block 0 in the other operating modes (see *Figure 8: 64-Mbit and 32-Mbit Boot Block addresses on page 14*).

The device remains in Extended Memory Block mode until the Exit Extended Memory Block command is issued or power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading from memory blocks in the main array.

The Extended Memory Block cannot be erased, and each bit of the Extended Memory Block can only be programmed once.

In Extended Memory Block mode, Erase, Chip Erase, Erase Suspend and Erase Resume commands are not allowed.

To exit from the Extended Memory Block mode the Exit Extended Memory Block command must be issued.

The Extended Memory Block is protected from further modification by programming Lock Register bit 0 (see *Section 7.1: Lock Register*). Once invoked, this protection cannot be undone.

6.3.2 Exit Extended Memory Block command

The Exit Extended Memory Block command is used to exit from the Extended Memory Block mode and return the device to Read mode. Four Bus Write operations are required to issue the command.

6.3.3 Lock Register command set

The M29EW offers a set of commands to access the Lock Register and to configure and verify its content. See the following sections in conjunction with *Section 7.1: Lock Register*, *Table 13* and *Table 14*.

Enter Lock Register Command Set command

Three Bus Write cycles are required to issue the Enter Lock Register Command Set command. Once the command has been issued, all Bus Read or Program operations are issued to the Lock Register.

Lock Register Program and Lock Register Read command

The Lock Register Program command allows to configure the Lock Register. The programmed data can then be checked by issuing a Lock Register Read command.

An Exit Protection Command Set command must then be issued to return the device to Read mode (see *Section 6.3.8: Exit Protection command set*).

6.3.4 Password Protection mode command set

Enter Password Protection Command Set command

Three Bus Write cycles are required to issue the Enter Password Protection Command Set command. Once the command has been issued, the commands related to the Password Protection mode can be issued to the device.

Password Program command

The Password Program command is used to program the 64-bit password used in the Password Protection mode.

To program the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A1-A0 plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A1-A0 in 16-bit mode.

The password can be checked by issuing a Password Read command.

Once Password Program operation has completed, an Exit Protection Command Set command must be issued to return the device to Read mode. The Password Protection mode can then be selected.

By default, all Password bits are set to ‘1’.

Password Read command

The Password Read command is used to verify the Password used in Password Protection mode.

To verify the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A1-A0 plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A1-A0 in 16-bit mode.

If the Password Mode Lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

An Exit Protection Command Set command must be issued to return the device to Read mode.

Password Unlock command

The Password Unlock command is used to clear the NVPB Lock bit allowing to modify the NVPBs.

The Password Unlock command must be issued along with the correct password.

There must be a 1 µs delay between successive Password Unlock commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay is not respected, the latest command will be ignored.

Approximately 1 µs is required for unlocking the device after the valid 64-bit password has been provided.

6.3.5 Non-Volatile Protection mode command set

Enter Non-Volatile Protection Command Set command

Three Bus Write cycles are required to issue the Enter Non-Volatile Protection Command Set command. Once the command has been issued, the commands related to the Non-Volatile Protection mode can be issued to the device.

Non-Volatile Protection Bit Program command (NVPB Program)

A block can be protected from program or erase by issuing a Non-Volatile Protection Bit command along with the block address. This command sets the NVPB to ‘1’ for a given block.

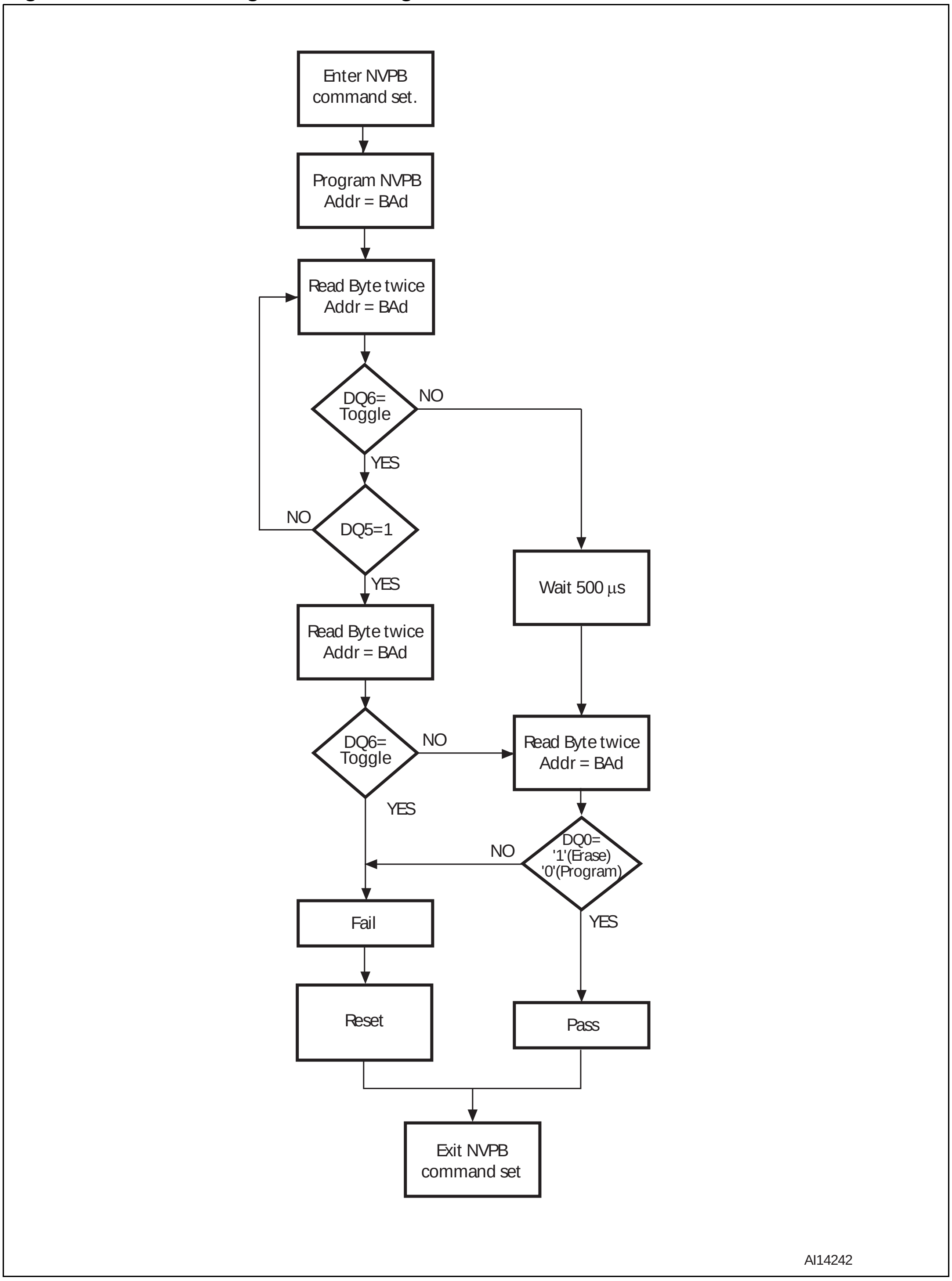
Read Non-Volatile Protection Bit Status command (Read NVPB Status)

The status of a NVPB for a given block or group of blocks can be read by issuing a Read Non-Volatile Modify Protection Bit command along with the block address.

Clear all Non-Volatile Protection Bits command (Clear all NVPBs)

The NVPBs are erased simultaneously by issuing a Clear all Non-Volatile Protection Bits command. No specific block address is required. If the NVPB Lock bit is set to ‘0’, the command fails.

Figure 12. NVPB Program/Erase algorithm



6.3.6 NVPB Lock Bit command set

Enter NVPB Lock Bit Command Set command

Three bus Write cycles are required to issue the Enter NVPB Lock Bit Command Set command. Once the command has been issued, the commands allowing to set the NVPB Lock bit can be issued to the device.

NVPB Lock Bit Program command

This command is used to set the NVPB Lock bit to ‘0’ thus locking the NVPBs, and preventing them from being modified.

Read NVPB Lock Bit Status command

This command is used to read the status of the NVPB Lock bit.

6.3.7 Volatile Protection mode command set

Enter Volatile Protection Command Set command

Three bus Write cycles are required to issue the Enter Volatile Protection Command Set command. Once the command has been issued, the commands related to the Volatile Protection mode can be issued to the device.

Volatile Protection Bit Program command (VPB Program)

The VPB Program command individually sets a VPB to ‘0’ for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit. (see *Table 16: Block Protection Status*).

Read VPB Status command

The status of a VPB for a given block can be read by issuing a Read VPB Status command along with the block address.

VPB Clear command

The VPB Clear command individually clears (sets to ‘1’) the VPB for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit. (see *Table 16: Block Protection Status*).

6.3.8 Exit Protection command set

The Exit Protection Command Set command is used to exit from the Lock Register, Password Protection, Non-Volatile Protection, Volatile Protection, and NVPB Lock Bit Command Set mode. It return the device to Read mode.

Table 13. Block Protection commands, 8-bit mode(1)(2)(3)

	Command	Length	Bus operations																					
			1st		2nd		3rd		4th		5th		6th		7th		8th		9th		10th		11th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock Register	Enter Lock Register Command Set(4)	3	AAA	AA	555	55	AAA	40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Lock Register	Lock Register Program	2	X	A0	X	DATA (5)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Lock Register	Lock Register Read	1	X	DATA (5)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Password Protection	Enter Password Protection Command Set(4)	3	AAA	AA	555	55	AAA	60	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Password Protection	Password Program (6)(7)	2	X	A0	PWAn	PWDn	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Password Protection	Password Read	8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6	07	PWD7	-	-	-	-	-	-
Password Protection	Password Unlock(7)	11	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6	07	PWD7	00	29
Non-Volatile Protection	Enter Non-Volatile Protection Command Set(4)	3	AAA	AA	555	55	AAA	C0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Non-Volatile Protection	NVPB Program(8)	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Non-Volatile Protection	Clear all NVPBs(9)	2	X	80	00	30	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Non-Volatile Protection	Read NVPB Status (8)	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NVPB Lock bit	Enter NVPB Lock Bit Command Set	3	AAA	AA	555	55	AAA	50	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NVPB Lock bit	NVPB Lock Bit Program(8)	2	X	A0	X	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NVPB Lock bit	Read NVPB Lock Bit Status (8)	1	X	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	Enter Volatile Protection Command Set	3	AAA	AA	555	55	AAA	E0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	VPB Program(8)	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	Read VPB Status	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	VPB Clear(8)	2	X	A0	BAd	01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Exit Protection Command Set (10)		2	X	90	X	00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Enter Extended Memory Block(4)		3	AAA	AA	555	55	AAA	88	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

1. Ad = address; Dat = data; BAd = Any address in the Block; RD = Read data; PWDn = Password byte 0 to 7; PWAn = Password Address (n = 0 to 7); X = Don't care. All values in the table are in hexadecimal.
2. Grey cells represent Read cycles. The other cells are Write cycles.
3. DQ15 to DQ8 are 'Don't care' during unlock and command cycles. Amax to A16 are 'Don't care' during unlock and command cycles unless an address is required.
4. An Enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = Lock Register content.
6. Only one portion of password can be programmed or read by each Password Program command.
7. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Protected and unprotected states correspond to 00 and 01, respectively.
9. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared Non Volatile Modify Protection bits.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to Read mode.

Table 14. Block Protection commands, 16-bit mode[1][2][3]

Command		Length	Bus operations													
			1st		2nd		3rd		4th		5th		6th		7th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock register	Enter Lock Register Command Set[4]	3	555	AA	2AA	55	555	40	-	-	-	-	-	-	-	-
	Lock Register Program	2	X	A0	X	DATA[5]	-	-	-	-	-	-	-	-	-	-
	Lock Register Read	1	X	DATA [5]	-	-	-	-	-	-	-	-	-	-	-	-
Password Protection	Enter Password Protection Command Set[4]	3	555	AA	2AA	55	555	60	-	-	-	-	-	-	-	-
	Password Program [6][7]	2	X	A0	PWAn	PWDn	-	-	-	-	-	-	-	-	-	-
	Password Read	4	00	PWD0	01	PWD1	02	PWD2	03	PWD3	-	-	-	-	-	-
	Password Unlock[7]	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
Non-Volatile Protection	Enter Non-Volatile Protection Command Set[4]	3	555	AA	2AA	55	555	C0	-	-	-	-	-	-	-	-
	NVPB Program[8]	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-
	Clear all NVPBs[9]	2	X	80	00	30	-	-	-	-	-	-	-	-	-	-
	Read NVPB Status	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-
NVPB Lock bit	Enter NVPB Lock Bit Command Set	3	555	AA	2AA	55	555	50	-	-	-	-	-	-	-	-
	NVPB Lock Bit Program	2	X	A0	X	00	-	-	-	-	-	-	-	-	-	-
	Read NVPB Lock Bit Status	1	X	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-
Volatile Protection	Enter Volatile Protection Command Set	3	555	AA	2AA	55	555	E0	-	-	-	-	-	-	-	-
	VPB Program	2	X	A0	BAd	00	-	-	-	-	-	-	-	-	-	-
	Read VPB Status	1	BAd	RD(0)	-	-	-	-	-	-	-	-	-	-	-	-
	VPB Clear	2	X	A0	BAd	01	-	-	-	-	-	-	-	-	-	-
Exit Protection Command Set[10]		2	X	90	X	00	-	-	-	-	-	-	-	-	-	-
Enter Extended Memory Block[4]		3	555	AA	2AA	55	555	88	-	-	-	-	-	-	-	-
Exit Extended Memory Block		4	555	AA	2AA	55	555	90	X	00	-	-	-	-	-	-

1. Ad = address; Dat = data; BAd = Any address in the Block; RD = Read data; PWDn = Password byte 0 to 3; PWAn = Password Address (n = 0 to 3); X = Don't care. All values in the table are in hexadecimal.
2. Grey cells represent Read cycles. The other cells are Write cycles.
3. DQ15 to DQ8 are 'Don't care' during unlock and command cycles. Amax to A16 are 'Don't care' during unlock and command cycles unless an address is required.
4. An Enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = Lock Register content.
6. Only one portion of password can be programmed or read by each Password Program command.
7. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Protected and unprotected states correspond to 00 and 01, respectively.
9. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared Non-volatile Modify Protection bits.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to Read mode.

7 Registers

The device features two registers:

1. A Lock Register that allows to configure the memory blocks and Extended Memory Block protection (see *Table 16: Block Protection Status*)
2. A Status Register that provides information on the current or previous Program or Erase operations.

7.1 Lock Register

The Lock Register is a 16-bit one-time programmable register. The bits in the Lock Register are summarized in *Table 15: Lock Register bits*.
See *Section 6.3.3: Lock Register command set* for a description of the commands allowing to read and program the Lock Register.

7.1.1 Password Protection Mode Lock bit (DQ2)

The Password Protection Mode Lock bit, DQ0, is one-time programmable. Programming (setting to '0') this bit permanently places the device in Password Protection mode.

Any attempt to program the Password Protection mode Lock bit when the Non-Volatile Protection Mode bit is programmed causes the operation to abort and the device to return to Read mode.

7.1.2 Non-Volatile Protection Mode Lock bit (DQ1)

The Non-Volatile Protection Mode Lock bit, DQ1, is one-time programmable. Programming (setting to '0') this bit permanently places the device in Non-Volatile Protection mode.

When shipped from Numonyx factory, all parts default to operate in Non-Volatile Protection mode. The memory blocks are unprotected (NVPBs set to '1').

Any attempt to program the Non-Volatile Protection mode Lock bit when the Password Protection Mode bit is programmed causes the operation to abort and the device to return to Read mode.

7.1.3 Extended Memory Block Protection bit (DQ0)

If the device is shipped with the Extended Memory Block unlocked, the block can be protected by setting the Extended Memory Block Protection bit, DQ0, to '0'. However, this bit is one-time programmable and once protected the Extended Memory Block cannot be unprotected any more.

The Extended Memory Block protection status can be read in Auto Select mode by issuing an Auto Select command (see *Table 9* and *Table 10*).

Table 15. Lock Register bits(1)

DQ15-3(2)	DQ2	DQ1	DQ0
Reserved	Password Protection Mode Lock bit	Non-Volatile Protection Mode Lock bit	Extended Memory Block Protection bit

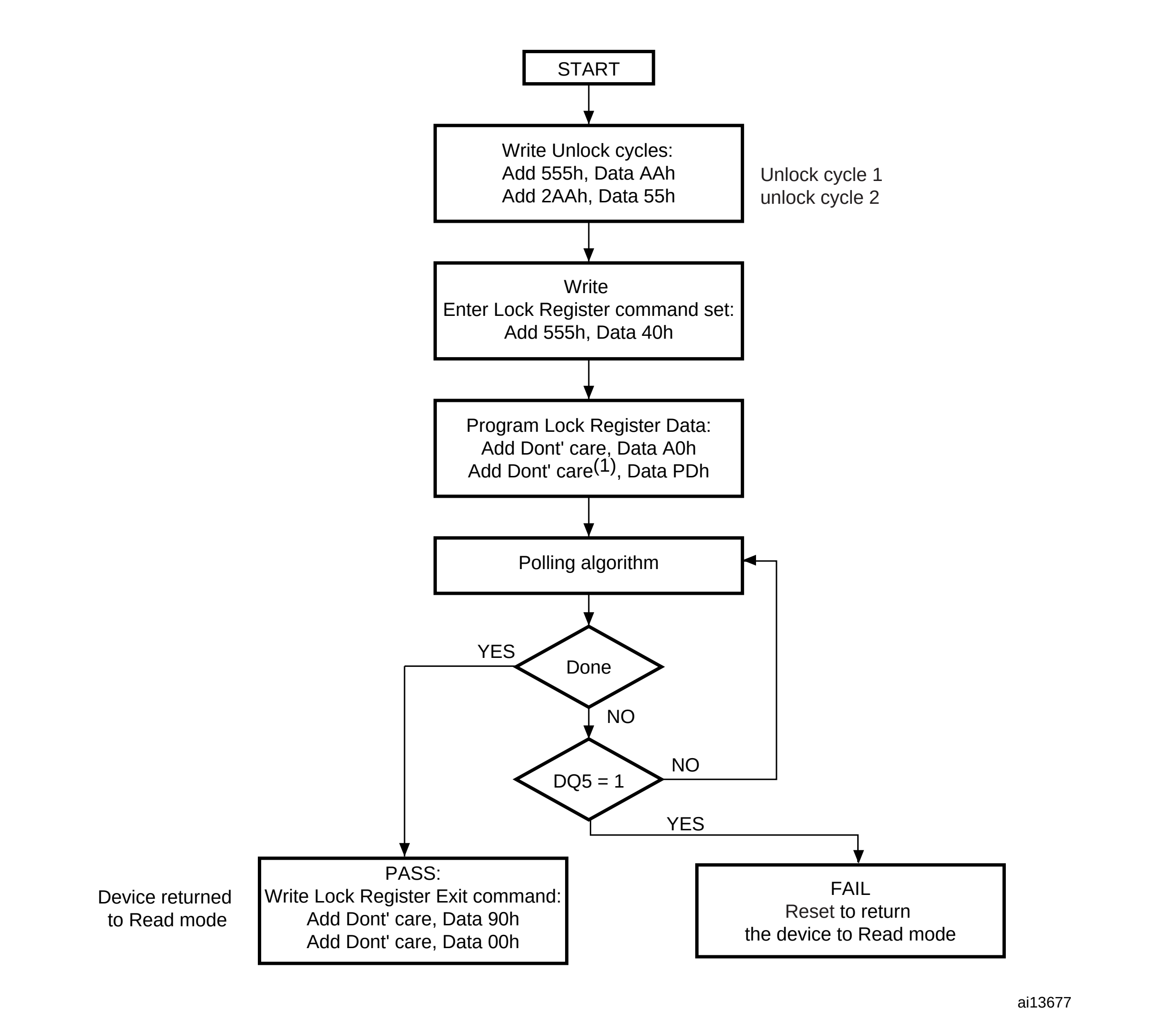
1. DQ0, DQ1 and DQ2 Lock Register bits are set to ‘1’ when shipped from the Numonyx.
2. DQ15 to DQ3 are reserved and default to ‘1’.

Table 16. Block Protection Status

NVPB Lock bit(1)	Block NVPB(2)	Block VPB(3)	Block protection status	Block Protection Status
1	1	1	00h	Block unprotected (NVPB changeable)
1	1	0	01h	Block protected by VPB (NVPB changeable)
1	0	1	01h	Block protected by NVPB (NVPB changeable)
1	0	0	01h	Block protected by NVPB and VPB (NVPB changeable)
0	1	1	00h	Block unprotected (NVPB unchangeable)
0	1	0	01h	Block protected by VPB (NVPB unchangeable)
0	0	1	01h	Block protected by NVPB (NVPB unchangeable)
0	0	0	01h	Block protected by NVPB and VPB (NVPB unchangeable)

1. If the NVPB Lock bit is set to ‘0’, all NVPBs are locked. If the NVPB Lock bit is set to ‘1’, all NVPBs are unlocked.
2. If the Block NVPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.
3. If the Block VPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.

Figure 13. Lock Register program flow chart



1. PD is the programmed data (see *Table 15: Lock Register bits*).
2. Each bit of the Lock Register can only be programmed once.

7.2 Status Register

The M29EW device has one Status Register. The various bits convey information and errors on the current and previous program/erase operation. Bus Read operations from any address within the memory, always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in *Table 17: Status Register bits*.

7.2.1 Data Polling bit (DQ7)

The Data Polling bit can be used to identify whether the Program/Erase controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations, from the address just programmed, output DQ7, not its complement.

During Erase or Blank Check operations the Data Polling bit outputs ‘0’, the complement of the erased state of DQ7. When the algorithm is complete, Data Polling produces a '1' on DQ7. After successful completion of the Erase or Blank Check operation the memory returns to Read mode.

In Erase Suspend mode the Data Polling bit will output a ‘1’ during a Bus Read operation within a block being erased. The Data Polling bit will change from ‘0’ to ‘1’ when the Program/Erase controller has suspended the Erase operation.

Figure 14: Data polling flow chart, gives an example of how to use the Data Polling bit. A Valid Address is the address being programmed or an address within the block being erased or blank checked.

7.2.2 Toggle bit (DQ6)

The Toggle bit can be used to identify whether the Program/Erase controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle bit is output on DQ6 when the Status Register is read.

During a Program/Erase operation the Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle bit will output when addressing a cell within a block being erased. The Toggle bit will stop toggling when the Program/Erase controller has suspended the Erase operation.

Figure 15: Toggle flow chart, gives an example of how to use the Data Toggle bit.

7.2.3 Error bit (DQ5)

The Error bit can be used to identify errors detected by the Program/Erase controller. The Error bit is set to ‘1’ when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory, or a Blank Check operation fails. If the Error bit is set a

Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to ‘0’ back to ‘1’ and attempting to do so will set DQ5 to ‘1’. A Bus Read operation to that address will show the bit is still ‘0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ‘0’ to ‘1’.

7.2.4 Erase Timer bit (DQ3)

The Erase Timer bit can be used to identify the start of Program/Erase controller operation during a Block Erase command. Once the Program/Erase controller starts erasing the Erase Timer bit is set to ‘1’. Before the Program/Erase controller starts the Erase Timer bit is set to ‘0’ and additional blocks to be erased may be written to the command interface. The Erase Timer bit is output on DQ3 when the Status Register is read.

7.2.5 Alternative Toggle bit (DQ2)

The Alternative Toggle bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory array data as if in Read mode.

After an Erase operation that causes the Error bit to be set, the Alternative Toggle bit can be used to identify which block or blocks have caused the error. The Alternative Toggle bit changes from ‘0’ to ‘1’ to ‘0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle bit does not change if the addressed block has erased correctly.

7.2.6 Buffered Program Abort bit (DQ1)

The Buffered Program Abort bit, DQ1, is set to ‘1’ when a Buffer Program operation aborts. The Buffered Program Abort and Reset command must be issued to return the device to Read mode (see Write to Buffer Program in *Section 6.1: Standard commands*).

For the complete polling flow chart, please refer to *Figure 16.: Status Register polling flow chart*.

Table 17. Status Register bits(1)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#
Program(2)	Any address	$\overline{DQ7}$	Toggle	0	–	No Toggle	0	0
Program During Erase Suspend	Any address	$\overline{DQ7}$	Toggle	0	–	–	–	0
Buffered Program Abort(2)	Any address	$\overline{DQ7}$	Toggle	0	–	–	1	0
Program Error	Any address	$\overline{DQ7}$	Toggle	1	–	–	–	Hi-Z
Chip Erase	Any address	0	Toggle	0	1	Toggle	–	0
Block Erase before timeout	Erasing block	0	Toggle	0	0	Toggle	–	0
	Non-erasing block	0	Toggle	0	0	No toggle	–	0
Block Erase/Blank Check	Erasing/Verifying block	0	Toggle	0	1	Toggle	–	0
	Non-erasing/Verifying block	0	Toggle	0	1	No toggle	–	0
Erase/Blank Check Suspend	Erasing/Verifying block	1	No Toggle	0	–	Toggle	–	Hi-Z
	Non-erasing/Verifying block	Data read as normal					–	Hi-Z
Erase/Blank Check Error	Good block address	0	Toggle	1	1	No toggle	–	Hi-Z
	Faulty Block address	0	Toggle	1	1	Toggle	–	Hi-Z

1. Unspecified data bits should be ignored.
2. $\overline{DQ7}$ for Buffer Program is related to the last address location loaded.

Figure 14. Data polling flow chart

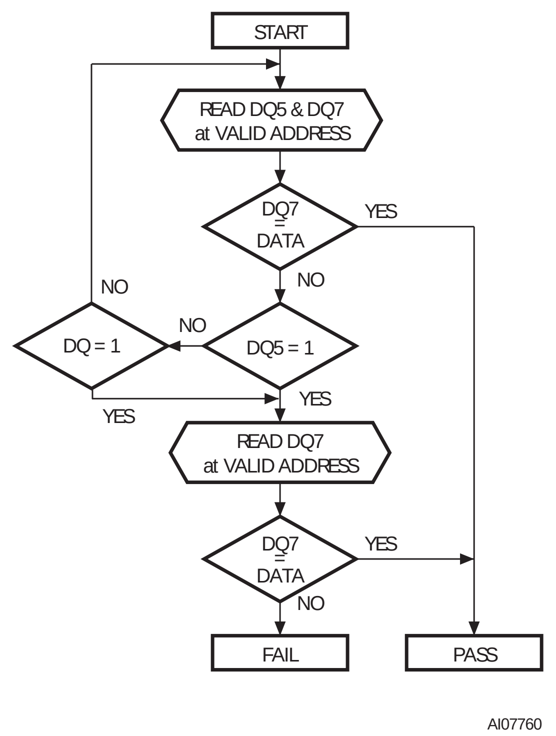


Figure 15. Toggle flow chart

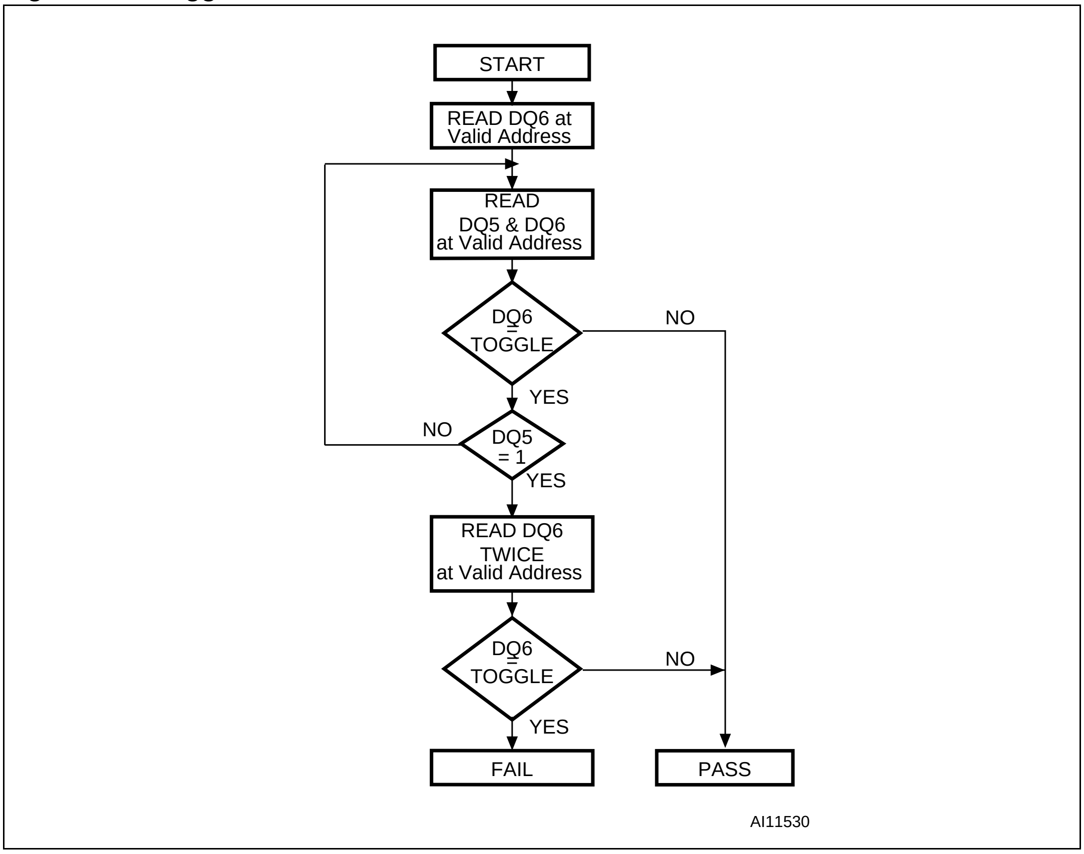
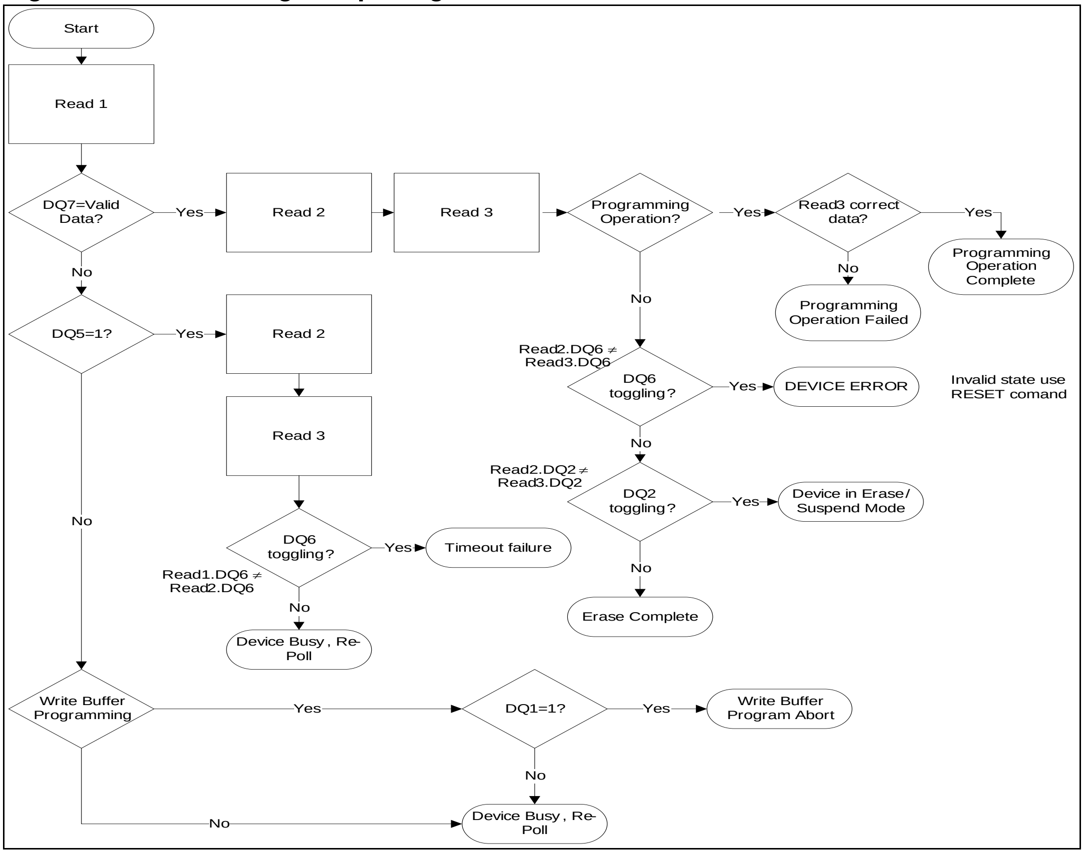


Figure 16. Status Register polling flow chart



8 Maximum Ratings

Stressing the device above the rating listed in *Table 18: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Refer also to the relevant quality documents from Numonyx.

Table 18. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature under bias	–40	85	°C
T_{STG}	Storage temperature	–65	125	°C
V_{IO}	Input or output voltage(1)(2)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage(1)(2)	–2	5.6	V
V_{CCQ}	Input/output supply voltage(1)(2)	–2	5.6	V
V_{PPH}(3)	Program voltage(1)(2)	–2	14.5	V

1. Minimum voltage may undershoot to –2 V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} + 2 V during transition and for less than 20ns during transitions.
3. V_{PPH} must not remain at 12 V for more than a cumulative total of 80hrs.

9 DC and AC Parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 19: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 19. Operating and AC measurement conditions

Parameter	Min	Max	Unit
V_{CC} supply voltage	2.7	3.6	V
V_{CCQ} supply voltage ($V_{CCQ} \leq V_{CC}$)	1.7	3.6	V
V_{PP} supply voltage	-0.6	12.5	V
Ambient operating temperature	– 40	85	°C
Load capacitance (C_L)	30		pF
Input rise and fall times	-	2.5	ns
Input pulse voltages	0 to V_{CCQ}		V
Input and output timing ref. voltages	$V_{CCQ}/2$		V

Figure 17. AC measurement load circuit

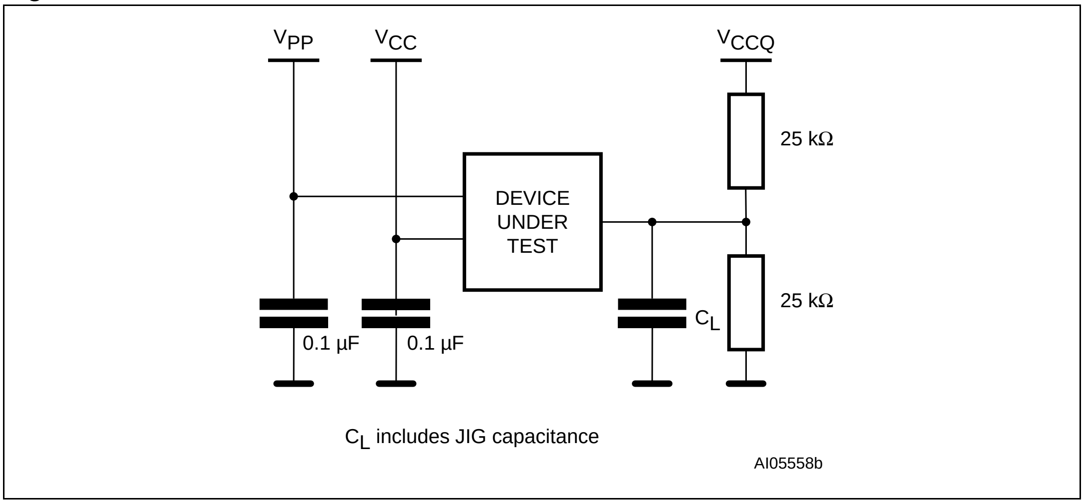


Figure 18. AC measurement I/O waveform

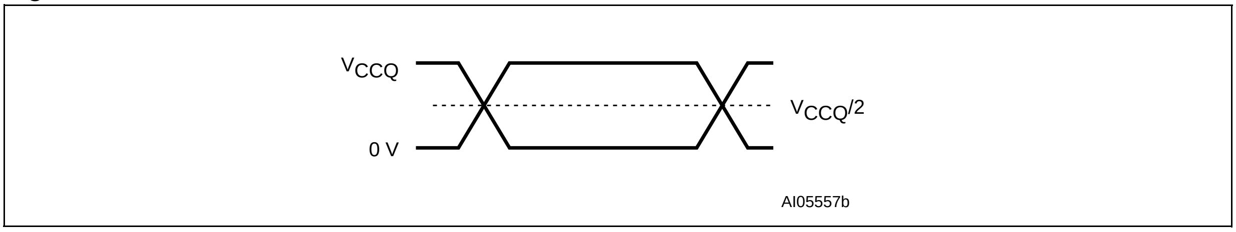


Table 20. Power-up wait timings

Symbol	Alt.	Parameter	Limit	Value	Unit
$t_{VCHVCQH}$	-	V_{CC}(1) High to V_{CCQ}(1) High	Min	0	µs
t_{VCHPH}(2)	t_{VCS}	V_{CC} High to rising edge of RST#	Min	60	µs
t_{VCQHPH}(2)	t_{VIOS}	V_{CCQ} High to rising edge of RST#	Min	0	µs
t_{PHEL}	t_{RH}	RST# High to Chip Enable Low	Min	50	ns
t_{PHWL}	-	RST# High to Write Enable Low	Min	150	ns

1. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.
2. If RST# is not stable for t_{VCHRH} or t_{VCQHRH}, the device does not permit any Read and Write operations and a hardware reset is required.

Figure 19. Power-up wait timings

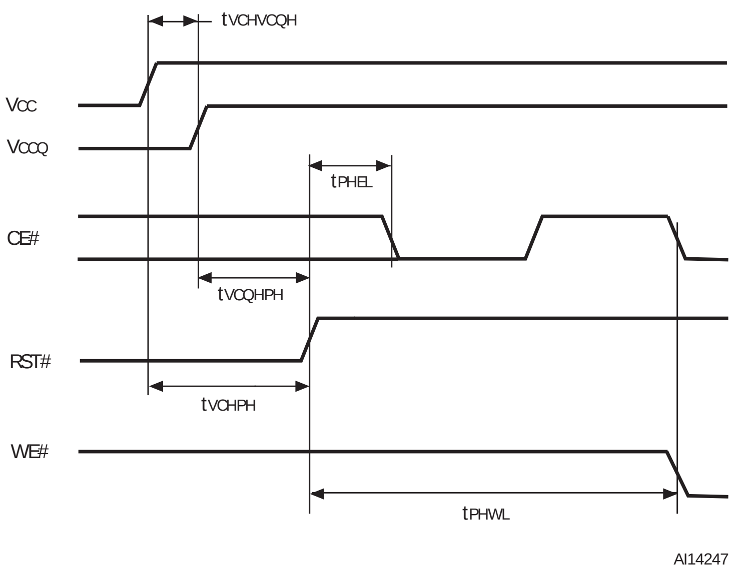


Table 21. Device capacitance[(1)]

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	2	7	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	2	5	pF

1. Sampled only, not 100% tested.

Table 22. DC characteristics

Symbol	Parameter		Test condition		Min	Typ	Max	Unit
I_{LI}[(1)]	Input leakage current		0 V ≤ V_{IN} ≤ V_{CC}		-	-	±1	µA
I_{LO}	Output leakage current		0 V ≤ V_{OUT} ≤ V_{CC}		-	-	±1	µA
I_{CC1}	Read current	Random Read	CE# = V_{IL}, OE# = V_{IH}, f = 5 MHz		-	20	25	mA
		Page Read	CE# = V_{IL}, OE# = V_{IH}, f = 13 MHz		-	12	16	mA
I_{CC2}	Supply current (Standby)	128-Mbit	CE# = V_{CCQ} ± 0.2V RST# = V_{CCQ} ± 0.2V		-	50	120	µA
		64-Mbit			-	35	120	
		32-Mbit			-	35	120	
I_{CC3}[(2)]	Supply current (Program/Erase/Blank Check)		Program/Erase controller active	V_{PP}/WP# = V_{IL} or V_{IH}	-	35	50	mA
				V_{PP}/WP#=V_{PPH}	-	26	33	mA
I_{PP1}	Vpp Current	Read	V_{PP}/WP# ≤ V_{CC}		-	2	15	µA
		Standby	V_{PP}/WP# ≤ V_{CC}		-	0.2	5	µA
I_{PP2}		Reset	RST# = V_{SS} ± 0.2 V		-	0.2	5	µA
I_{PP3}		Program operation ongoing	V_{PP}/WP# = 12 V ± 5%		-	5	10	mA
			V_{PP}/WP# = V_{CC}		-	0.05	0.10	mA
I_{PP4}		Erase operation ongoing	V_{PP}/WP# = 12 V ± 5%		-	5	10	mA
			V_{PP}/WP# = V_{CC}		-	0.05	0.10	mA
V_{IL}	Input Low voltage		V_{CC} ≥ 2.7 V		–0.5	-	0.8	V
V_{IH}	Input High voltage		V_{CC} ≥ 2.7 V		2	-	V_{CCQ}+0.5	V
V_{OL}	Output Low voltage		I_{OL} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$		-	-	0.2	V
V_{OH}	Output High voltage		I_{OH} = -100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$		V_{CCQ}–0.2	-	-	V
V_{PPLK}	V_{PP} Lock-Out voltage		-		-	-	0.4	V
V_{PPH}	Voltage for V_{PP}/WP# Program acceleration		-		11.5	-	12.5	V
V_{PPL}	V_{PP} logic level				2.7	-	3.6	V
V_{LKO}[(2)]	Program/Erase lockout supply voltage		-		2.3	-	-	V

1. The maximum input leakage current is ±5 µA on the V_{PP}/WP# pin.
2. Sampled only, not 100% tested.

Figure 20. Random Read AC waveforms (8-bit mode)

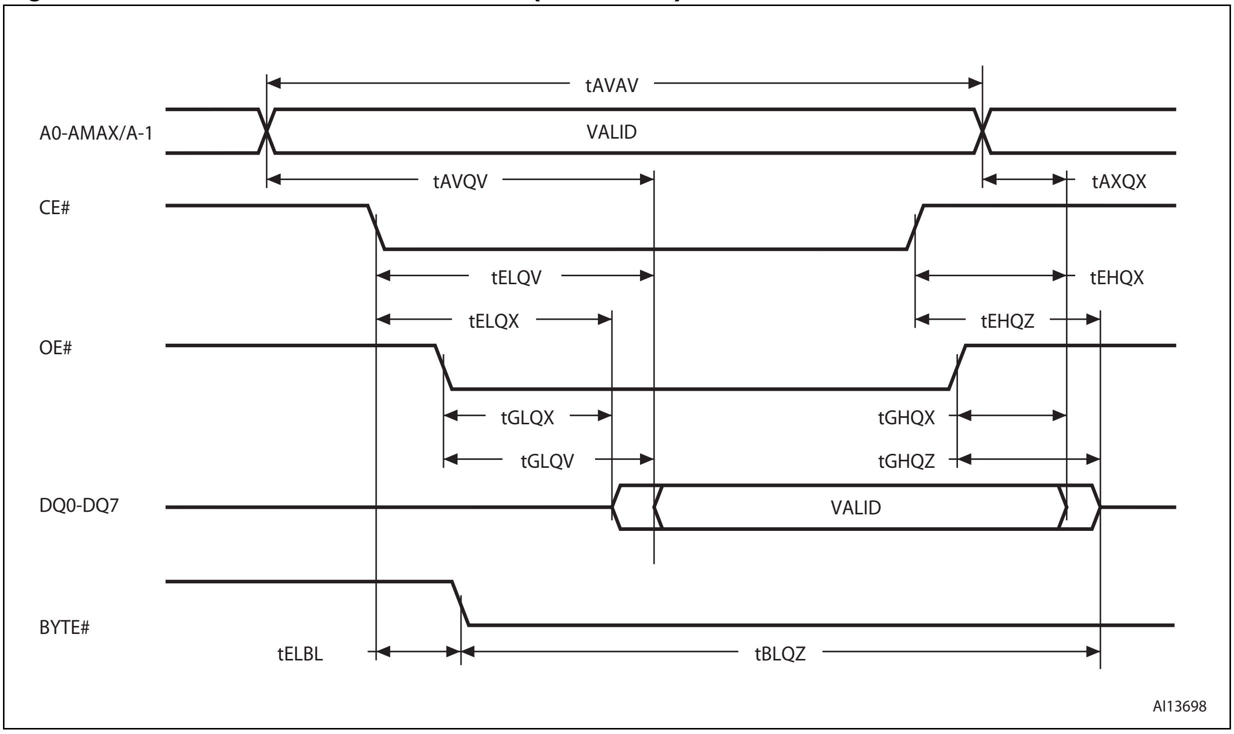


Figure 21. Random Read AC waveforms (16-bit mode)

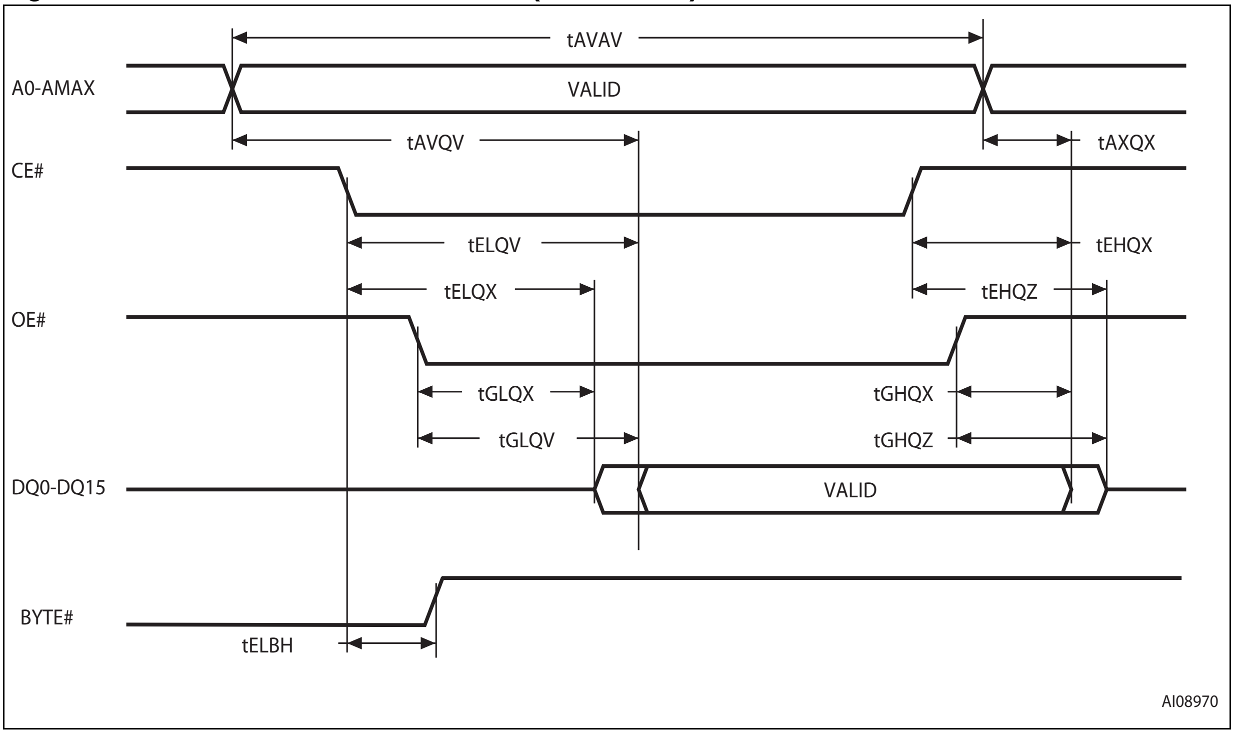
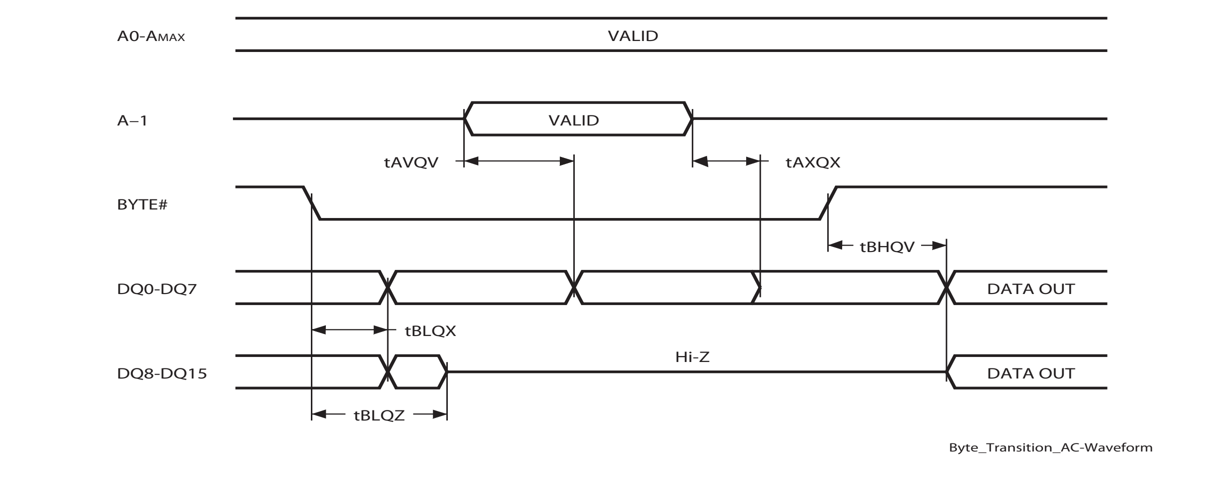


Figure 22. Byte Transition AC waveform



1. CE# and OE# are V_{IL}.

Figure 23. Page Read AC waveforms (16-bit mode)

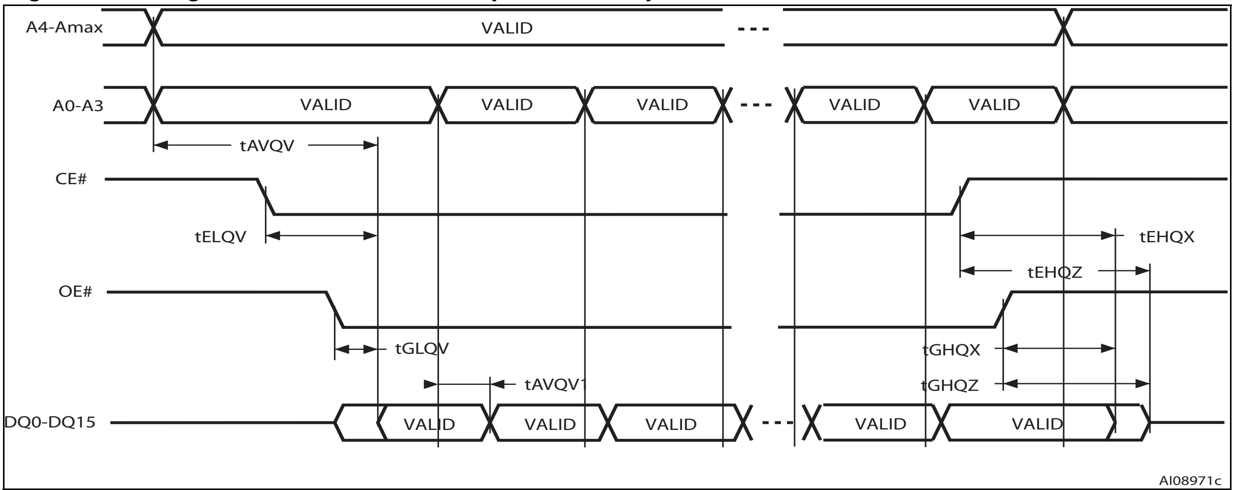


Table 23. Read AC characteristics (Sheet 1 of 2)

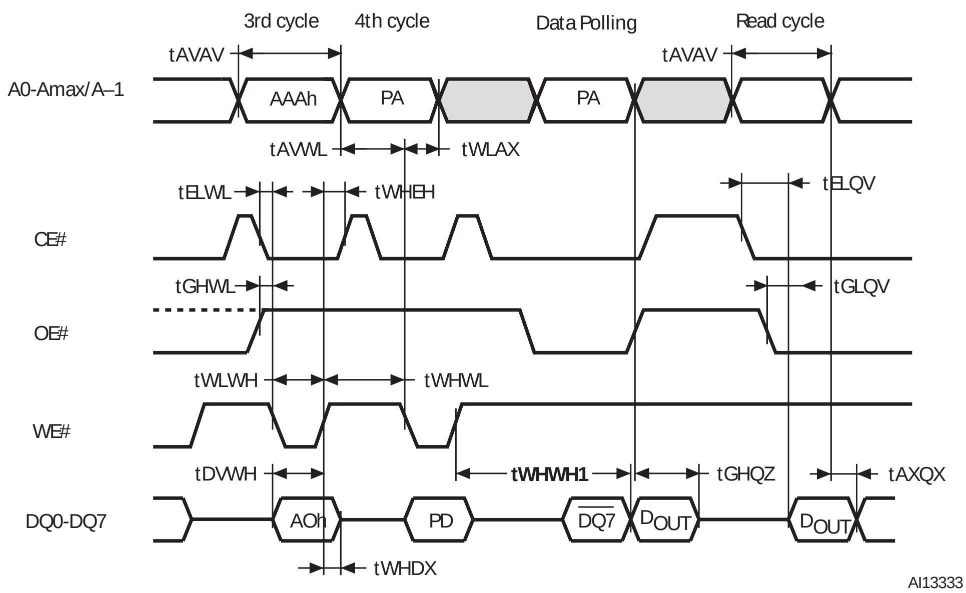
Symbol	Alt.	Parameter	Test condition	Limit	BGA	TSOP	Unit
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	CE# = V_{IL}, OE# = V_{IL}	Min	60	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	CE# = V_{IL}, OE# = V_{IL}	Max	60	70	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	CE# = V_{IL}, OE# = V_{IL}	Max	25		ns
t_{ELQX}(1)	t_{LZ}	Chip Enable Low to Output Transition	OE# = V_{IL}	Min	0		ns
t_{ELQV}	t_E	Chip Enable Low to Output Valid	OE# = V_{IL}	Max	60	70	ns
t_{GLQX}(1)	t_{OLZ}	Output Enable Low to Output Transition	CE# = V_{IL}	Min	0		ns

Table 23. Read AC characteristics (Sheet 2 of 2)

Symbol	Alt.	Parameter	Test condition	Limit	BGA	TSOP	Unit
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	CE# = V_{IL}	Max	25		ns
t_{EHQZ}(1)	t_{HZ}	Chip Enable High to Output Hi-Z	OE# = V_{IL}	Max	20		ns
t_{GHQZ}(1)	t_{DF}	Output Enable High to Output Hi-Z	CE# = V_{IL}	Max	15		ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition	-	Min	0		ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to BYTE# Low or High	-	Max	10		ns
t_{BLQV}	t_{FLQV}	BYTE# Low to Output Valid	-	Max	1		µs
t_{BHQV}	t_{FHQV}	BYTE# High to Output Valid	-	Max	1		µs
t_{BLQZ}	t_{FLQZ}	BYTE# Low to Output in high Z	-	Max	1		µs

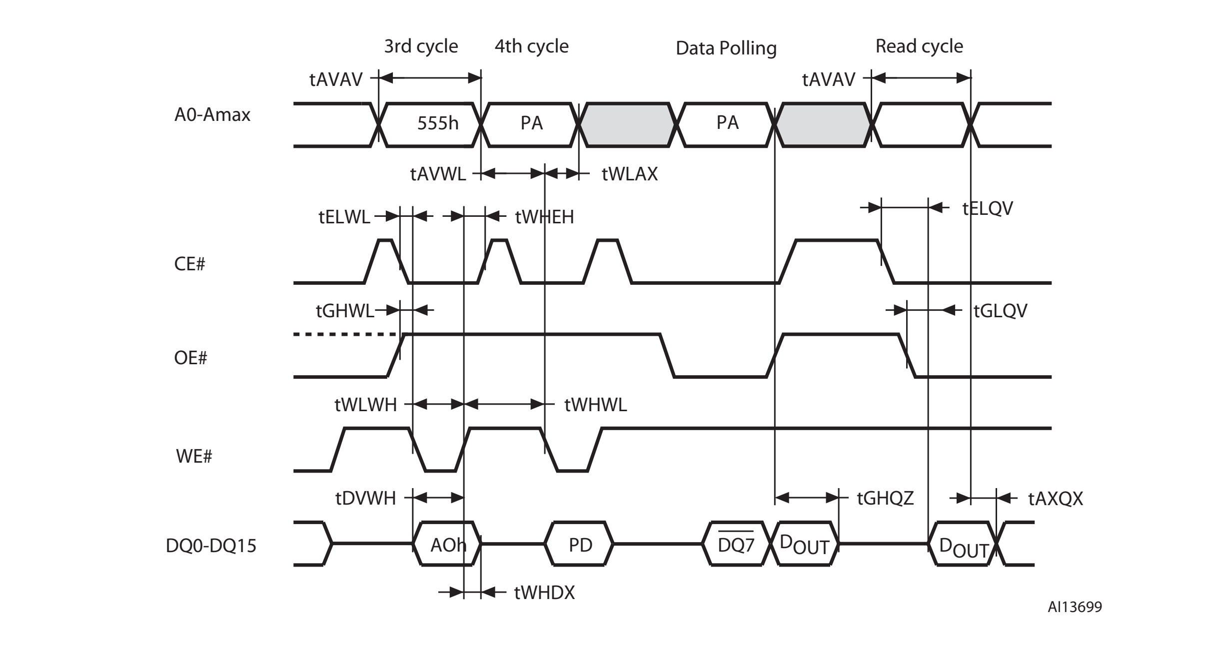
1. Sampled only, not 100% tested.

Figure 24. Write Enable Controlled Program waveforms (8-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Figure 25. Write Enable Controlled Program waveforms (16-bit mode)



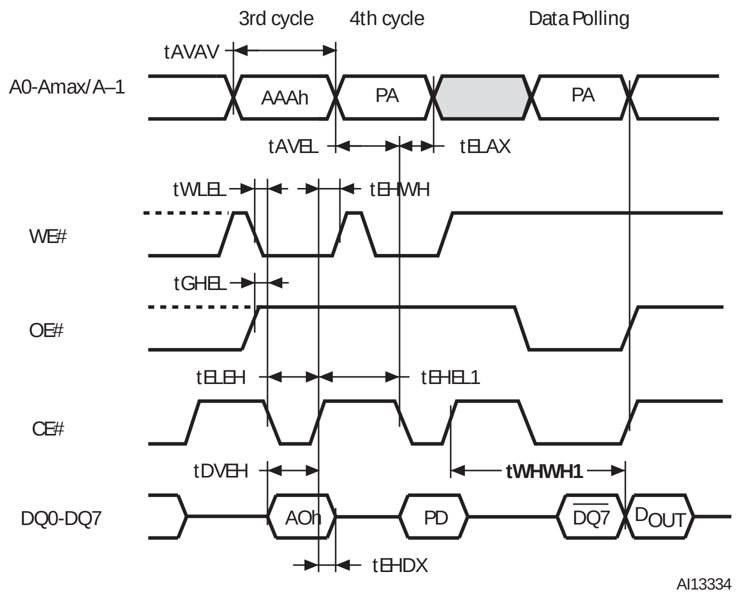
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Table 24. Write AC characteristics, Write Enable Controlled

Symbol	Alt	Parameter	Limit	BGA	TSOP	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	60	70	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	35		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	30		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45		ns
t_{GHWL}	-	Output Enable High to Write Enable Low	Min	0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0		ns
t_{WHRL}(1)	t_{BUSY}	Program/Erase Valid to RY/BY# Low	Max	90		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	60		µs

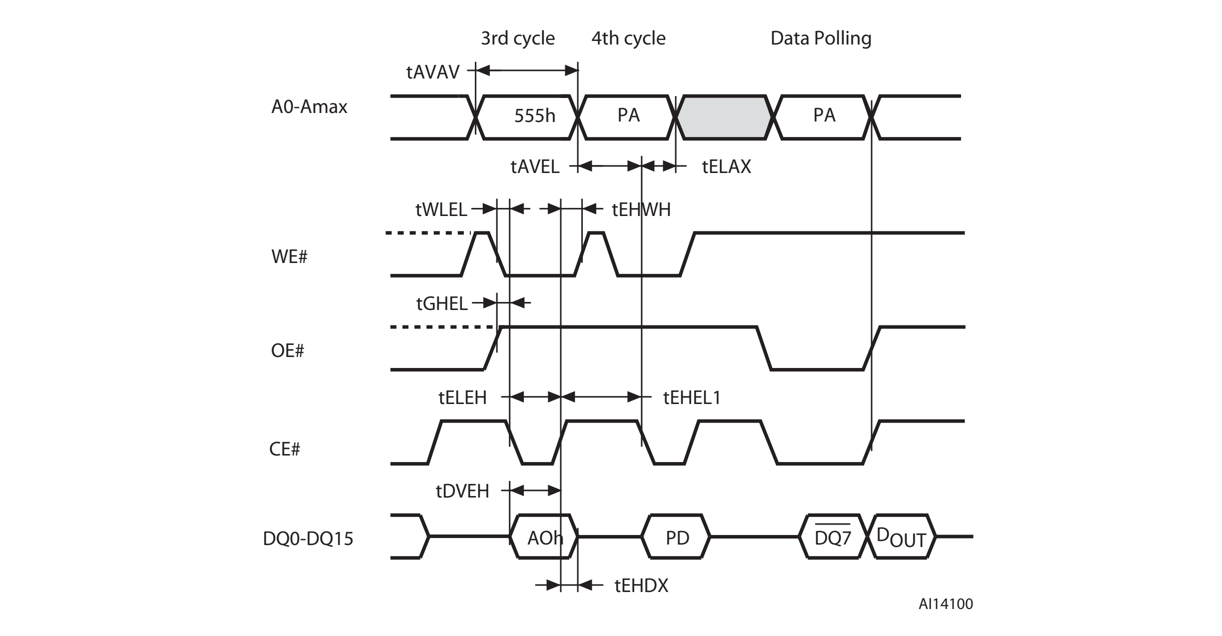
1. Sampled only, not 100% tested.

Figure 26. Chip Enable Controlled Program waveforms (8-bit mode)



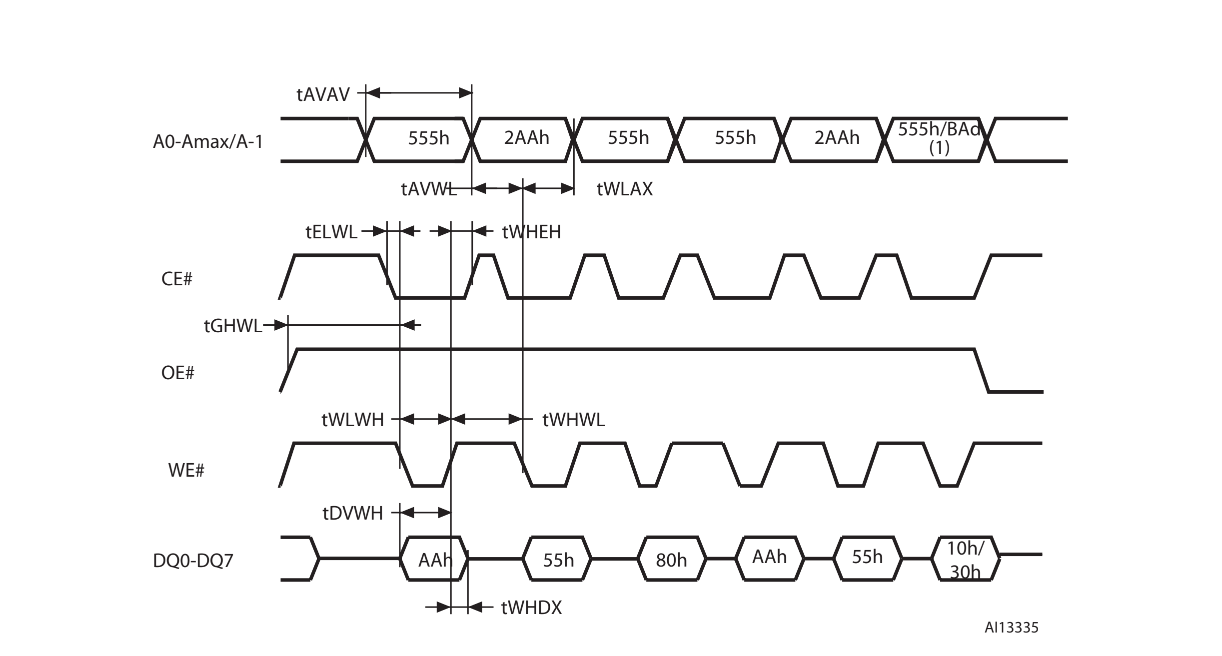
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Figure 27. Chip Enable Controlled Program waveforms (16-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of Status Register Data Polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.2.1: Data Polling bit (DQ7)*).
4. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Figure 28. Chip/Block Erase waveforms (8-bit mode)



1. For a Chip Erase command, addresses and data are 555h and 10h, respectively, while they are BAd and 30h for a Block Erase command.
2. BAd is the block address.
3. See *Table 24: Write AC characteristics, Write Enable Controlled*, *Table 25: Write AC characteristics, Chip Enable Controlled* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Table 25. Write AC characteristics, Chip Enable Controlled

Symbol	Alt.	Parameter	Limit	BGA	TSOP	Unit
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	60	70	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	35		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	30		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45		ns
t_{GHEL}	-	Output Enable High Chip Enable Low	Min	0		ns

Figure 29. Reset AC waveforms (no program/erase in progress)

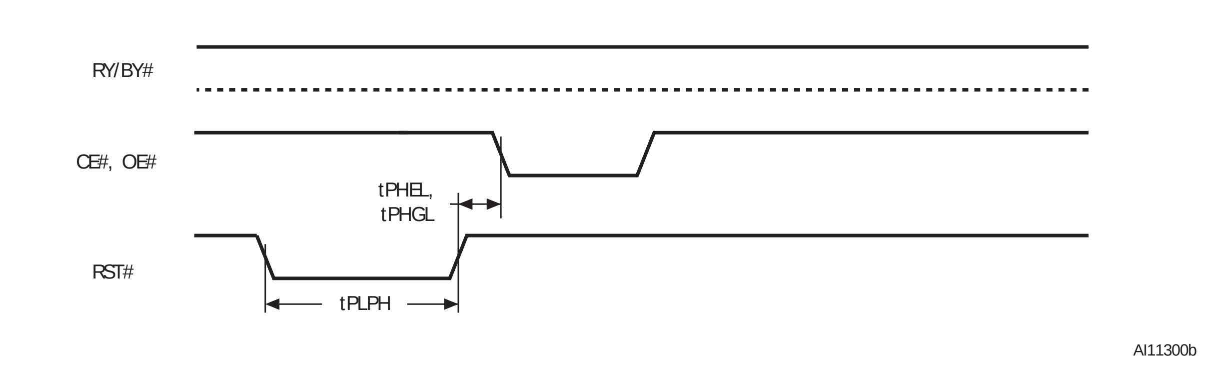


Figure 30. Reset AC waveforms (during program/erase operation)

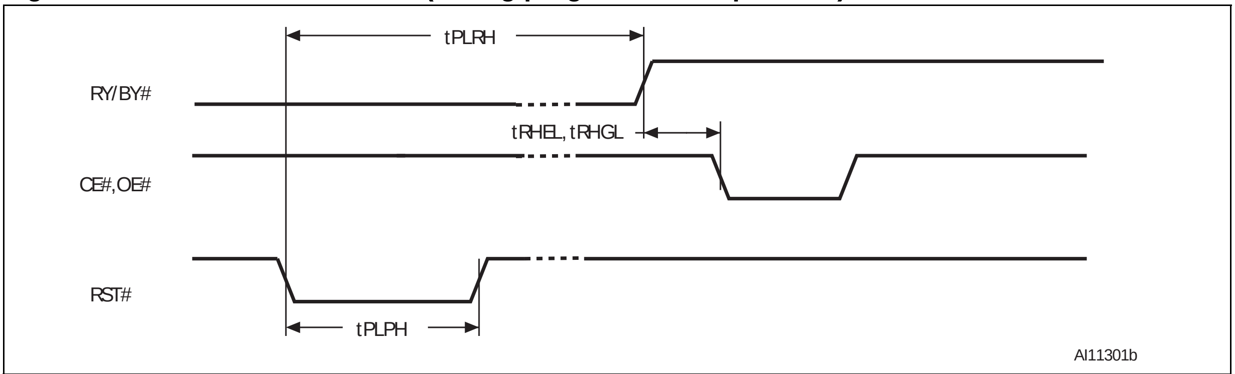


Table 26. Reset AC characteristics

Symbol	Alt.	Parameter	Min	Max	Unit
t_{PLRH}(1)	t_{READY}	RST# Low to Read mode, during Program or Erase	-	25	µs
t_{PLPH}	t_{RP}	RST# Pulse width	100	-	ns
t_{PHEL}, t_{PHGL}(1)	t_{RH}	RST# High to Chip Enable Low, Output Enable Low	50	-	ns
-	t_{RPD}	RST# Low to Standby mode, during Read mode	10	-	µs
		RST# Low to Standby mode, during Program or Erase	50	-	µs
t_{RHWL}, t_{RHEL}, t_{RHGL}(1)	t_{RB}	RY/BY# High to Write Enable Low, Chip Enable Low, Output Enable Low	0	-	ns

1. Sampled only, not 100% tested.

Figure 31. Accelerated program timing waveforms

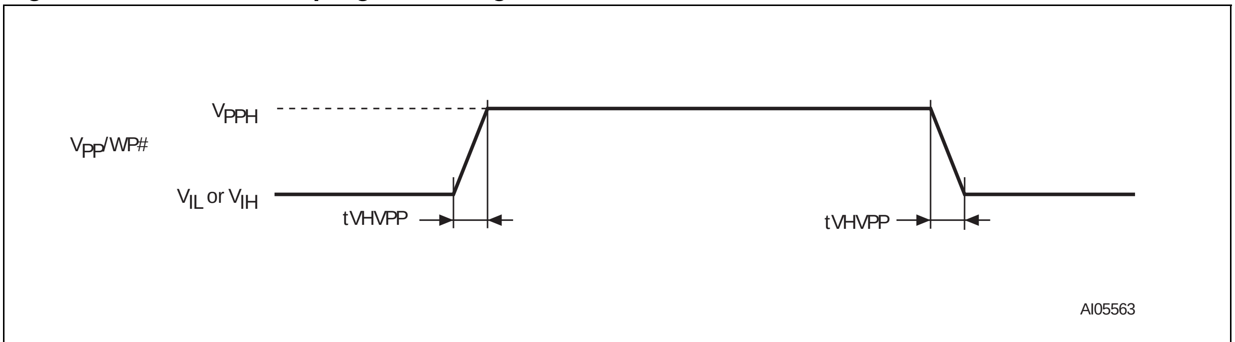
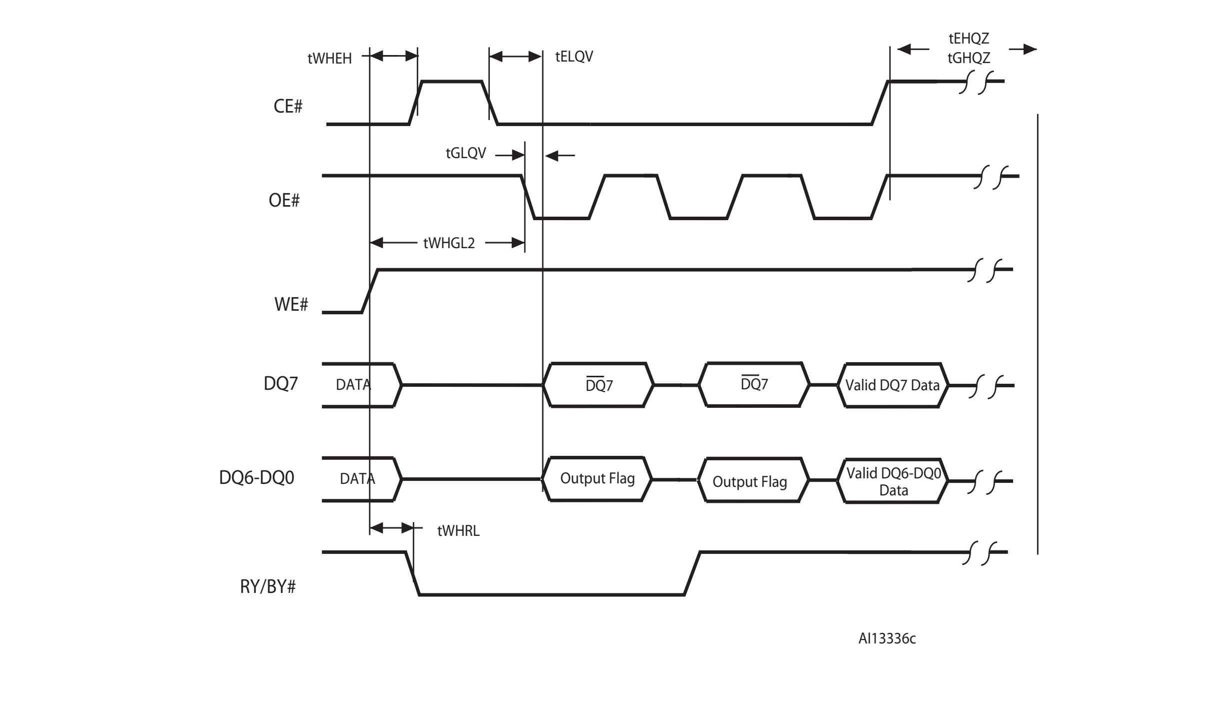
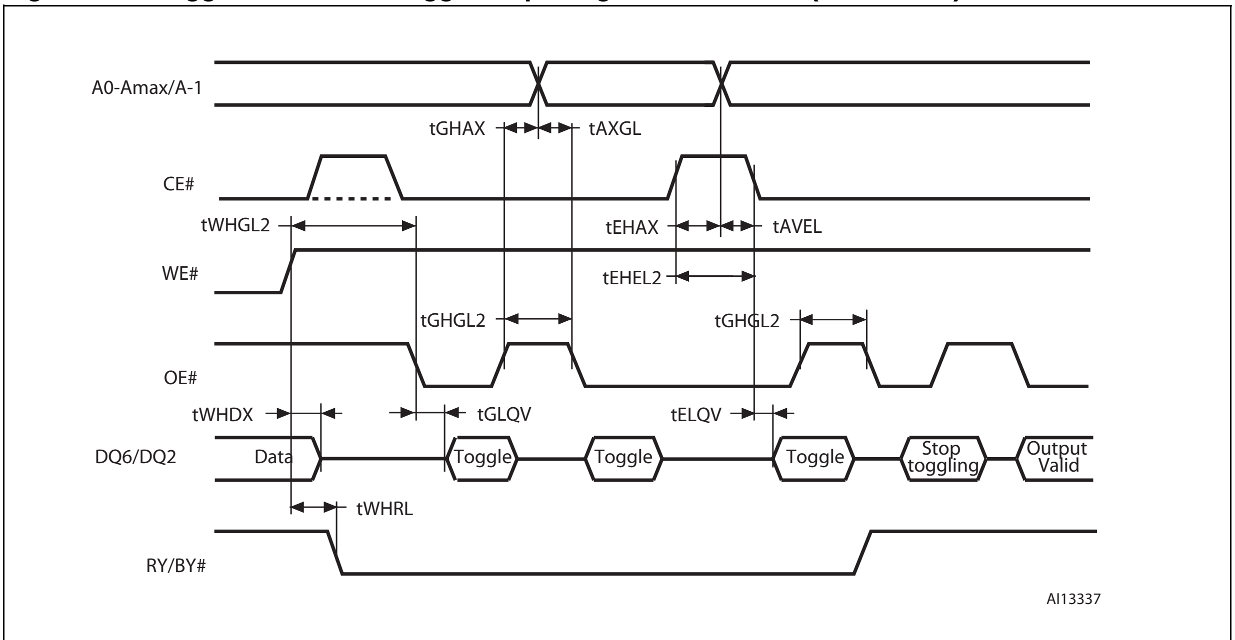


Figure 32. Data polling AC waveforms



1. DQ7 returns valid data bit when the ongoing Program or Erase command is completed.
2. See *Table 27: Accelerated Program and Data Polling/Data Toggle AC characteristics* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Figure 33. Toggle/Alternative Toggle bit polling AC waveforms (8-bit mode)



1. DQ6 stops toggling when the ongoing Program or Erase command is completed. DQ2 stops toggling when the in-progress Chip Erase or Block Erase command is completed.
2. See *Table 27: Accelerated Program and Data Polling/Data Toggle AC characteristics* and *Table 23: Read AC characteristics (Sheet of 2)* for details on the timings.

Table 27. Accelerated Program and Data Polling/Data Toggle AC characteristics

Symbol	Alt	Parameter	Min	Max	Unit
t_{VHVPP}	-	V_{PP}/WP# raising or falling time	250	-	ns
t_{VHHWH}	-	Valid V_{HH} on V_{PP}/WP# to WE# high	50	-	ns
t_{AXGL}	t_{ASO}	Address setup time to Output Enable Low during Toggle bit polling	15	-	ns
t_{GHAX}, t_{EHAX}	t_{AHT}	Address hold time from Output Enable during Toggle bit polling	0	-	ns
t_{EHEL2}	t_{EPH}	Chip Enable High during Toggle bit polling	20	-	ns
t_{WHGL2}, t_{GHGL2}	t_{OEH}	Output Hold time during Data and Toggle bit polling	20	-	ns
t_{WHRL}	t_{BUSY}	Program/Erase Valid to RY/BY# Low	-	90	ns

10 Programming and Erase Performance

Table 28. Programming and Erase Performance

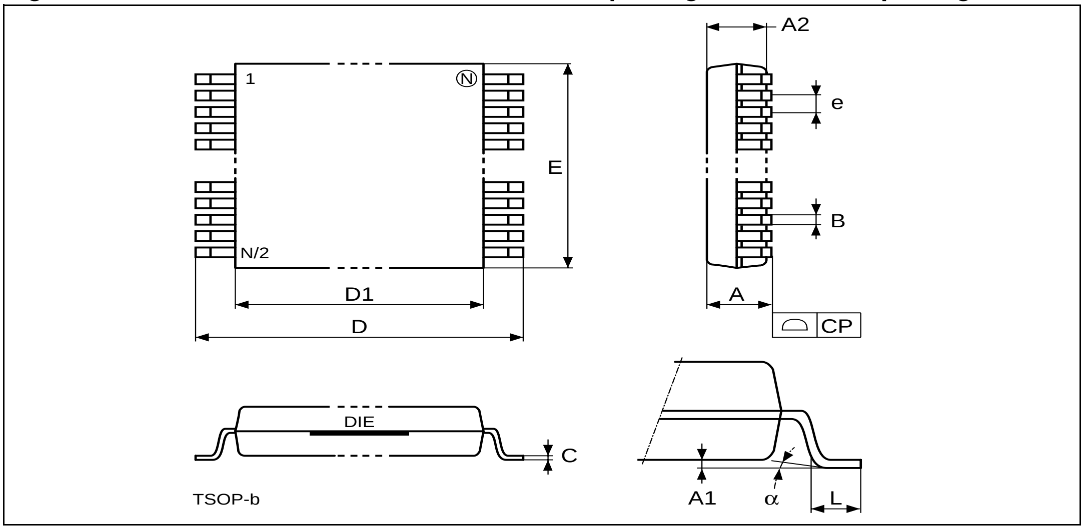
Parameter		Buffer Size	Byte	Word	Min	Typ(1)(2)	Max(2)	Unit
Block Erase		-	-	-	-	0.5	4	s
Erase Suspend latency		-	-	-	-	20	25	µs
Block Erase time-out		-	-	-	50	-	-	µs
Byte Program	Single Byte Program	-	-	-	-	15	175	µs
	Double / Quadruple / Octuple Byte Program	-	-	-	-	10	200	µs
	Byte Write to Buffer Program	32	32	-	-	70	200	µs
		64	64	-	-	85	200	
		256	256	-	-	160	710	
	Effective Write to Buffer Program per Byte	32	1	-	-	2.19	6.25	µs
		64	1	-	-	1.33	3.125	
		256	1	-	-	0.625	2.77	
Word Program	Single Word Program	-	-	-	-	15	175	µs
	Word Write to Buffer Program	16	-	16	-	70	200	µs
		32	-	32	-	85	200	
		128	-	128	-	160	710	
		256	-	256	-	284	1280	
	Full Buffer Program With V_{PPH}	256	-	256	-	160	800	µs
	Effective Write to Buffer Program per Word	16	-	1	-	4.375	12.5	µs
		32	-	1	-	2.66	6.25	
		128	-	1	-	1.25	5.55	
		256	-	1	-	1.11	5	
	Effective Full Buffer Program per Word With V_{PPH}	256	-	1	-	0.625	3.125	µs
Program Suspend latency		-	-	-	-	20	25	µs
Blank Check		-	-	-	-	3.2	-	ms
Program/Erase cycles (per block)		-	-	-	100,000	-	-	Cycles

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.

11 Package Mechanical Specifications

Numonyx offers these devices in both lead-free and leaded packages. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 34. TSOP56 – 56 lead thin small-outline package,14 x 20 mm, package outline



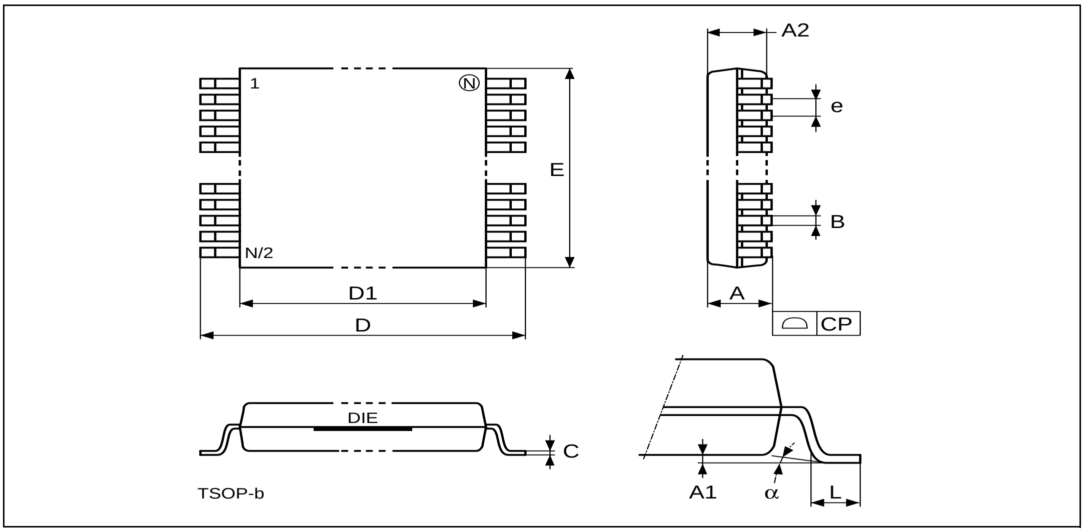
1. Drawing is not to scale.

Table 29. TSOP56 – 56 lead thin small-outline package, 14 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.20	–	–	0.047
A1	–	0.05	–	–	0.002	–
A2	0.995	0.965	1.025	0.039	0.038	0.040
B(1)	0.22	0.17	0.27	0.0087	0.0067	0.0106
C	0.125	0.115	0.135	0.0049	0.0045	0.0053
CP	–	–	0.10	–	–	0.004
E	14.00	13.80	14.20	0.551	0.543	0.559
D	20.00	19.80	20.20	0.787	0.780	0.795
D1	18.40	18.20	18.60	0.724	0.717	0.732
e	0.50	–	–	0.020	–	–
L	0.60	0.50	0.70	0.024	0.020	0.028
α	3^o	0^o	5^o	3^o	0^o	5^o
N	56					

1. For legacy lead width, 0.15mm (Typ), 0.10mm (Min), 0.20mm (Max).

Figure 35. TSOP48 – 48 lead thin small-outline package, 12 x 20 mm, package outline

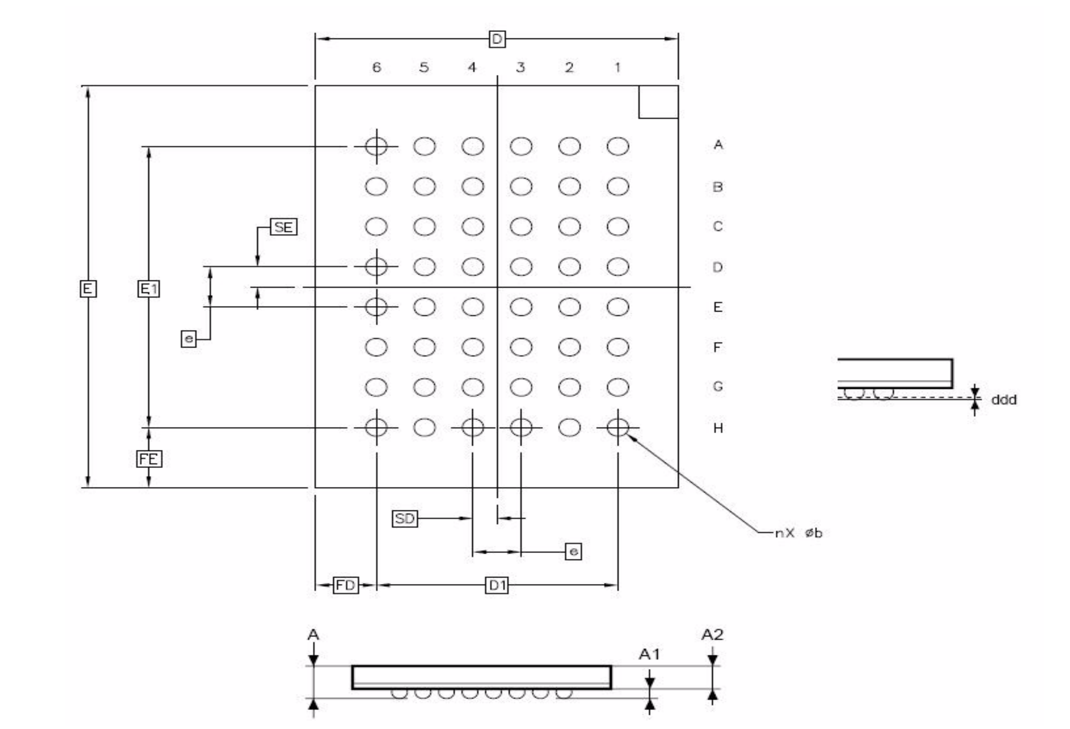


1. Drawing is not to scale.

Table 30. TSOP48 – 48 lead thin small-outline package, 12 x 20 mm, package mechanical data

Symbol	millimeters		
	Typ	Min	Max
A	–	–	1.20
A1	0.10	0.05	0.15
A2	1.00	0.95	1.05
B	0.22	0.17	0.27
C	–	0.10	0.21
CP	–	–	0.10
E	12.00	11.90	12.10
D	20.00	19.80	20.20
D1	18.40	18.30	18.50
e	0.50	–	–
L	0.60	0.50	0.70
α	3°	0°	5°
N	48		

Figure 36. BGA48 6 x 8 mm - 6 x 8 active ball array, package outline

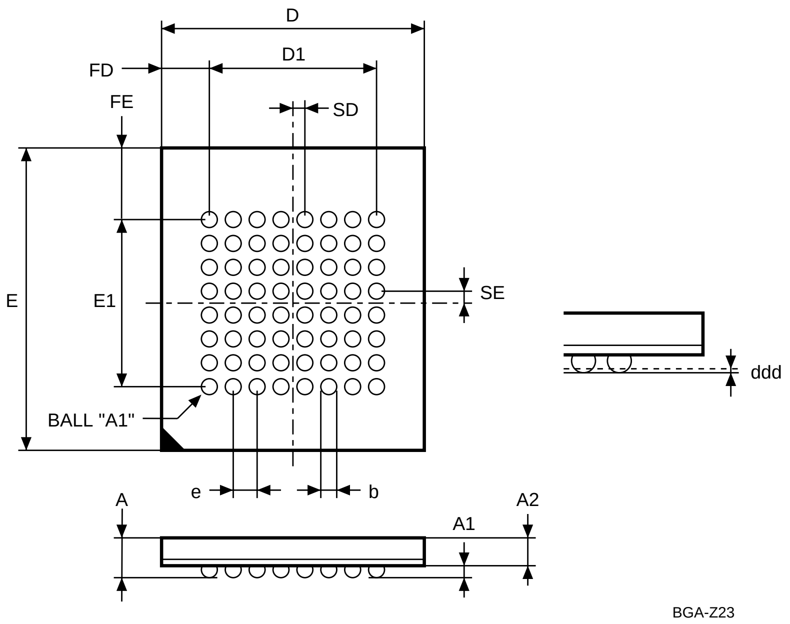


1. Drawing is not to scale.
2. Drawing is bottom view.

Table 31. BGA48 6 x 8 mm - 6 x 8 active ball array, package mechanical data

Symbol	millimeters		
	Typ	Min	Max
A	–	–	1.00
A1	–	0.20	–
A2	0.64	–	–
b	0.35	0.30	0.40
D	6.00	5.90	6.10
D1	4.00	–	–
e	0.80	–	–
E	8.00	7.90	8.10
E1	5.60	–	–
FD	1.00	–	–
FE	1.20	–	–
SD	0.40	–	–
SE	0.40	–	–
ddd	–	–	0.10

Figure 37. Fortified BGA64 11 x 13 mm - 8 x 8 active ball array, package outline



1. Drawing is not to scale.
2. Drawing is bottom view.

Table 32. Fortified BGA64 11 x 13 mm - 8 x 8 active ball array, package mechanical data

Symbol	millimeters		
	Typ	Min	Max
A	–	–	1.40
A1	0.49	0.40	–
A2	0.80	–	–
b	0.60	0.55	0.65
D	11.00	10.90	11.10
D1	7.00	–	–
ddd	–	–	0.10
e	1.00	–	–
E	13.00	12.90	13.10
E1	7.00	–	–
FD	2.00	–	–
FE	3.00	–	–
SD	0.50	–	–
SE	0.50	–	–

12 Ordering Information

Table 33. Ordering information scheme

Example: RC 28F 128 M29EW H *

Package

JS = TSOP56: 14 x 20 mm, lead free, RoHS compliant, halogen free

PC = Fortified BGA64: 11 x 13 mm, lead free, RoHS compliant, halogen free

RC = Fortified BGA64: 11 x 13 mm, leaded

JR = TSOP48: 12 x 20 mm, lead free, RoHS compliant, halogen free

PZ = BGA48: 6 x 8 mm, lead free, RoHS compliant, halogen free

Product Line

28F= NOR Parallel Interface

Device Density

128=128-Mbit

064=64-Mbit

032=32-Mbit

Device Type

M29EW = 3V core, page flash memory

Device function

H = uniform block, highest block protected by V_{PP}/WP#

L = uniform block, lowest block protected by V_{PP}/WP#

B = bottom boot, bottom two blocks protected by V_{PP}/WP#

T = top boot, top two blocks protected by V_{PP}/WP#

Device features

*= The last digit is randomly assigned to cover packing media and/or features or other specific configuration.

Note: *This product is also available with the Extended Memory Block Numonyx pre-locked. For further details and ordering information contact your nearest Numonyx sales office.*

Devices are shipped from Numonyx factory with the memory content bits erased to ‘1’. For a list of available options (package, High/Low protect, etc.) or for further information on any aspect of the device, please contact your nearest Numonyx Sales Office.

Table 34. Valid Combinations of SBC M29EW Part Numbers

128-Mbit	64-Mbit	32-Mbit
JS28F128M29EWH*	JS28F064M29EWH*	JR28F032M29EWH*
JS28F128M29EWL*	JS28F064M29EWL*	JR28F032M29EWL*
PC28F128M29EWH*	JS28F064M29EWB*	JR28F032M29EWB*
PC28F128M29EWL*	JS28F064M29EWT*	JR28F032M29EWT*
RC28F128M29EWH*	JR28F064M29EWH*	PZ28F032M29EWH*
RC28F128M29EWL*	JR28F064M29EWL*	PZ28F032M29EWL*
-	JR28F064M29EWB*	PZ28F032M29EWB*
-	JR28F064M29EWT*	PZ28F032M29EWT*
-	PC28F064M29EWH*	-
-	PC28F064M29EWL*	-
-	PC28F064M29EWB*	-
-	PC28F064M29EWT*	-
-	PZ28F064M29EWH*	-
-	PZ28F064M29EWL*	-
-	PZ28F064M29EWB*	-
-	PZ28F064M29EWT*	-

Note: *For further information on ordering products or for product part numbers, go to: http://www.numonyx.com/en-US/MemoryProducts/Pages/PartNumberLookup.aspx.*

Appendix A 128-Mbit Memory Address Table

Table 35. Block Address Table(1)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
0	128 / 64	0000000-001FFFF	0000000-000FFFF
1	128 / 64	0020000-003FFFF	0010000-001FFFF
2	128 / 64	0040000-005FFFF	0020000-002FFFF
3	128 / 64	0060000-007FFFF	0030000-003FFFF
4	128 / 64	0080000-009FFFF	0040000-004FFFF
5	128 / 64	00A0000-00BFFFF	0050000-005FFFF
6	128 / 64	00C0000-00DFFFF	0060000-006FFFF
7	128 / 64	00E0000-00FFFFF	0070000-007FFFF
8	128 / 64	0100000-011FFFF	0080000-008FFFF
9	128 / 64	0120000-013FFFF	0090000-009FFFF
10	128 / 64	0140000-015FFFF	00A0000-00AFFFF
11	128 / 64	0160000-017FFFF	00B0000-00BFFFF
12	128 / 64	0180000-019FFFF	00C0000-00CFFFF
13	128 / 64	01A0000-01BFFFF	00D0000-00DFFFF
14	128 / 64	01C0000-01DFFFF	00E0000-00EFFFF
15	128 / 64	01E0000-01FFFFF	00F0000-00FFFFF
16	128 / 64	0200000-021FFFF	0100000-010FFFF
17	128 / 64	0220000-023FFFF	0110000-011FFFF
18	128 / 64	0240000-025FFFF	0120000-012FFFF
19	128 / 64	0260000-027FFFF	0130000-013FFFF
20	128 / 64	0280000-029FFFF	0140000-014FFFF
21	128 / 64	02A0000-02BFFFF	0150000-015FFFF
22	128 / 64	02C0000-02DFFFF	0160000-016FFFF
23	128 / 64	02E0000-02FFFFF	0170000-017FFFF
24	128 / 64	0300000-031FFFF	0180000-018FFFF
25	128 / 64	0320000-033FFFF	0190000-019FFFF
26	128 / 64	0340000-035FFFF	01A0000-01AFFFF
27	128 / 64	0360000-037FFFF	01B0000-01BFFFF
28	128 / 64	0380000-039FFFF	01C0000-01CFFFF
29	128 / 64	03A0000-03BFFFF	01D0000-01DFFFF
30	128 / 64	03C0000-03DFFFF	01E0000-01EFFFF

Table 35. Block Address Table(1)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
31	128 / 64	03E0000-03FFFFF	01F0000-01FFFFF
32	128 / 64	0400000-041FFFF	0200000-020FFFF
33	128 / 64	0420000-043FFFF	0210000-021FFFF
34	128 / 64	0440000-045FFFF	0220000-022FFFF
35	128 / 64	0460000-047FFFF	0230000-023FFFF
36	128 / 64	0480000-049FFFF	0240000-024FFFF
37	128 / 64	04A0000-04BFFFF	0250000-025FFFF
38	128 / 64	04C0000-04DFFFF	0260000-026FFFF
39	128 / 64	04E0000-04FFFFF	0270000-027FFFF
40	128 / 64	0500000-051FFFF	0280000-028FFFF
41	128 / 64	0520000-053FFFF	0290000-029FFFF
42	128 / 64	0540000-055FFFF	02A0000-02AFFFF
43	128 / 64	0560000-057FFFF	02B0000-02BFFFF
44	128 / 64	0580000-059FFFF	02C0000-02CFFFF
45	128 / 64	05A0000-05BFFFF	02D0000-02DFFFF
46	128 / 64	05C0000-05DFFFF	02E0000-02EFFFF
47	128 / 64	05E0000-05FFFFF	02F0000-02FFFFF
48	128 / 64	0600000-061FFFF	0300000-030FFFF
49	128 / 64	0620000-063FFFF	0310000-031FFFF
50	128 / 64	0640000-065FFFF	0320000-032FFFF
51	128 / 64	0660000-067FFFF	0330000-033FFFF
52	128 / 64	0680000-069FFFF	0340000-034FFFF
53	128 / 64	06A0000-06BFFFF	0350000-035FFFF
54	128 / 64	06C0000-06DFFFF	0360000-036FFFF
55	128 / 64	06E0000-06FFFFF	0370000-037FFFF
56	128 / 64	0700000-071FFFF	0380000-038FFFF
57	128 / 64	0720000-073FFFF	0390000-039FFFF
58	128 / 64	0740000-075FFFF	03A0000-03AFFFF
59	128 / 64	0760000-077FFFF	03B0000-03BFFFF
60	128 / 64	0780000-079FFFF	03C0000-03CFFFF
61	128 / 64	07A0000-07BFFFF	03D0000-03DFFFF
62	128 / 64	07C0000-07DFFFF	03E0000-03EFFFF
63	128 / 64	07E0000-07FFFFF	03F0000-03FFFFF
64	128 / 64	0800000-081FFFF	0400000-040FFFF

Table 35. Block Address Table(1)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
65	128 / 64	0820000-083FFFF	0410000-041FFFF
66	128 / 64	0840000-085FFFF	0420000-042FFFF
67	128 / 64	0860000-087FFFF	0430000-043FFFF
68	128 / 64	0880000-089FFFF	0440000-044FFFF
69	128 / 64	08A0000-08BFFFF	0450000-045FFFF
70	128 / 64	08C0000-08DFFFF	0460000-046FFFF
71	128 / 64	08E0000-08FFFFF	0470000-047FFFF
72	128 / 64	0900000-091FFFF	0480000-048FFFF
73	128 / 64	0920000-093FFFF	0490000-049FFFF
74	128 / 64	0940000-095FFFF	04A0000-04AFFFF
75	128 / 64	0960000-097FFFF	04B0000-04BFFFF
76	128 / 64	0980000-099FFFF	04C0000-04CFFFF
77	128 / 64	09A0000-09BFFFF	04D0000-04DFFFF
78	128 / 64	09C0000-09DFFFF	04E0000-04EFFFF
79	128 / 64	09E0000-09FFFFF	04F0000-04FFFFF
80	128 / 64	0A00000-0A1FFFF	0500000-050FFFF
81	128 / 64	0A20000-0A3FFFF	0510000-051FFFF
82	128 / 64	0A40000-0A5FFFF	0520000-052FFFF
83	128 / 64	0A60000-0A7FFFF	0530000-053FFFF
84	128 / 64	0A80000-0A9FFFF	0540000-054FFFF
85	128 / 64	0AA0000-0ABFFFF	0550000-055FFFF
86	128 / 64	0AC0000-0ADFFFF	0560000-056FFFF
87	128 / 64	0AE0000-0AFFFFF	0570000-057FFFF
88	128 / 64	0B00000-0B1FFFF	0580000-058FFFF
89	128 / 64	0B20000-0B3FFFF	0590000-059FFFF
90	128 / 64	0B40000-0B5FFFF	05A0000-05AFFFF
91	128 / 64	0B60000-0B7FFFF	05B0000-05BFFFF
92	128 / 64	0B80000-0B9FFFF	05C0000-05CFFFF
93	128 / 64	0BA0000-0BBFFFF	05D0000-05DFFFF
94	128 / 64	0BC0000-0BDFFFF	05E0000-05EFFFF
95	128 / 64	0BE0000-0BFFFFF	05F0000-05FFFFF
96	128 / 64	0C00000-0C1FFFF	0600000-060FFFF
97	128 / 64	0C20000-0C3FFFF	0610000-061FFFF
98	128 / 64	0C40000-0C5FFFF	0620000-062FFFF

Table 35. Block Address Table(1)

Block Number	Block Size (Kbytes / Kwords)	x8 Address (HEX)	x16 Address (HEX)
99	128 / 64	0C60000-0C7FFFF	0630000-063FFFF
100	128 / 64	0C80000-0C9FFFF	0640000-064FFFF
101	128 / 64	0CA0000-0CBFFFF	0650000-065FFFF
102	128 / 64	0CC0000-0CDFFFF	0660000-066FFFF
103	128 / 64	0CE0000-0CFFFFF	0670000-067FFFF
104	128 / 64	0D00000-0D1FFFF	0680000-068FFFF
105	128 / 64	0D20000-0D3FFFF	0690000-069FFFF
106	128 / 64	0D40000-0D5FFFF	06A0000-06AFFFF
107	128 / 64	0D60000-0D7FFFF	06B0000-06BFFFF
108	128 / 64	0D80000-0D9FFFF	06C0000-06CFFFF
109	128 / 64	0DA0000-0DBFFFF	06D0000-06DFFFF
110	128 / 64	0DC0000-0DDFFFF	06E0000-06EFFFF
111	128 / 64	0DE0000-0DFFFFF	06F0000-06FFFFF
112	128 / 64	0E00000-0E1FFFF	0700000-070FFFF
113	128 / 64	0E20000-0E3FFFF	0710000-071FFFF
114	128 / 64	0E40000-0E5FFFF	0720000-072FFFF
115	128 / 64	0E60000-0E7FFFF	0730000-073FFFF
116	128 / 64	0E80000-0E9FFFF	0740000-074FFFF
117	128 / 64	0EA0000-0EBFFFF	0750000-075FFFF
118	128 / 64	0EC0000-0EDFFFF	0760000-076FFFF
119	128 / 64	0EE0000-0EFFFFF	0770000-077FFFF
120	128 / 64	0F00000-0F1FFFF	0780000-078FFFF
121	128 / 64	0F20000-0F3FFFF	0790000-079FFFF
122	128 / 64	0F40000-0F5FFFF	07A0000-07AFFFF
123	128 / 64	0F60000-0F7FFFF	07B0000-07BFFFF
124	128 / 64	0F80000-0F9FFFF	07C0000-07CFFFF
125	128 / 64	0FA0000-0FBFFFF	07D0000-07DFFFF
126	128 / 64	0FC0000-0FDFFFF	07E0000-07EFFFF
127	128 / 64	0FE0000-0FFFFFF	07F0000-07FFFFF

1. The 128M-bit device consists of 128 blocks, from block 0 to block 127.

Appendix B Common Flash Interface (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query command is issued, the memory enters Read CFI Query mode and read operations output the CFI data. Table 36, Table 37, Table 38, Table 39 and Table 40 and show the addresses (A-1, A0-A7) used to retrieve the data.

Table 36. Query structure overview(1)

Address		Sub-section name	Description
x16	x8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing & voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)

1. Query data are always presented on the lowest order data outputs.

Table 37. CFI query identification string(1)

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query Unique ASCII String ‘QRY’	‘Q’
11h	22h	0052h		‘R’
12h	24h	0059h		‘Y’
13h	26h	0002h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm	AMD compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for primary algorithm extended query table (see Table 40)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate vendor command set and control interface ID code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for alternate algorithm extended query table	NA
1Ah	34h	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 38. CFI query system interface information(1)

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} logic supply minimum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	2.7 V
1Ch	38h	0036h	V_{CC} logic supply maximum Program/Erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	3.6 V
1Dh	3Ah	00B5h	V_{PPH} [programming] supply minimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	11.5 V
1Eh	3Ch	00C5h	V_{PPH} [programming] supply maximum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 10 mV	12.5 V
1Fh	3Eh	0004h	Typical time-out for single byte/word program = 2^n µs	16 µs
20h	40h	0009h	Typical time-out for maximum size buffer program = 2^n µs	512 µs
21h	42h	0009h	Typical time-out for individual block erase = 2^n ms	0.5 s
22h	44h	000Fh 0010h 0011h	Typical time-out for full Chip Erase = 2^n ms	32M 33 s 64M 66 s 128M 131 s
23h	46h	0004h	Maximum time-out for byte/word program = 2^n times typical time-out	256 µs
24h	48h	0002h	Maximum time-out for buffer program = 2^n times typical time-out	2048 µs
25h	4Ah	0003h	Maximum time-out per individual block erase = 2^n times typical time-out	4 s
26h	4Ch	0002h	Maximum time-out for Chip Erase = 2^n times typical time-out	32M 131 s 64M 262 s 128M 524 s

1. The values given in the above table are valid for all packages.

Table 39. Device geometry definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0016h / 0017h / 0018h	Device size = 2^n in number of bytes	4 Mbytes 8 Mbytes 16 Mbytes
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x8, x16 Async.

Table 39. Device geometry definition

Address		Data	Description	Value
x16	x8			
2Ah 2Bh	54h 56h	0008h(1) 0000h	Maximum number of bytes in multiple-byte program or page= 2^n	256
2Ch	58h	See below table	Number of Erase block regions within device. It specifies the number of regions containing contiguous Erase blocks of the same size. 01h = uniform device 02h = boot device	-
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	See below table	Erase block region 1 information bits 0-15 = y, y+1 = Number of Erase blocks of identical size. bits 16-31 = z, Block size in region1 is zx256 bytes.	-
31h 32h 33h 34h	62h 64h 66h 68h	See below table	Erase block region 2 information bits 0-15 = y, y+1 = Number of Erase blocks of identical size. bits 16-31 = z, Block size in region 2 is zx256 bytes.	-
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase block region 3 information	0
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information	0

1. The value at 2Ah in CFI region is purposely set to 08h (256 bytes) due to compatibility reasons. The maximum 256-word program buffer can be used to optimize system program performance.

Address	32-Mbit			64-Mbit			128-Mbit
	Top	Bottom	Uniform	Top	Bottom	Uniform	Uniform
2Ch	02h	02h	01h	02h	02h	01h	01h
2Dh	07h	07h	3Fh	07h	07h	7Fh	7Fh
2Eh	00h	00h	00h	00h	00h	00h	00h
2Fh	20h	20h	00h	20h	20h	00h	00h
30h	00h	00h	01h	00h	00h	01h	02h
31h	3Eh	3Eh	00h	7Eh	7Eh	00h	00h
32h	00h	00h	00h	00h	00h	00h	00h
33h	00h	00h	00h	00h	00h	00h	00h
34h	01h	01h	00h	01h	01h	00h	00h

Table 40. Primary algorithm-specific extended query table (1)

Address x16	Address x8	Data	Description	Value
40h	80h	0050h	Primary algorithm extended query table unique ASCII string “PRI”	‘P’
41h	82h	0052h		‘R’
42h	84h	0049h		‘I’
43h	86h	0031h	Major version number, ASCII	‘1’
44h	88h	0033h	Minor version number, ASCII	‘3’
45h	8Ah	0018h	Address sensitive unlock (bits 1 to 0) 00 = required, 01= not required Silicon revision number (bits 7 to 2)	Required
46h	8Ch	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = read and write	2
47h	8Eh	0001h	Block protection 00 = not supported, x = number of blocks per group	1
48h	90h	0000h	Temporary block unprotect 00 = not supported, 01 = supported	Not supported
49h	92h	0008h	Block protect / unprotect 08 = M29EWH/M29EWL	8
4Ah	94h	0000h	Simultaneous operations: not supported	NA
4Bh	96h	0000h	Burst mode, 00 = not supported, 01 = supported	Not supported
4Ch	98h	0002h	Page mode, 00 = not supported, 01 = 8-word page 02 = 8-word page, 03 = 16-word page	8-word page
4Dh	9Ah	00B5h	V_{PPH} supply minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5 V
4Eh	9Ch	00C5h	V_{PPH} supply maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5 V
4Fh	9Eh	00xxh	Top/bottom boot block flag xx = 02h: Bottom boot device, HW protection for bottom two blocks xx = 03h: Top boot device, HW protection for top two blocks xx = 04h: Uniform device, HW protection for lowest block xx = 05h: Uniform device, HW protection for highest block	device type (bottom boot, top boot, uniform)
50h	A0h	0001h	Program suspend, 00 = not supported, 01 = supported	Supported

1. The values given in the above table are valid for all packages.

Appendix C Extended Memory Block

The M29EW has an extra block, the Extended Memory Block, that can be accessed using a dedicated command. This Extended Memory Block is 128 words in x16 mode and 256 bytes in x8 mode. It is used as a security block (to provide a permanent security identification number) or to store additional information.

The device can be shipped either with the Extended Memory Block pre-locked by Numonyx, or unlocked.

If the Extended Memory Block is not pre-locked by Numonyx, it can be customer-lockable. Its status is indicated by bit DQ7 of Extended Memory Block Verify Indicator in Auto Select mode. This bit is permanently set to either ‘1’ or ‘0’ at the Numonyx factory and cannot be changed. When set to ‘1’, it indicates that the device is pre-locked by Numonyx and the Extended Memory Block is protected. When set to ‘0’, it indicates that the device is customer-lockable. Bit DQ7 being permanently locked to either ‘1’ or ‘0’ is another security feature which ensures that a customer-lockable device cannot be used instead of a Numonyx pre-locked one.

Bit DQ7 is the most significant bit in the Extended Memory Block Verify Indicator. It can be read in Auto Select mode using either the Programmer (see *Table 7* and *Table 8*) or the In-system method (see *Table 9* and *Table 10*).

The Extended Memory Block can only be accessed when the device is in Extended Memory Block mode. For details of how the Extended Memory Block mode is entered and exited, refer to the *Section 6.3.1: Enter Extended Memory Block command* and *Section 6.3.2: Exit Extended Memory Block command*, and to *Table 13* and *Table 9*.

C.1 Numonyx pre-locked Extended Memory Block

If devices of which the Extended Memory Block is pre-locked upon customer request, the 128bits security identification number is written to the Extended Memory Block address space (see *Table 41: Extended Memory Block address and data*) in Numonyx factory. The contents in the Extended Memory Block cannot be changed any more.

C.2 Customer-lockable Extended Memory Block

A device where the Extended Memory Block is customer-lockable is delivered with the DQ7 bit set to ‘0’ and the Extended Memory Block unprotected. It is up to the customer to program and protect the Extended Memory Block but care must be taken because the protection of the Extended Memory Block is not reversible.

If the device has not been shipped with the Extended Memory Block pre-protected, the block can be protected by setting the Extended Memory Block Protection bit, DQ0, to ‘0’.

However, this bit can only be programmed once; and once it is protected the Extended Memory Block cannot be unprotected.

Once the Extended Memory Block is programmed, the Exit Extended Memory Block command must be issued to exit the Extended Memory Block mode and return the device to Read mode.

Table 41. Extended Memory Block address and data

<table>
<tr><th colspan="2">Address(1)</th><th colspan="3">Data</th></tr>
<tr><th>x8</th><th>x16</th><th>Numonyx pre-locked</th><th colspan="2">Customer-lockable</th></tr>
<tr><td>000000h-00000Fh</td><td>000000h-000007h</td><td>Secure identification number</td><td rowspan="2">Determined by customers (default)</td><td>Secure identification number</td></tr>
<tr><td>000010h-0000FFh</td><td>000008h-00007Fh</td><td>Protected and unavailable</td><td>Determined by customers</td></tr>
</table>

Appendix D Revision History

Table 42. Document revision history

Date	Version	Changes
Jun 2009	01	Initial release
Apr 2010	02	Added 48L TSOP and 48B BGA connection information. Added 64M and 32M memory map. Added 48L TSOP and 48B BGA package outline information. Updated program performance and suspend latency. Order information updated with device feature digit. Updated part number information in valid combination table. CFI updated to cover 64-Mbit and 32-Mbit device related information. Read electronic signature information updated to cover 64-Mbit and 32-Mbit device. Block protection information updated to cover 64-Mbit and 32-Mbit device. Updated the Random Read AC waveforms about BYTE# pin in *Section 9: DC and AC Parameters*. Added a note to state fast program (double program, quadruple program and octuple program) can only work with VPPL in *Section 6.2: Fast Program commands on page 37*. Updated typical time-out and maximum time-out for buffer program at CFI table. Updated the description of V_{PP}/WP# pin in *Section 2.8: V_{PP}/Write Protect (V_{PP}/WP#) on page 16*. Added JESD47E compliant.

Date	Version	Changes
May 2010	03	Updated the Random Read AC waveforms about BYTE# pin in *Section 9: DC and AC Parameters*. Put a link for product part numbers in *Section 12: Ordering Information*.
Jan 2011	04	Aligned with device about the commands for double byte/quadruple byte/octuble byte program at *Table 11: Fast Program commands, 8-bit mode on page 46* and double word/quadruple word program at *Table 12: Fast Program commands, 16-bit mode on page 47*. Corrected the CFI value for address 2Fh (x16) for 64-Mbit/32-Mbit Top/Bottom devices. Corrected the CFI value for address 22h (x16) for 32-Mbit devices. Removed the invalid automatic standby mode from front page and *Section 3: Bus Operations on page 19*. Removed the statement about unlock bypass fast program at note of *Section 6.2: Fast Program commands on page 37* since it's not valid. Added JEDEC standard lead width for TSOP56 package at *Table 29: TSOP56 – 56 lead thin small-outline package, 14 x 20 mm, package mechanical data on page 82*
Apr 2011	05	For read ID and read protection status, align with device about higher address pins input status at *Table 5*, *Table 6*, *Table 7* and *Table 8*. Corrected the glitch filter from 5ns to 3ns Removed the invalid statement about applying VID to A9 to enter Auto Select mode at *Section 7.1.3: Extended Memory Block Protection bit (DQ0)* Add Blank Check related information