

TB62212FTAG

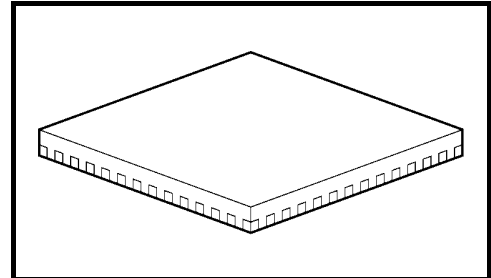
PWM Chopper Type Dual-Stepping Motor Driver

The TB62212FTAG is a PWM chopper type dual-stepping motor driver.

Two stepping motor drivers can drive up to four brushed DC motors. Incorporating two pairs of H-bridge drivers, the TB62212FTAG can drive two DC motors or a single stepping motor.

Features

- Single-chip motor driver for bipolar stepping motor control
- Monolithic IC structured by BiCD process.
- Low ON-resistance: $R_{on} = 2.2 \Omega$
(Upper and lower sum of P- and N-channel output transistors: $T_j = 25^\circ\text{C}$ @0.6 A typ.)
In large mode, ON-resistance of combined H-bridges is: $R_{on} = 1.1 \Omega$ (Upper and lower sum of P- and N-channel output transistors: $T_j = 25^\circ\text{C}$ @0.6 A typ.)
- Over-current detection (ISD), thermal shutdown (TSD) and V_M power-on reset circuits
- Since the IC incorporates a V_{CC} regulator for internal circuit operation, an external power supply (5 V) is not required.
- Package: Quad leadless package with a backside heat sink (QFN48-P-0707-0.50: 0.5-mm lead pitch)
- Maximum output withstand voltage: 40 V
- Output current: 2.0 A (max) in DC (S) mode; 1.5 A (max) in Stepping (S) mode
- Chopping frequency can be set by external oscillator. High-speed chopping is possible at 100 kHz or higher.

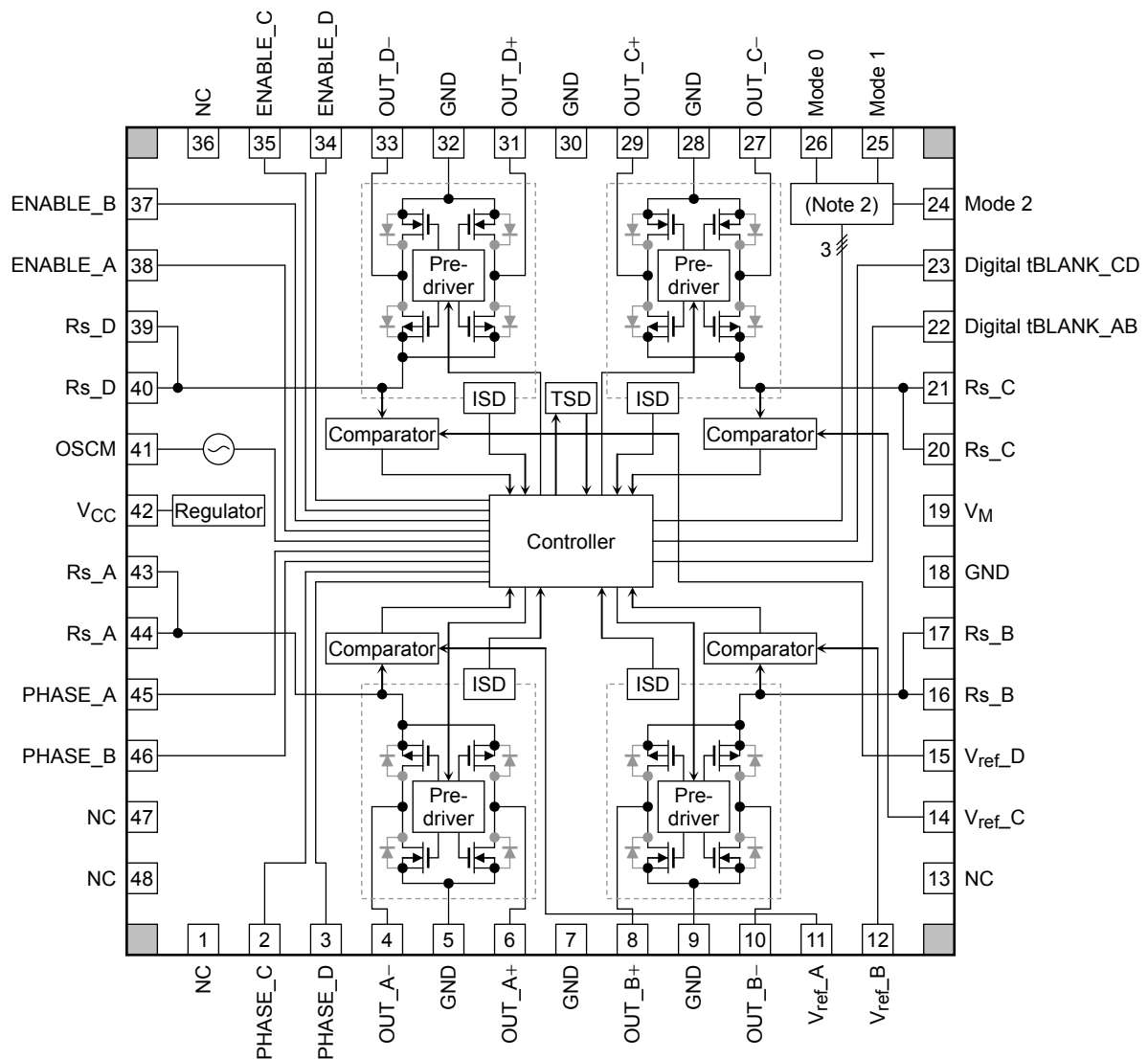


Weight: 0.14 g(typ.)

Note) This product is sensitive to electrostatic discharge. Please handle with care

ESD	Weak pin	value	condition
HBM	4, 6, 8, 10, 27, 29, 31, 33	-1.2kV	Reference 19pin (VM)

Block Diagram and Pin Layout (Brushed DC Motor(S) × 4-Axis Control Mode)



Note 1: GND wiring: We recommend that a heat sink be grounded at any parts, and the board and output pins be grounded at only one contact point. Take the heat dissipation into consideration when designing the board. When in controlling the setting pins for each mode by SW, those pins should be pulled up to power supply like V_{CC} or pulled down to GND not to go into a high-impedance (Hi-Z) state. Utmost care is necessary in the design of the output line, V_M line and GND line since IC may be destroyed due to short-circuit between outputs, to supply, or to ground. Especially for those pins that are connected to power supply and get a large current flow (such as V_M , RS, OUT and GND), they should be properly wired; otherwise troubles including destruction may occur to this IC. If the logic input pins are not wired properly, malfunction that would destroy the IC may occur due to a large current exceeding the absolute maximum ratings. Care should be taken in the design of board layouts and implementation of the IC.

Note 2: Mode (2, 1, 0)
 $(H, H, H) = \text{stepper_S} \times 2$
 $(H, H, L) = \text{DC_L} \times 2$
 $(H, L, H) = \text{stepper_L}$
 $(H, L, L) = \text{DC_S} \times 4$
 $(L, H, H) = \text{DC_L} + \text{stepper_s}$
 $(L, H, L) = \text{DC_S} \times 2 + \text{stepper_s}$

Pin Assignment

Pin No.	Function	(1) Stepping (S) × 2	(2) DC (L) × 2	(3) Stepping (L)	(4) DC (S) × 4	(5) DC (L) + Stepping (S)	(6) DC (S) × 2 + Stepping (S)
1	No connect	No connect	No connect	No connect	No connect	No connect	No connect
2	PHASE_C	Phase input for C	IN1 input for C and D	Phase input for C and D	IN1 input for C	Phase input for C	Phase input for C
3	PHASE_D	Phase input for D	PWM for C and D	—	IN1 input for D	Phase input for D	Phase input for D
4	OUT_A-	Negative output for motor A	Negative output for motors A and B	Negative output for motors A and B	Negative output for motors A	Negative output for motors A and B	Negative output for motor A
5	GND	Ground for A	Ground for A	Ground for A	Ground for A	Ground for A	Ground for A
6	OUT_A+	Positive output for motor A	Positive output for motors A and B	Positive output for motors A and B	Positive output for motor A	Positive output for motors A and B	Positive output for motor A
7	GND	Ground	Ground	Ground	Ground	Ground	Ground
8	OUT_B+	Positive output for motor B	Positive output for motors A and B	Positive output for motors A and B	Positive output for motor B	Positive output for motors A and B	Positive output for motor B
9	GND	Ground for B	Ground for B	Ground for B	Ground for B	Ground for B	Ground for B
10	OUT_B-	Negative output for motor B	Negative output for motors A and B	Negative output for motors A and B	Negative output for motor B	Negative output for motors A and B	Negative output for motor B
11	V _{ref_A}	V _{ref} for A	V _{ref} for A and B	V _{ref} for A and B	V _{ref} for A	V _{ref} for A and B	V _{ref} for A
12	V _{ref_B}	V _{ref} for B	—	—	V _{ref} for B	—	V _{ref} for B
13	No connect	No connect	No connect	No connect	No connect	No connect	No connect
14	V _{ref_C}	V _{ref} for C	V _{ref} for C and D	V _{ref} for C and D	V _{ref} for C	V _{ref} for C	V _{ref} for C
15	V _{ref_D}	V _{ref} for D	—	—	V _{ref} for D	V _{ref} for D	V _{ref} for D
16	Rs_B	Power supply for B	Power supply for A and B	Power supply for A and B	Power supply for B	Power supply for B	Power supply for B
17	Rs_B	Power supply for B	Power supply for A and B	Power supply for A and B	Power supply for B	Power supply for B	Power supply for B
18	GND	Logic ground	Logic ground	Logic ground	Logic ground	Logic ground	Logic ground
19	V _M	V _M reference monitor	V _M reference monitor	V _M reference monitor	V _M reference monitor	V _M reference monitor	V _M reference monitor
20	Rs_C	Power supply for C	Power supply for C	Power supply for C	Power supply for C	Power supply for C	Power supply for C
21	Rs_C	Power supply for C	Power supply for C	Power supply for C	Power supply for C	Power supply for C	Power supply for C
22	Digital tBLANK_AB	—	tBLANK setting (Note)	—	tBLANK setting (Note)	tBLANK setting (Note)	tBLANK setting (Note)
23	Digital tBLANK_CD	—	tBLANK setting (Note)	—	tBLANK setting (Note)	—	—
24	Mode 2	High	High	High	High	Low	Low
25	Mode 1	High	High	Low	Low	High	High
26	Mode 0	High	Low	High	Low	High	Low
27	OUT_C-	Negative output for motor C	Negative output for motors C and D	Negative output for motors C and D	Negative output for motor C	Negative output for motor C	Negative output for motor C
28	GND	Ground for C	Ground for C	Ground for C	Ground for C	Ground for C	Ground for C
29	OUT_C+	Positive output for motor C	Positive output for motors C and D	Positive output for motors C and D	Positive output for motor C	Positive output for motor C	Positive output for motor C
30	GND	Ground	Ground	Ground	Ground	Ground	Ground

Pin No.	Function	(1) Stepping (S) × 2	(2) DC (L) × 2	(3) Stepping (L)	(4) DC (S) × 4	(5) DC (L) + Stepping (S)	(6) DC (S) × 2 + Stepping (S)
31	OUT_D+	Positive output for motor D	Positive output for motors C and D	Positive output for motors C and D	Positive output for motor D	Positive output for motor D	Positive output for motor D
32	GND	Ground for D	Ground for D	Ground for D	Ground for D	Ground for D	Ground for D
33	OUT_D-	Negative output for motor D	Negative output for motors C and D	Negative output for motors C and D	Negative output for motor D	Negative output for motor D	Negative output for motor D
34	ENABLE_D	Enable input for D	—	—	IN2 input for D	Enable input for D	Enable input for D
35	ENABLE_C	Enable input for C	IN2 input for C and D	Enable input for C and D	IN2 input for C	Enable input for C	Enable input for C
36	No connect	No connect	No connect	No connect	No connect	No connect	No connect
37	ENABLE_B	Enable input for B	—	—	IN2 input for B	—	IN2 input for B
38	ENABLE_A	Enable input for A	IN2 input for A and B	Enable input for A and B	IN2 input for A	IN2 input for A and B	IN2 input for A
39	Rs_D	Power supply for D	Power supply for C and D	Power supply for C and D	Power supply for D	Power supply for D	Power supply for D
40	Rs_D	Power supply for D	Power supply for C and D	Power supply for C and D	Power supply for D	Power supply for D	Power supply for D
41	OSCM	OSCM	OSCM	OSCM	OSCM	OSCM	OSCM
42	V _{CC}	Regulator monitor	Regulator monitor	Regulator monitor	Regulator monitor	Regulator monitor	Regulator monitor
43	Rs_A	Power supply for A	Power supply for A	Power supply for A	Power supply for A	Power supply for A	Power supply for A
44	Rs_A	Power supply for A	Power supply for A	Power supply for A	Power supply for A	Power supply for A	Power supply for A
45	PHASE_A	Phase input for A	IN1 input for A and B	Phase input for A and B	IN1 input for A	IN1 input for A and B	IN1 input for A
46	PHASE_B	Phase input for B	PWM for A and B	—	IN1 input for B	PWM for A and B	IN1 input for B
47	No connect	No connect	No connect	No connect	No connect	No connect	No connect
48	No connect	No connect	No connect	No connect	No connect	No connect	No connect

Pin 22,23 Note: L: No tBLANK
H: tBLANK = OSCM × 3

Descriptions of Motor Drive Modes

- | | |
|---|--------------------------|
| (1) Stepping (S) × 2 control mode pin name and assignment | Mode (2, 1, 0)=(H, H, H) |
| (2) DC (L) × 2 control mode pin name and assignment | Mode (2, 1, 0)=(H, H, L) |
| (3) Stepping (L) × 1 control mode pin name and assignment | Mode (2, 1, 0)=(H, L, H) |
| (4) DC (S) × 4 control mode pin name and assignment | Mode (2, 1, 0)=(H, L, L) |
| (5) Stepping (S) × 1 control mode + DC (L) × 1 control mode pin name and assignment | Mode (2, 1, 0)=(L, H, H) |
| (6) Stepping (S) × 1 control mode + DC (S) × 2 control mode pin name and assignment | Mode (2, 1, 0)=(L, H, L) |

*: In the modes that include DC (S) mode, the digital tBLANK time can be separately set for each axis pair, axes A and B and axes C and D.

In DC (S) × 4-axis control mode, the external short brake function cannot be used. Thus, the short brake operation should be performed by using the IN1 and IN2 inputs.

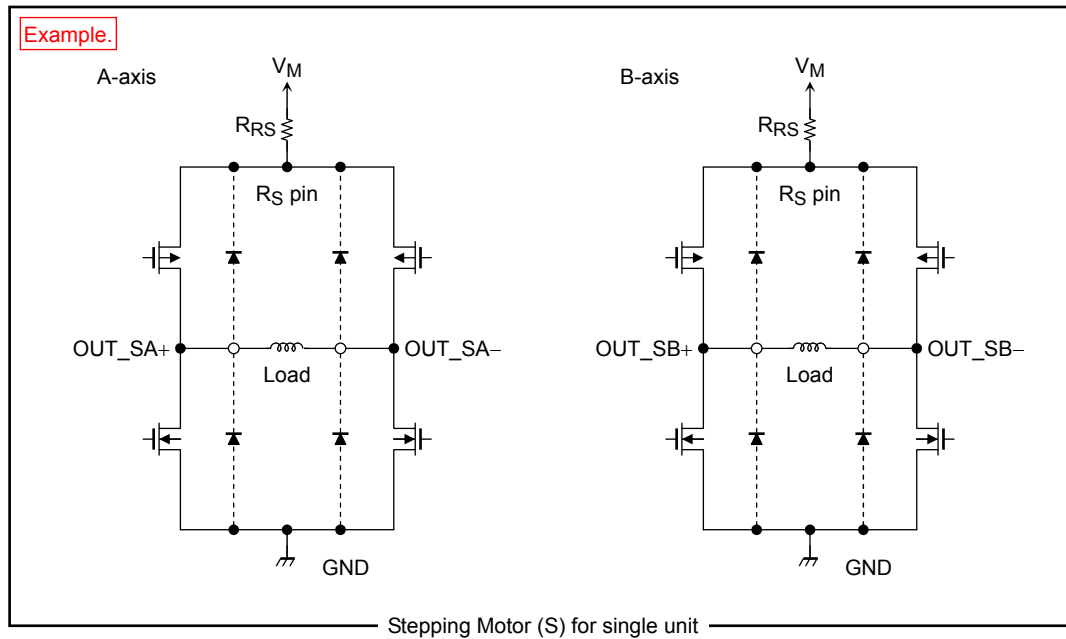
The motor drive Mode(2, 1, 0)= (H, L, L) is provided only for Toshiba testing and must not be used during normal operation.

Note 1: In Combination mode, such as Stepping (L) and DC (L) modes, the impedance outside the IC should be balanced.

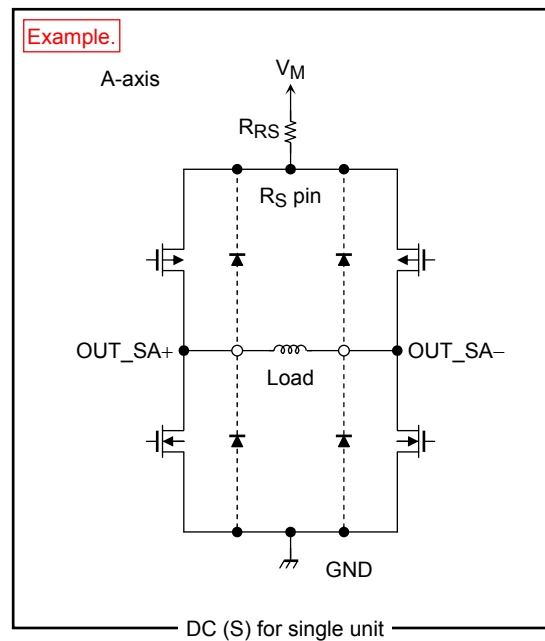
Note 2: In large mode, if the impedance of wiring to mutually connected output transistors is unbalanced, the current that flows through the transistor also becomes unbalanced and may exceed the absolute maximum rating of the transistor, thus permanently damaging the transistors.

H-bridge Combination (connection method) for Each Type of Motor Driver

Stepping Motor (S) Combination



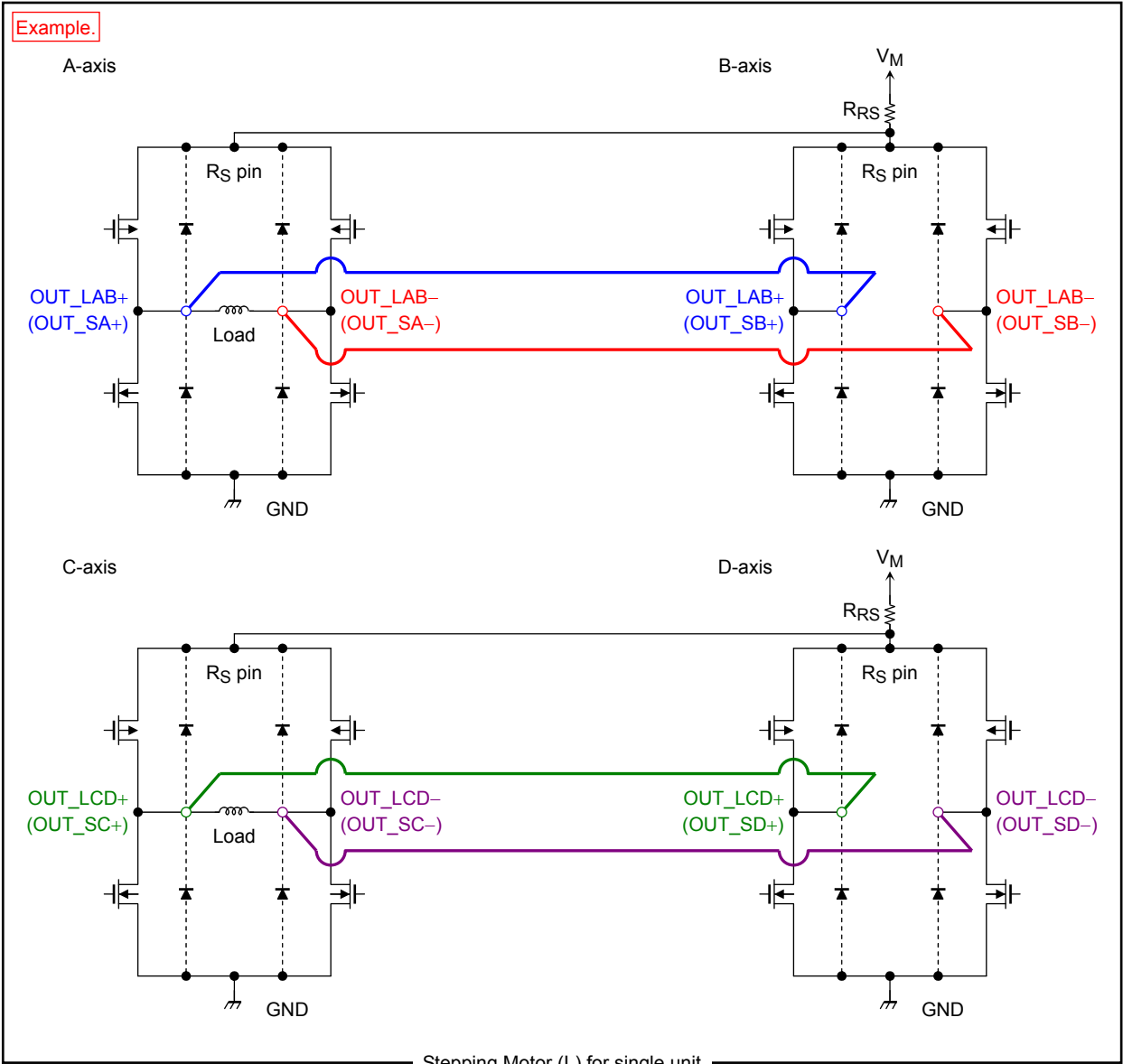
DC Motor (S) Combination



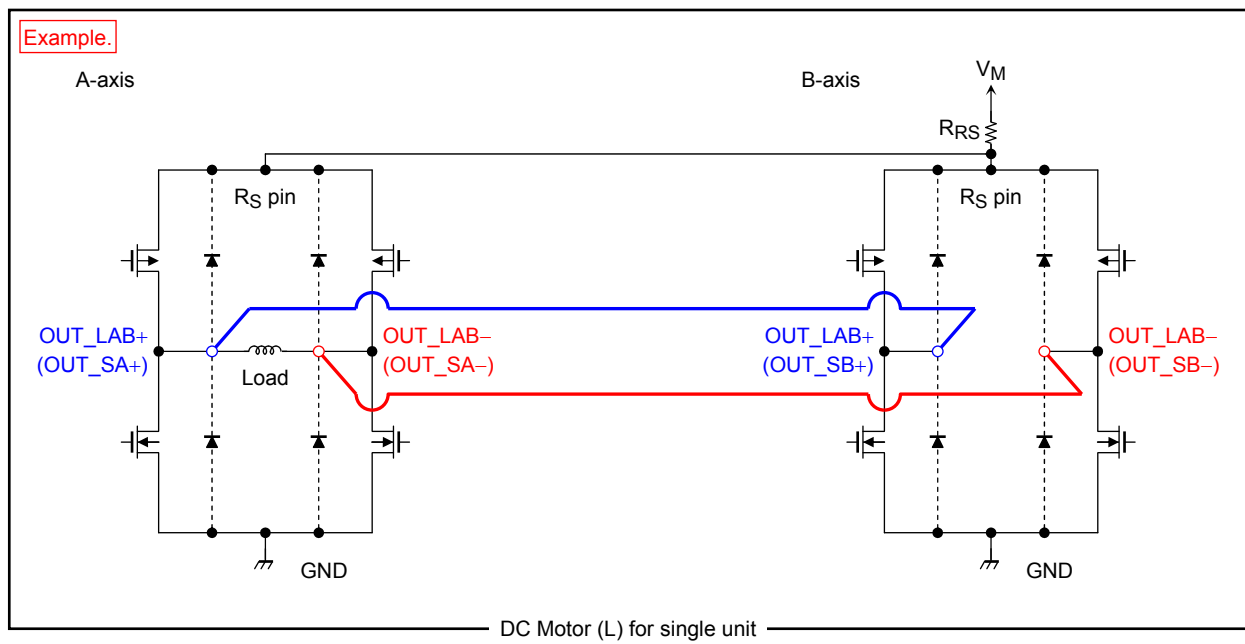
○: Indicates an IC output pin connected to a motor.

Stepping Motor (L) Combination

Example.



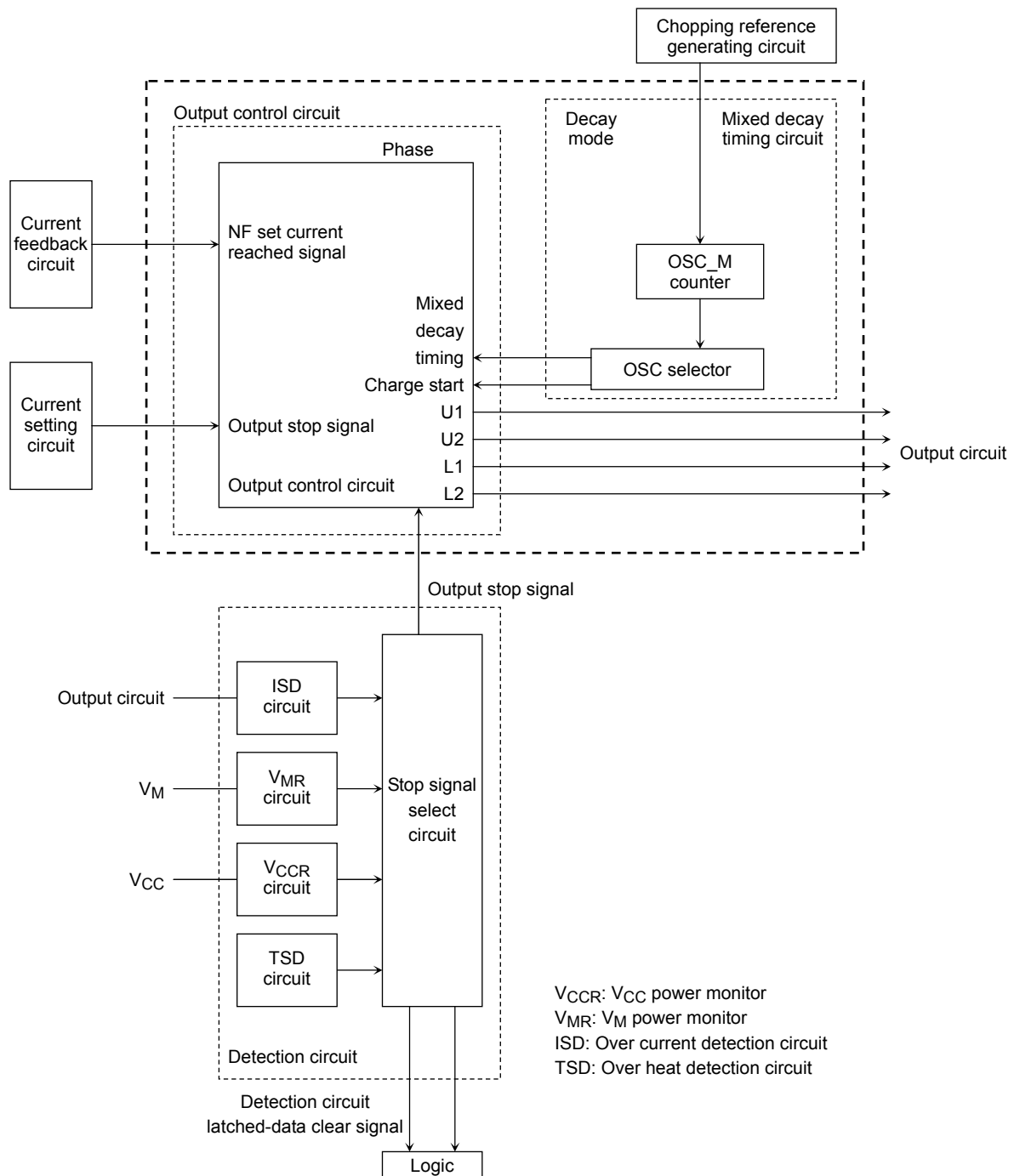
DC Motor (L) Combination



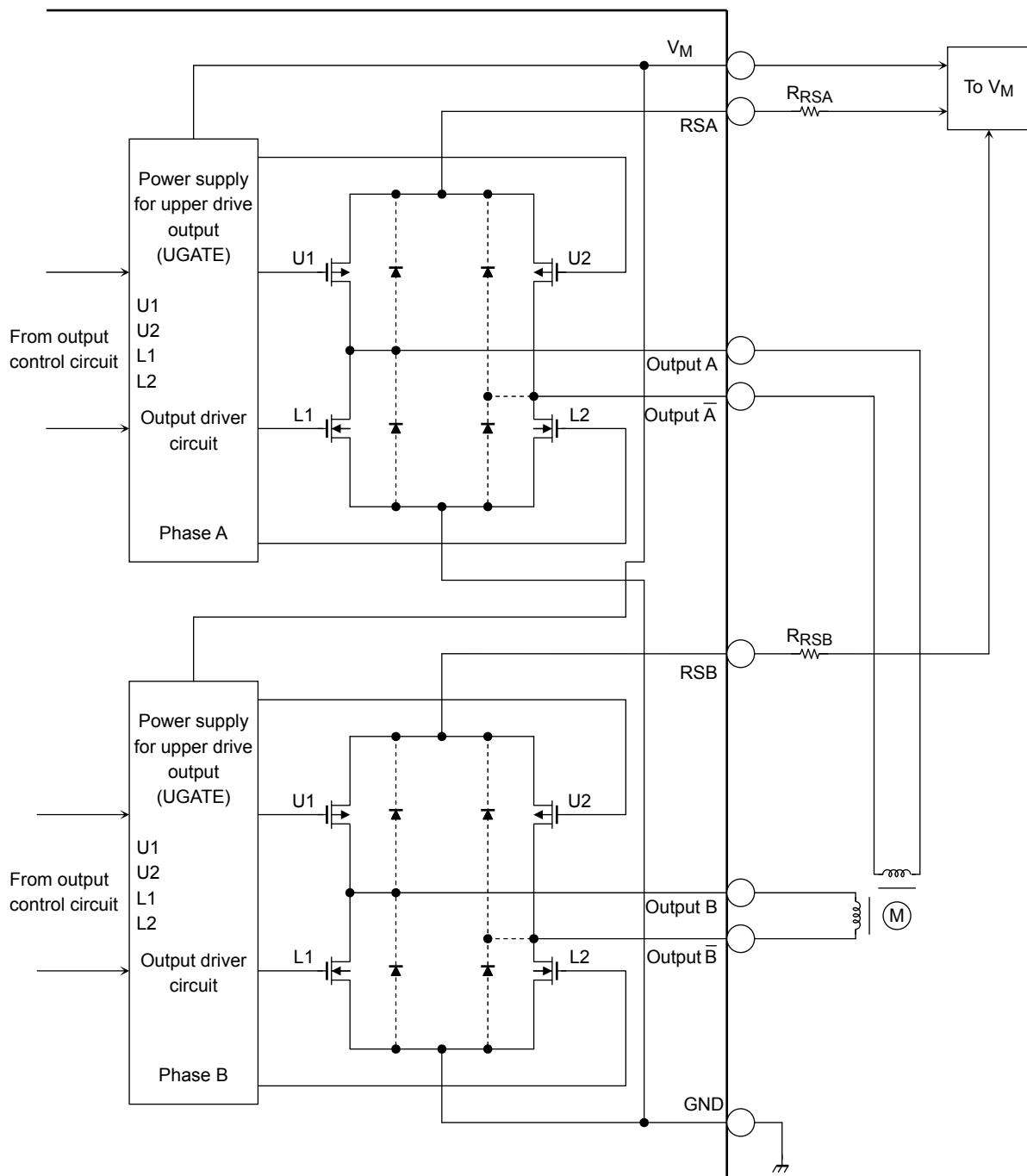
○ : Indicates an IC output pin connected to a motor.

Output Control Circuit, Current Feedback Circuit, and Current Setting Circuit for Motor Driver

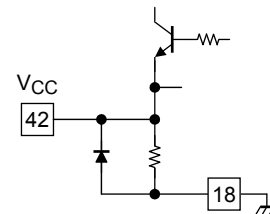
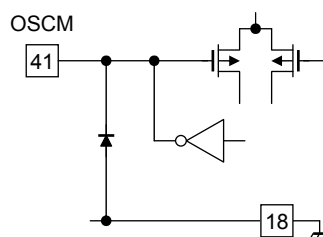
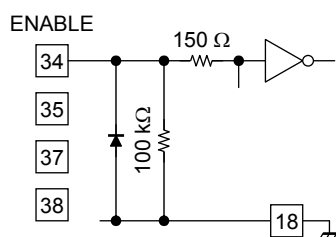
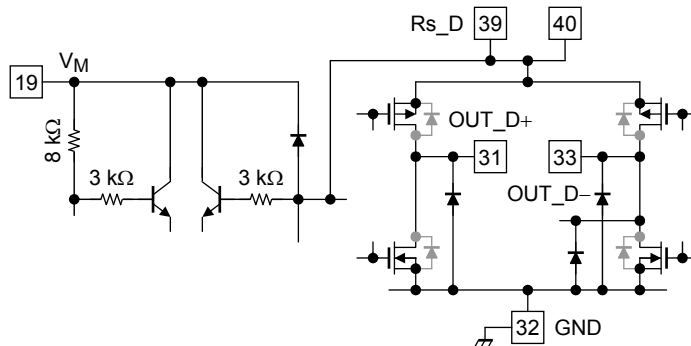
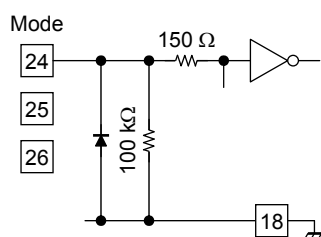
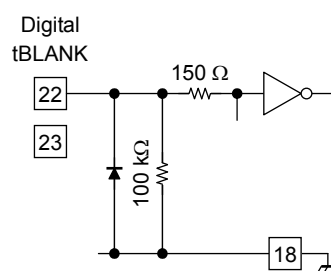
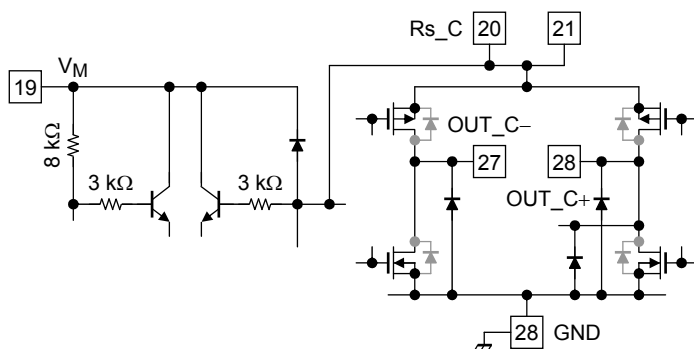
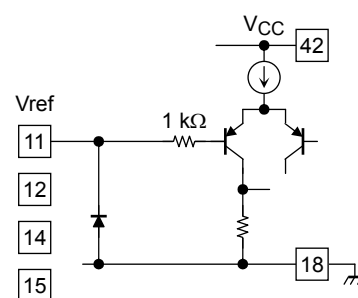
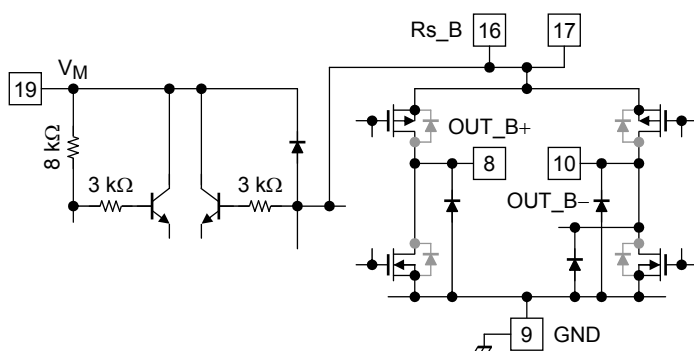
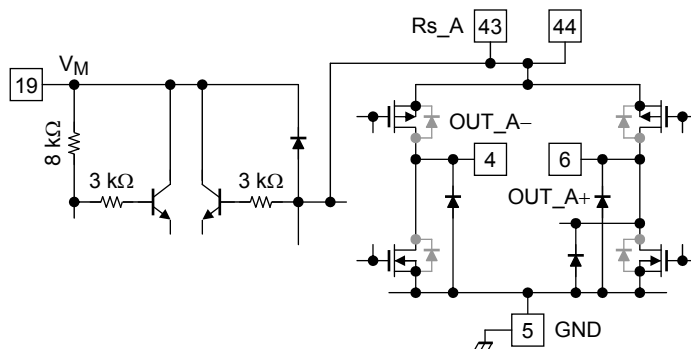
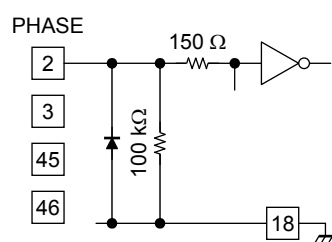
Note: Logic input pins are internally connected to pull-down resistors of about 100 k Ω .
However, connect those pins to GND if not used, or it may lead to malfunction.



Output Equivalent Circuit of A/B-unit (C/D-unit conforms to A/B-unit.)



Input Equivalent Circuits



Input Signal Functions (Stepping motor mode)

Input					Action
PHASE	ENABLE	M_MODE	V _{CCR} (Note 1) Or V _{MR}	Operation of TSD/ISD (Note 2)	
H	H	STEP	H	L	Output+: High, Output-: Low
L	H	STEP	H	L	Output-: High, Output+: Low
H	L	STEP	H	L	When ENABLE = L, output current of the respective phase is turned off.
H	H	STEP	H	L	Normal operation
H	H	—	L	L	Standby mode
H	H	—	H	H	Standby mode when TSD/ISD triggered. Remains until powered on again.

Note 1: V_{CCR} and V_{MR}

High when the operable range (3 V typical) or higher and Low when lower.

When one of V_{CCR} or V_{MR} is operating, the system is halted (OR relationship).

Note 2: High when the overheat detection circuit (TSD) or the over-current detection circuit (ISD) is in operation.

When one of TSD or ISD is operating, the system shuts down or goes into stand-by mode (OR relationship).

Note 3: Function of TSD and ISD

Until the POR is released again after the TSD or the ISD is triggered, the detection circuit remains activated and the IC is halted.

1. PHASE Input Pin Function (Stepping motor mode)

This pin indicates the current polarity used in driving a stepping motor. When in 2-phase excitation drive mode, motor can be rotated by changing the mode of this pin in phase A/B into sequential mode.

Input	Function
H	Positive polarity (A: H, $\bar{A}$: L)
L	Negative polarity (A: L, $\bar{A}$: H)

2. ENABLE Input Pin Function (Stepping motor mode)

Select whether to activate the output of the respective phases when driving a stepping motor. By controlling this pin, motor can be halted in OFF mode or can be driven in 1-2 phase excitation mode.

Upon start-up and shutdown, this pin should be set to Low to avoid malfunction.

Input	Function
H	Output of the corresponding channel: ON
L	Output of the corresponding channel: OFF

3. Function Table for Motor Drive Mode Selection

Motor drive modes can be selected depending on the type of motors to be driven.

The configuration of H-bridge drivers and control category are changed according to the selected mode.

There is basically no need to change drive modes during motor operation. Thus, the TB62212FTAG does not support dynamic mode switching.

Changing the settings of these pins changes the functions and timing of control pins.

The setting of mode select pins must not be changed after the TB62212FTAG is powered on.

MODE 0	MODE 1	MODE 2	Drive Mode
H	H	H	Stepping (S) × 2
L	H	H	DC (L) (Combination) × 2
H	L	H	Stepping (L) (Combination) × 1
L	L	H	DC (S) × 4
H	H	L	DC (L) (Combination) × 1 + Stepper S
L	H	L	DC (S) × 2 + Stepper S
H	L	L	Inhibit (For Toshiba testing only)
L	L	L	Standby mode

Stepping Motor Mode

This mode is used to drive stepping motors. The tBLANK time is specified as a fixed analog value (about 300 ns). Each motor is controlled via two logic control inputs, PHASE (current direction) and ENABLE (ON/OFF), and via the Vref input for constant-current control.

Brushed DC Motor Mode

This mode is used to drive brushed DC motors.

The tBLANK time can be specified as a fixed analog value, or as three OSC cycles in digital tBLANK mode, where OSC is a reference signal for chopper circuit.

When DC motors are driven under PWM control, a discharge current spike can occur due to a varistor. To prevent this current spike from erroneously tripping the constant-current sensor, the constant-current sensor is digitally blanked for a period of time that is determined by tBLANK, which is derived from the OSC signal.

Using this blanking function enables constant-current limiter control, as well as external PWM control. An over-current can be observed only during blank times.

Combination Mode

The Combination mode, such as DC (L) and Stepper (L) modes, can be selected when two units of H-bridges with the same characteristics are operated in parallel.

In this mode, the actual ON-resistance is reduced by half while the current capability is doubled. (Specifications actually include the thermal capacitance as well. See electrical characteristics for more details.)

To use this mode, the power supply, ground, and output pins that have identical names should be shorted together on the board.

At the same time, the wirings of a board should be routed to balance the impedance at each pin. Otherwise, the shorted pins may experience a current imbalance and more current may flow into either one of them than the other.

4. D_tBLANK Input Pin Function (only in DC Motor mode)

D_tBLANK	Motor Drive Mode
L	OFF: Digital Blank Time = OSC × 0
H	ON: Digital Blank Time = OSC × 3

Note: When D_tBLANK is Low, only the analog tBLANK time is provided.

5. Control Signal Functions in Brushed DC Motor Mode 1 (in DC (L) × 2-Axis Control Mode)

Control Input			State of the Output Stage		
IN1 (PHASE pin)	IN2 (ENABLE pin)	PWM (Short brake)	OUT+	OUT–	Mode
H	H	H	L	L	Short brake
		L			
L	H	H	L	H	Forward/reverse
		L	L	L	Short brake
H	L	H	H	L	Reverse/forward
		L	L	L	Short brake
L	L	H	OFF (High-Z)	OFF (High-Z)	Stop
		L			

When the TB62212FTAG enters the modes in which the short brake pin is not used such as DC (S) × 4 mode, the PWM input is held High.

6. Control Signal Functions in Brushed DC Motor Mode 2 (in DC (S) × 4-Axis Control Mode)

Control Input		State of the Output Stage		
IN1 (PHASE pin)	IN2 (ENABLE pin)	OUT+	OUT–	Mode
H	H	L	L	Short brake
L	H	L	H	Forward/reverse
H	L	H	L	Reverse/forward
L	L	OFF (High-Z)	OFF (High-Z)	Stop

External PWM Control Function

The motor speed can be controlled by applying 0-V and 5-V (higher than TTL level) PWM signals at the PWM pin.

In PWM mode, the PWM chopper circuit alternates between on and short brake.

When the PWM speed control is not required, the PWM pin (short brake pin) must be held High.

When the constant-current limiter is used, the TB62212FTAG enters 37.5% Mixed Decay mode after an output current reaches the predefined current value. The dead band time is internally inserted to prevent a shoot-through current eliminating the need of special arrangement.

The short brake function is disabled in Stepping Motor mode (Large or Small).

Stepping motors can also be driven in Brushed DC motor mode.

To perform such operation, the short brake function should not be used and the D_tBLANK pin should be set Low.

At the same time, input signal functions should also be confirmed.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Logic supply voltage	Internal V _{CC}	6	V	
Output voltage	V _M	40	V	
Output current	I _{out} (ST_S)	1.5	A/phase	(Note 1)
	I _{out} (ST_L)	1.8	A/phase	
	I _{out} (DC_S)	2.0	A/phase	
	I _{out} (DC_L)	4.0	A/phase	
Current detect pin voltage	V _{RS}	V _M ± 4.5	V	
Logic input voltage	V _{IN}	−0.4 to 6.0	V	
Constant current reference voltage input pin	V _{ref}	GND to 4.2 V	V	
Power dissipation	P _D	1.4	W	(Note 3)
		3.2		(Note 4)
Operating temperature	T _{opr}	−40 to 85	°C	
Storage temperature	T _{stg}	−55 to 150	°C	
Junction temperature	T _j	150	°C	

Note 1: Perform thermal calculations for the maximum current value under normal conditions. Use the IC with adequate margin per phase with respect to the absolute maximum ratings.

Note 2: Measured for the IC only. (Ta = 25°C)

Note 3: Measured when mounted on the board. (Ta = 25°C)

Ta: IC ambient temperature

T_{opr}: IC ambient temperature when starting operation

T_j: IC chip temperature during operation. T_j (max) is controlled by TSD (thermal shutdown circuit).

Absolute Maximum Ratings

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

If the voltage or current on any pin exceeds the absolute maximum rating, the device's internal circuitry can be destroyed, degraded, or damaged, which may lead to destruction, damage, or degradation of peripheral circuitry or parts.

When designing the operating environment and the usage environment, please make sure that the absolute maximum ratings are not exceeded under any operating conditions.

Use the actual applications within the above-listed operating range.

Operating Ranges (Ta = 0 to 85°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Internal logic power supply voltage	V _{CC}	—	(Automatically generated)	4.5	5.0	5.5	V
Motor power supply voltage	V _M	—		10	24	38	V
Motor output current	I _{out} (ST_S)	—	Ta = 25°C, per phase	—	0.3	1.0	A
	I _{out} (ST_L)	—	Ta = 25°C, per phase	—	0.6	1.5	
	I _{out} (DC_S)	—	Ta = 25°C, per phase	—	1.0	1.9	
	I _{out} (DC_L)	—	Ta = 25°C, per phase	—	2.0	3.8	
Logic input voltage	V _{IN}	—	—	GND	3.3	5.0	V
Chopping frequency setting range	f _{chop}	—	V _{CC} = 5.0 V	40	100	150	kHz
V _{ref} voltage	V _{ref}	—	V _M = 24 V	GND	3.0	4.0	V
Current detect pin voltage	V _{RS}	—	V _M = 24 V	0	±1.0	±1.5	V

Note: Use the maximum junction temperature (T_j) at 120°C or less. The Maximum current cannot be used under certain thermal conditions.

Electrical Characteristics 1 (Unless otherwise specified, Ta = 25°C, V_M = 24 V)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Logic input voltage	High	V _{IN} (H)	1	Logic input pins	2.0	3.3	5.4	V
	Low	V _{IN} (L)			GND – 0.4	GND	0.8	
Logic input hysteresis		His	1	Logic input pins	0.1	0.2	0.5	V
Logic input current		I _{IN} (H)	2	V _{IN} = 5 V, Input pins with resistor	—	50	70	μA
		I _{IN} (L)			—	—	1.0	
Power dissipation (V _M pin)		I _{M1}	3	OUT OPEN (ENABLE ALL = L), Output all off	—	1.0	2.0	mA
		I _{M2}		OUT OPEN, f _{PWM} = 100 kHz Logic active, Output off	—	8	10	
Output leakage current	Upper side	I _{OH}	5	V _{RS} = V _M = 24 V, V _{out} = 0 V, ENABLE ALL = L	–1	—	—	μA
	Lower side	I _{OL}		V _{RS} = V _M = V _{out} = 24 V, ENABLE ALL = L	—	—	1.0	μA
Output current differential		ΔI _{out1}	7	Differences between output current channels I _{out} = 0.6 A	–5	—	5	%
Output current setting differential		ΔI _{out2}	7	I _{out} = 0.6 A	–5	—	5	%
RS pin current		I _{RS}	8	V _{RS} = 24 V, V _M = 24 V, ENABLE ALL = L (All halted)	—	—	10	μA
Output transistor drain-source ON-resistance	R _{on} (DS: Upper/Lower-sides) S	9	9	I _{out} = 0.6 A, T _j = 25°C, Drain-source, (Upper + Lower) Small Mode	—	2.2	2.6	Ω
	R _{on} (DS: Upper/Lower-sides) L			I _{out} = 0.6 A, T _j = 25°C, Drain-source, (Upper + Lower) Large Mode	—	1.1	1.3	

Electrical Characteristics 2 (Unless otherwise specified, Ta = 25°C, V_M = 24 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
V _{ref} input voltage	V _{ref}	10	ENABLE = H, Output on	GND	2.0	4.0	V
V _{ref} input current	I _{ref}	10	ENABLE = L, Output off, V _{ref} = 3.0 V	0	—	10	μA
V _{ref} attenuation ratio	V _{ref} (gain)	6	ENABLE = H, Output on, V _{ref} = 2.0 V	1/4.8	1/5.0	1/5.2	—
TSD temperature	T _J TSD (Note 1)	11	—	130	—	170	°C
Internal V _{CC} return voltage	V _{CCR}	12	ENABLE = H	2.0	3.0	4.0	V
V _M return voltage	V _{MR}	13	ENABLE = H	7.0	8.0	9.0	V
Detection current of over-current detection circuit	ISD (Note 2)	14	f _{chop} = 100 kHz set	—	2.8	—	A

Note 1: Thermal shut down (TSD) circuit

When the IC junction temperature reaches the specified value and become overheated under irregular conditions causing the TSD circuit to be activated, the internal halt circuit is activated shutting down all the outputs to off (Hi-Z).

When the temperature is set between 130°C (min) to 170°C (max), the TSD circuit operates.

When the TSD circuit is activated, output is halted until the POR is released.

Note 2: Over-current detection circuit

When the current exceeding the specified value flows to the output under irregular conditions, the internal halt circuit is activated switching all the outputs to off.

Until the POR is released, the over-current detection circuit remains activated.

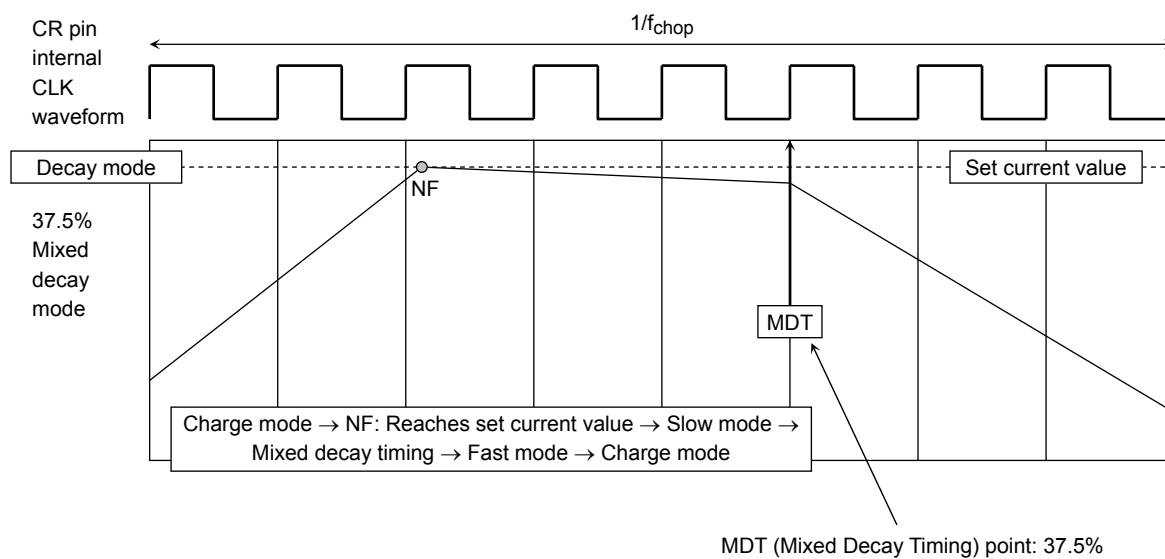
For permanent fail-safe operation, be sure to add a fuse to the V_M power supply.

AC Characteristics (Ta = 25°C, V_M = 24 V, 6.8 mH/5.7 Ω)

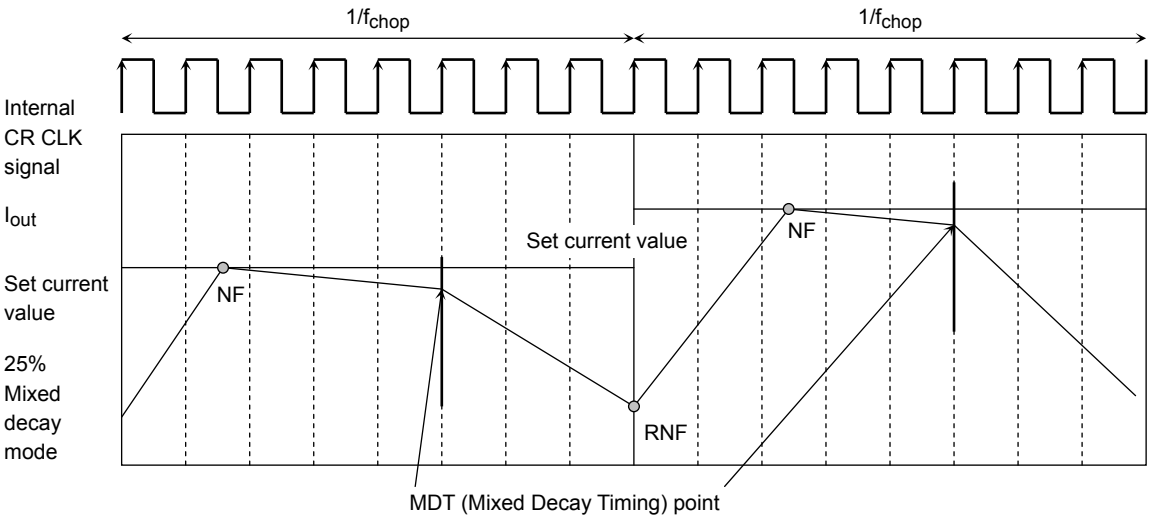
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Logic input frequency	f _{Logic}		—	1.0	—	200	kHz
Minimum signal pulse width	t _w (t _{Logic})		—	100	—	—	ns
	t _{wp}			50	—	—	
	t _{wn}			50	—	—	
Output transistor switching characteristic	t _r		Output load: 6.8 mH/5.7 Ω	—	0.1	—	μs
	t _f			—	0.1	—	
	t _{pLH} (INX)		Signal to OUT Output load: 6.8 mH/5.7 Ω	—	1	—	
	t _{pHL} (INX)			—	1.5	—	
	t _{pLH} (OSC)		OSC_M to OUT Output load: 6.8 mH/5.7 Ω	—	0.5	—	
	t _{pHL} (OSC)			—	1	—	
PWM ON-duty minimum width	t _{PWM} (Min)		When in DC motor mode Output load: 6.8 mH/5.7 Ω	2	—	—	μs
Noise rejection dead band time	t _{BLANK_AB} (L) t _{BLANK_CD} (L)		I _{out} = 0.6 A, V _M = 24 V Analog t _{BLANK} value	200	300	400	ns
	t _{BLANK_AB} (H) t _{BLANK_CD} (H)		I _{out} = 0.6 A, f _{OSC_M} = 800 kHz f _{OSC_M} cycle × 3	4.0	5.0	6.0	μs
OSC_M reference signal oscillation frequency	f _{OSC_M}		C _{osc} = 220 pF	600	800	1000	kHz
Chopping frequency range	f _{chop}		Output active (I _{out} = 1.0 A)	40	100	150	kHz
Chopping frequency	f _{chop}		Output active (I _{out} = 0.6 A) OSC = 800 kHz	—	100	—	kHz

Mixed Decay Mode Current Waveform and Settings

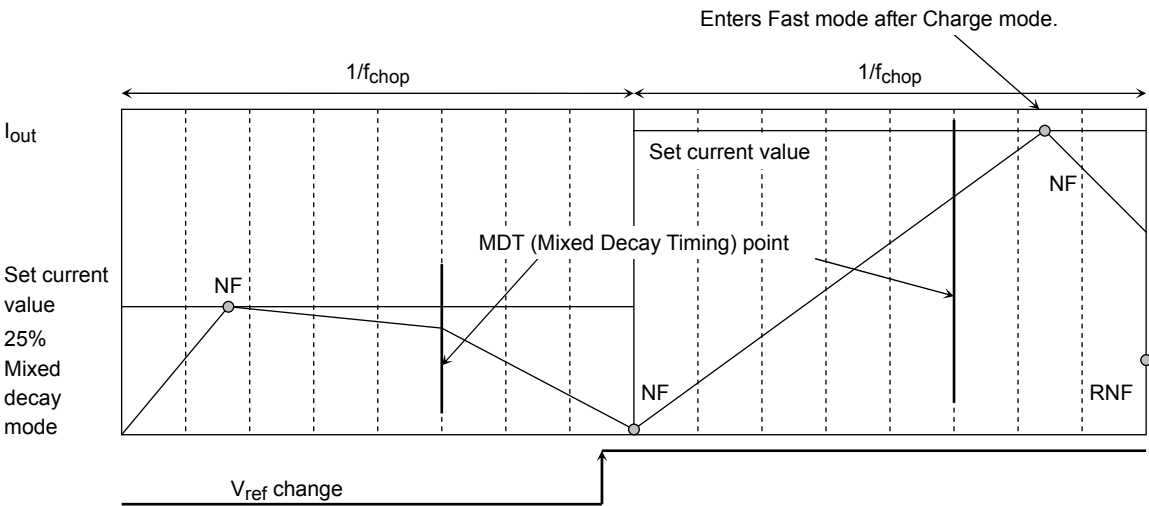
NF is the point where the output current reaches the set current value. When controlling the constant current, the Mixed Decay Mode ratio that determines the current oscillation amplitude (pulsating current) is set to 37.5%.



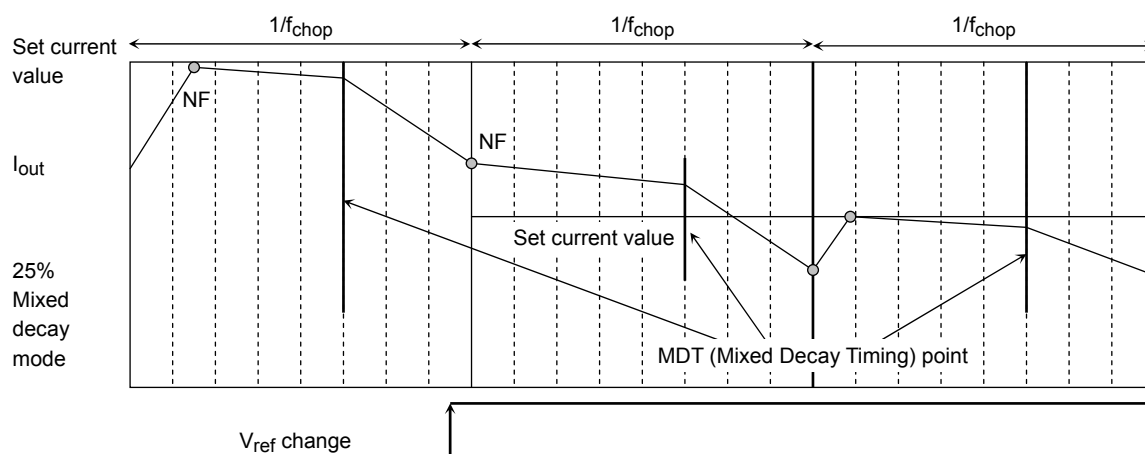
Mixed Decay Mode Waveform (Current waveform)



When NF Point Comes after the Mixed Decay Timing



When Output Current > Set Current in Mixed Decay Mode



Calculation of Set Current

Determining R_{RS} and V_{ref} determines the set current value.

$$I_{out} = V_{ref (gain)} \times \frac{V_{ref} (V)}{R_{RS} (\Omega)}$$

$V_{ref (gain)}$: V_{ref} attenuation ration is 1/5.0 (typ.)

For example, when

$$V_{ref} = 1.5 \text{ V}, R_{RS} = 1.0 \Omega,$$

The value of the motor constant current (Peak current) can be obtained as follows.

$$I_{out} = 1.5 \text{ V} / 5.0 / 1.0 \Omega = 0.30 \text{ A}$$

Calculating the Oscillation Frequency (Chopping reference frequency)

The OSC oscillation frequency (f_{osc}) and the chopping frequency (f_{chop}) can be calculated by the following formula:

$$f_{osc} = 61820 \times C \text{ (pF)}^{-0.8043} \text{ (kHz)}$$

When $C_{osc} = 220 \text{ pF}$ is connected, $f_{osc} = 810 \text{ kHz}$.

At this time, the actual chopping frequency of the stepping motor is 1/8 the OSC oscillation frequency, which is, $810/8 = 101 \text{ kHz}$.

IC Power Dissipation

IC power dissipation is classified into two: power consumed by transistors in the output block and power consumed by the logic block and the charge pump circuit.

Power Consumed by the Power Transistor (calculated with $R_{on} = 2.2 \Omega$ which is the total R_{on} of upper and lower transistor)

Power is consumed by the upper and lower transistors of the H-bridges. The following formula expresses the power consumed by the transistors of a single H-bridge.

$$P \text{ (out)} = I_{out} \text{ (A)} \times V_{DS} \text{ (V)} \times \text{H-switch} \times 2 = I_{out}^2 \times R_{on} \text{ (upper/lower)} \times \text{H-switch} \times 2 \dots\dots\dots (1)$$

The average power dissipation for output under 2-phase excitation operation when the output current waveform becomes the perfect rectangular waveform can be calculated as follows.

Under the conditions of $R_{on} \text{ (upper/lower)} = 2.2 \Omega$ (@1.0 A), $I_{out} \text{ (Peak: Max)} = 0.6 \text{ A}$, $V_M = 24 \text{ V}$,

$$\begin{aligned} P \text{ (out unit)} &= 0.6 \text{ (A)}^2 \times 2.2 \text{ (}\Omega\text{)} \times \text{H-switch} \times 2 \dots\dots\dots (2) \\ &= 1.584 \text{ (W)} \end{aligned}$$

Power Consumed by the Logic Block and IM

Power dissipation of the logic block and IM is calculated as follows by separating it into the one at operation and the one at stop.

$$I \text{ (IM2)} = 8.0 \text{ mA (typ.): at operation}$$

Output section (total of current consumed by the circuits connected to V_M and current consumed by output switching) is connected to V_M (24 V).

Power dissipation is calculated as follows:

$$\begin{aligned} P \text{ (IM)} &= 24 \text{ (V)} \times 0.008 \text{ (A)} \dots\dots\dots (3) \\ &= 0.192 \text{ (W)} \end{aligned}$$

Power Dissipation

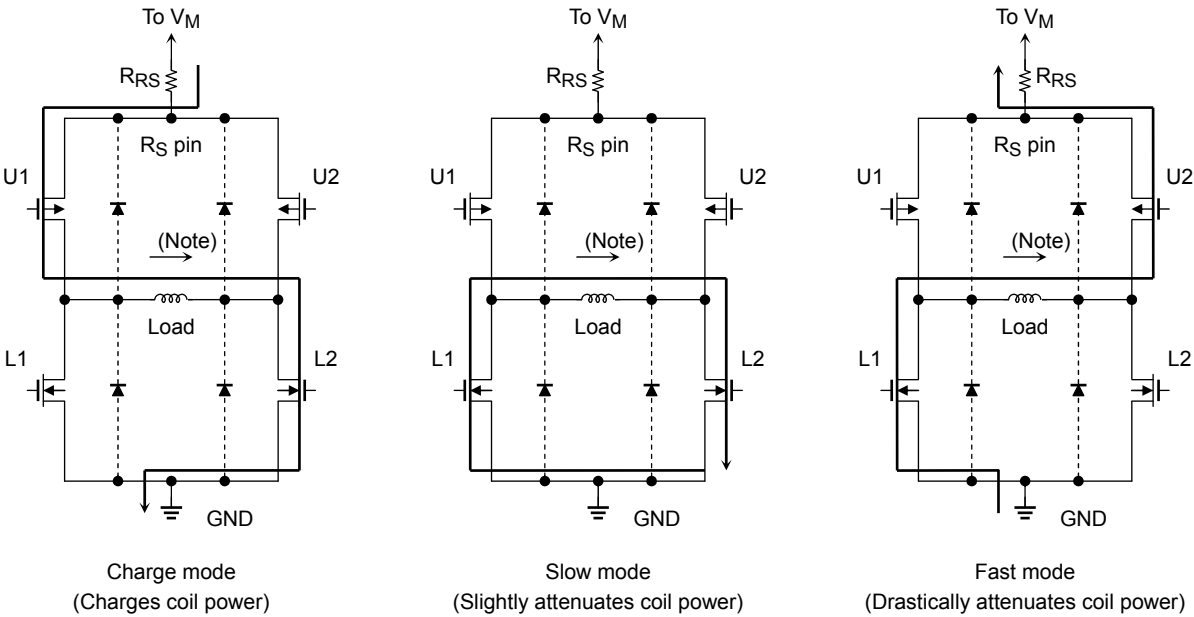
Thus, power dissipation for a single unit (P) is determined as follows by (2) and (3) above.

$$P = P \text{ (out unit)} + P \text{ (IM)} = 1.776 \text{ (W)}$$

In the actual motor current, the effective current changes depending on the rotation frequency, which causes the consumption current to change.

For thermal design on the board, evaluate by mounting the IC and complete the design with adequate margin.

Output Transistor Operating Mode



Output Transistor Operation Functions

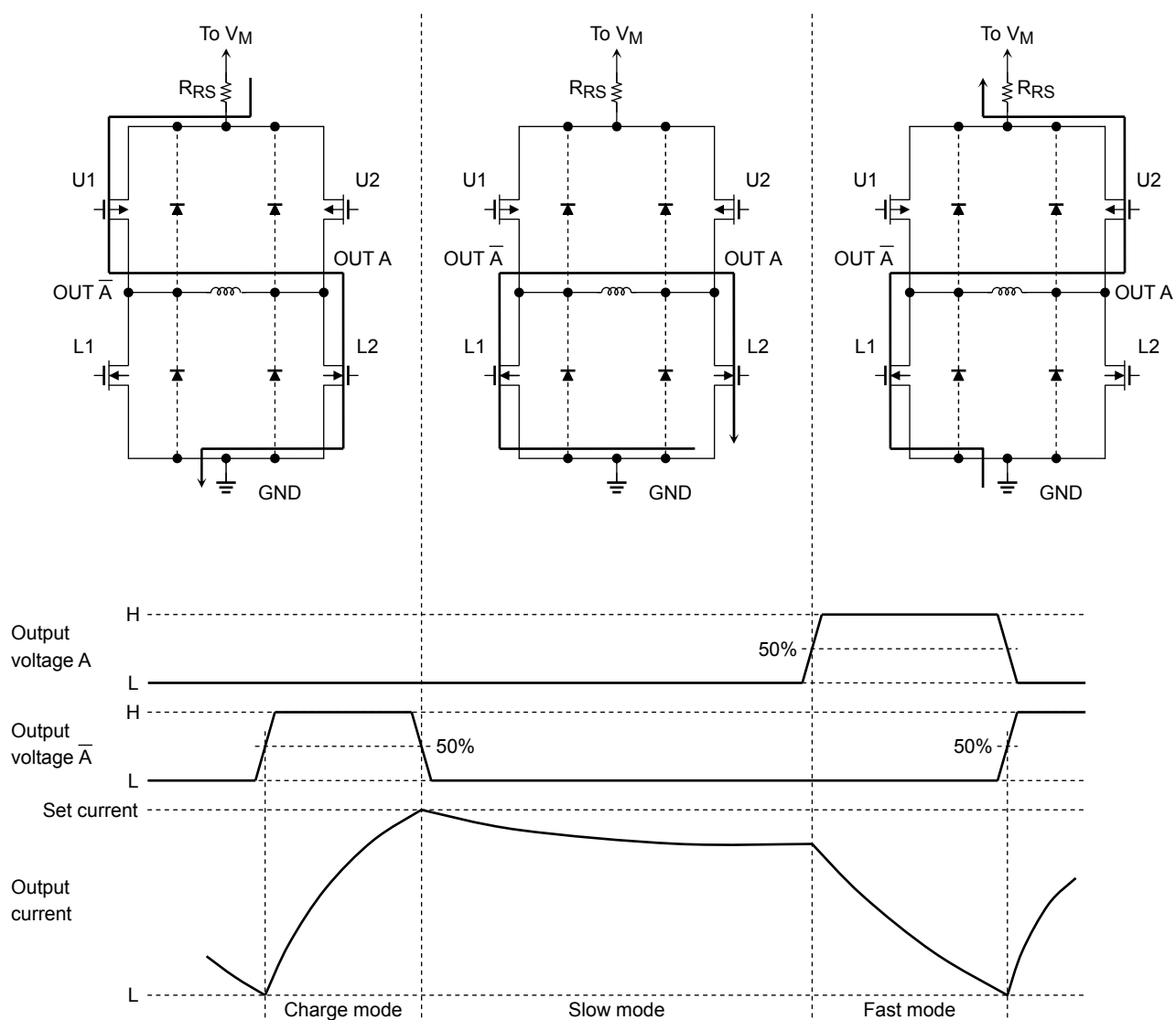
Mode	U1	U2	L1	L2
Charge	ON	OFF	OFF	ON
Slow	OFF	OFF	ON	ON
Fast	OFF	ON	ON	OFF

Note: The above table is an example where current flows in the direction of the arrows in the above figures.
When the current flows in the opposite direction, see the table below.

Mode	U1	U2	L1	L2
Charge	OFF	ON	ON	OFF
Slow	OFF	OFF	ON	ON
Fast	ON	OFF	OFF	ON

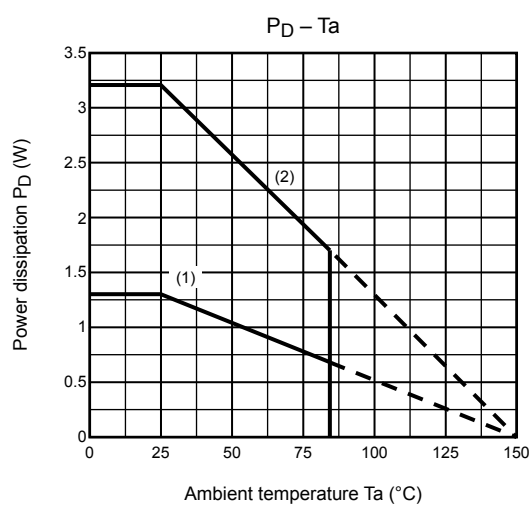
Output Transistor Operation Mode 2

Sequence of Mixed Decay Mode



The constant current is controlled by changing mode from Charge → Slow → Fast

$P_D - T_a$ (Package Power Dissipation)

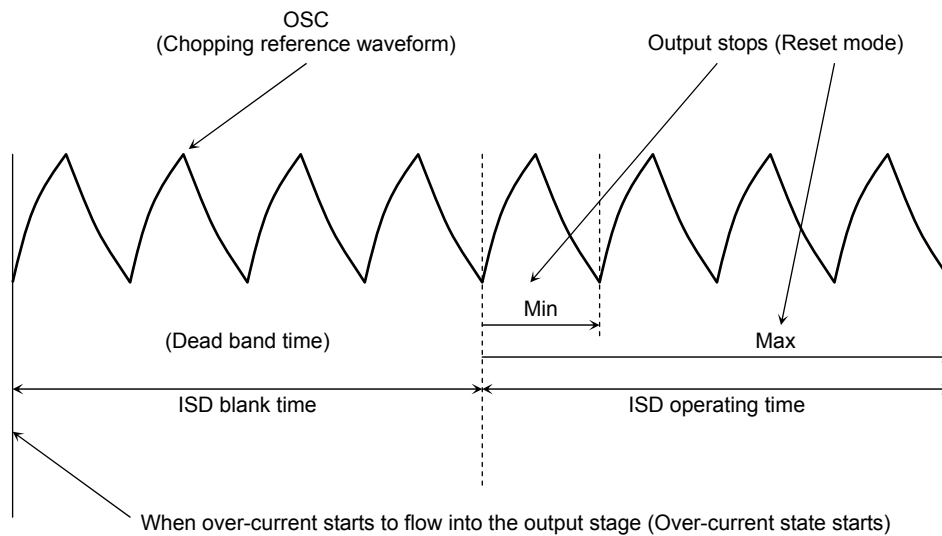


(1) IC only: $R_{th(j-a)}$: 113°C/W

(2) When mounted on the board (100 mm × 200 mm × 1.6 mm) : 37°C/W typ.

Operating Time for Over-current Detection Circuit

ISD Dead Band Time and ISD Operating Time



The over-current detection circuit has a dead band time to prevent erroneous detection of IRR or spike current at switching. The dead band time being synchronized with the frequency of the OSC for setting chopping frequency is expressed as follows.

$$\text{Dead band time} = 4 \times \text{OSC cycle}$$

Time required to stop the output after over-current flows into the output stage is expressed as follows.

$$\text{Minimum time} = 5 \times \text{OSC cycle (Including the maximum value of synchronization time of one OSC cycle)}$$

$$\text{Maximum time} = 8 \times \text{OSC cycle}$$

Note that the above-mentioned operating times are achieved only when over-current flows as it is expected. Depending on the timing of output control mode, the circuit may not be triggered.

Thus, to ensure safe operation, please insert a fuse in the motor power supply.

The capacity of the fuse is determined according to the usage conditions. Please select one whose capacity does not exceed the power dissipation for the IC to avoid any operating problems.

tBLANK (noise rejection dead band time)

The TB62212FTAG incorporates two different dead band times (blank times) for different motors to be driven so as to prevent malfunctions because of switching noise.

1. Analog tBLANK Functions

The noise rejection dead band time (analog tBLANK) defined by the AC characteristics of the motor block is fixed within the IC. It is mainly used to avoid misjudging the IRR (diode recovery current) when a stepping motor is driven by constant current.

It is fixed within the IC and thus cannot be altered.

2. Digital tBLANK (in Brushed DC Motor mode)

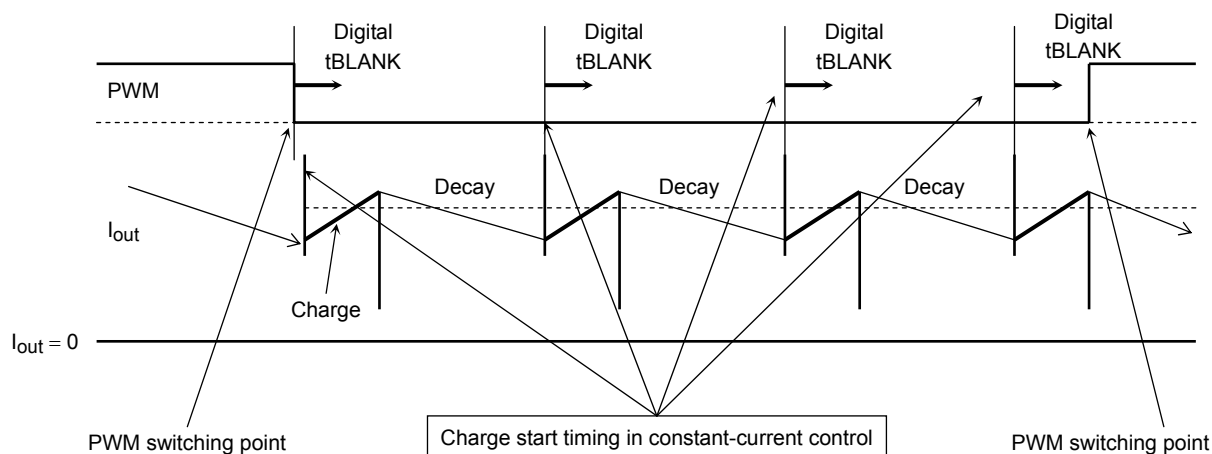
Unlike the analog tBLANK, the digital tBLANK time, specified when the initial setup mode is selected, is generated digitally from an external chopping period. This blank time is used to prevent false detections of over-current conditions due to recovery currents of a varistor generated during PWM operation of DC motors in DC Motor mode.

When Stepping Motor mode is selected via the mode select pins, the digital tBLANK time is nullified (0 μ s) and the analog tBLANK time, which is internally fixed, becomes effective.

Since this blank time is generated based on the OSC_M signal, the time can be adjusted by changing the OSC_M signal frequency.

(Please note that the characteristics other than the blank time, such as motor chopping frequency and the dead band time inserted at power on, are also changed when the OSC_M signal frequency is changed.)

Digital tBLANK Insertion Timing in Brushed DC Motor Mode



The digital tBLANK time is inserted immediately after the switching timing of externally applied PWM signals, IN1, IN2 and SB (such as the switching timing between short brake and charging), and also when the charging in constant-current chopper drive is started.

The digital tBLANK time becomes effective only in DC Motor mode.

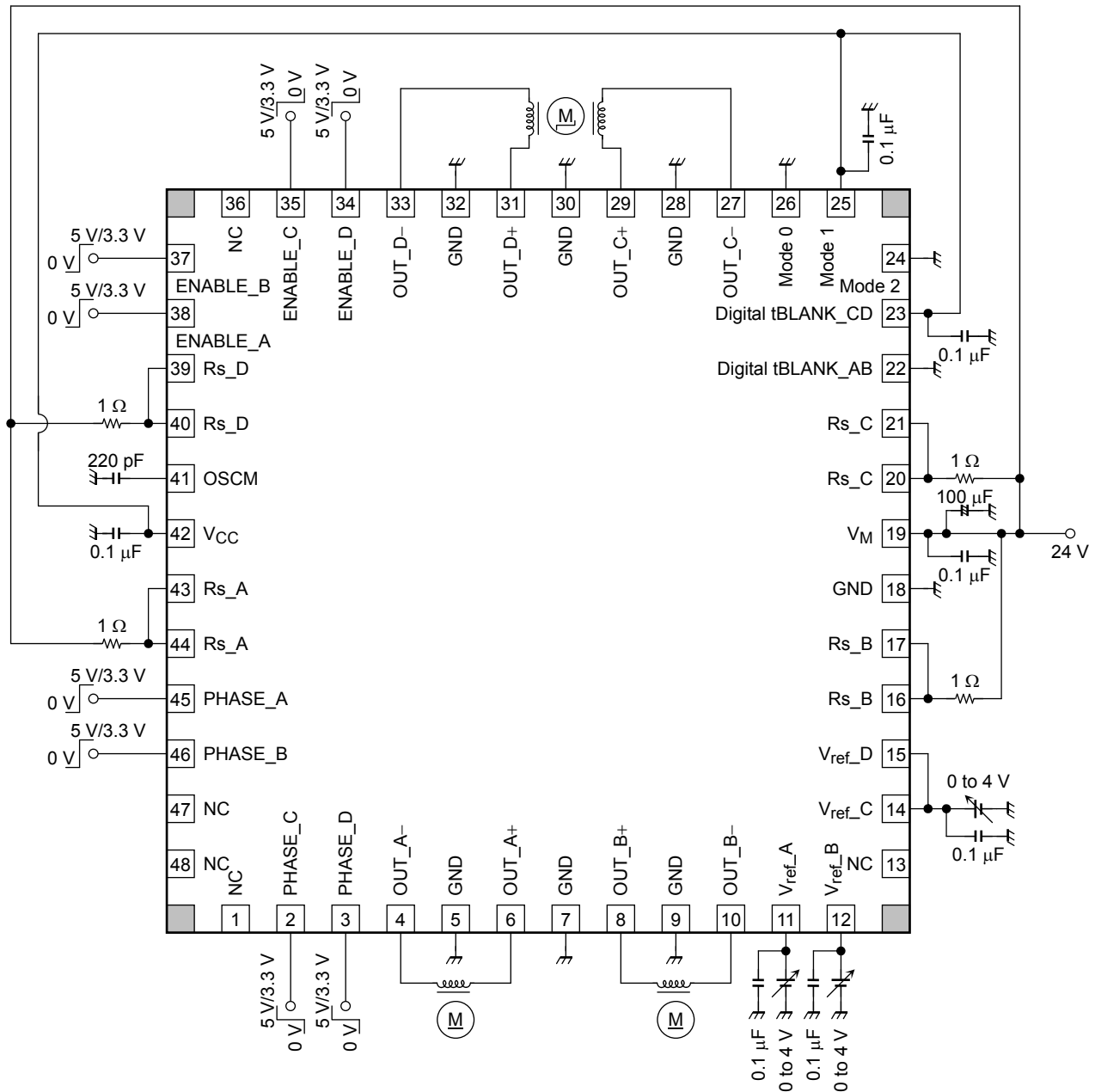
The TB62212FTAG enters 37.5% Mixed-Decay mode when starting DC motor operation. In this mode, the TB62212FTAG stays in Charge mode for the first 3 CLK cycles of the whole period, which is also a digital tBLANK time. Thus, depending on the timing, operation mode might be switched directly to Fast-Decay mode.

Application Circuit

The values for the respective devices are all recommended values.

For values under each input condition, see the above-mentioned operating ranges.

(In this example, $V_{ref} = 1.5\text{ V}$, $f_{chop} = 100\text{ kHz}$, Motor 1: 0.3 A, Motor 2: 0.3 A)



Note: Adding bypass capacitor is recommended if necessary.

Make sure that GND wiring has only one contact point.

To input the data, see the section on the recommended input data.

If the signal setting is inappropriate, an unexpected large current may flow, causing damage to the IC.

The IC may be destroyed due to short-circuit between output pins, to supply, or to ground. Design an output line, V_{CC} (V_M) line and GND line with great care. Also, extremely high voltage will be applied to the IC when the IC is mounted in the wrong orientation, which causes the IC to be destroyed. Always confirm the pin assignment and the position of pin 1 before mounting and using the IC.

QFN48-P-0707-0.5

Chamfer radius: 3-R0.2

Notes on Contents**1. Block Diagrams**

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations**Notes on Handling of ICs**

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.
- (3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.

If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, over-current or IC failure can cause smoke or ignition. (The over-current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs**(1) Over-current Protection Circuit**

Over-current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over-current protection circuits operate against the over-current, clear the over-current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over-current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over-current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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