

DATA SHEET

74ABT16374B

16-bit D-type flip-flop;
positive-edge trigger (3-State)

Product data
Supersedes data of 2004 Mar 01

2004 Mar 08

16-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT16374B

DESCRIPTION

The 74ABT16374B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16374B has two 8-bit, edge triggered registers, with each register coupled to eight 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-LOW Output Enable (nOE) controls all eight 3-State buffers for its register independent of the clock operation.

When nOE is LOW, the stored data appears at the outputs for that register. When nOE is HIGH, the outputs for that register are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

FEATURES

- Two 8-bit positive edge triggered registers
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State output buffers
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	C _L = 50 pF; V _{CC} = 5 V	2.6 2.2	ns
C _{IN}	Input capacitance	V _I = 0 V or V _{CC}	4	pF
C _{OUT}	Output capacitance	V _O = 0V or V _{CC} ; 3-State	7	pF
I _{CCZ}	Quiescent supply current	Outputs disabled; V _{CC} = 5.5 V	500	μA
I _{CCL}		Outputs LOW; V _{CC} = 5.5 V	8	mA

ORDERING INFORMATION

T_{amb} = –40 °C to +85 °C

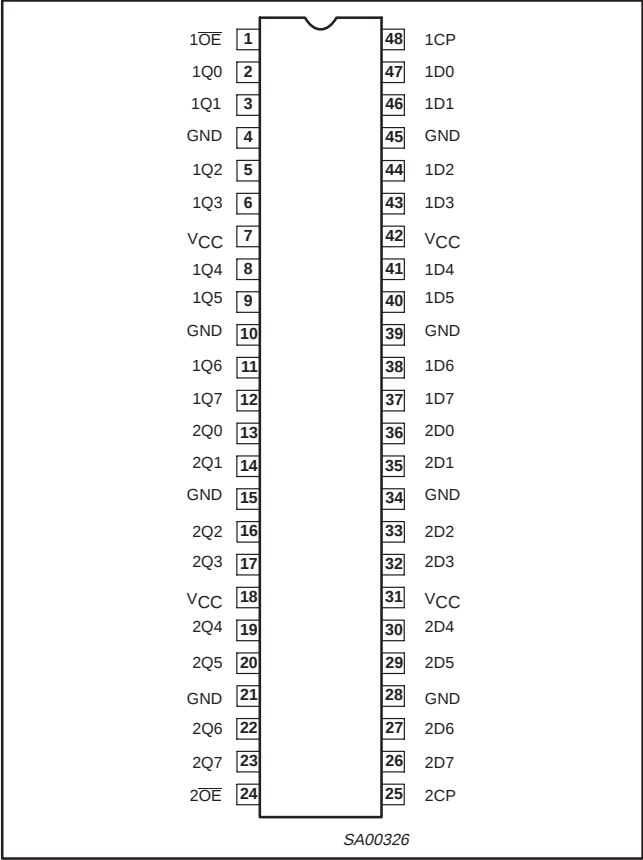
Type number	Package		
	Name	Description	Version
74ABT16374BB	QFP52	plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 × 10 × 2.0 mm	SOT379-1
74ABT16374BDGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABT16374BDL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

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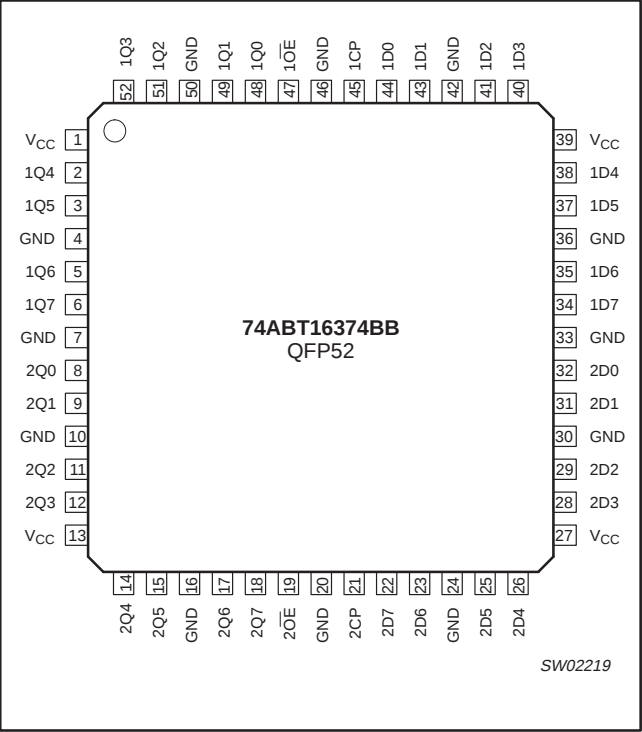
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PIN CONFIGURATION

TSSOP48 and SSOP48 pinning



QFP52 pinning



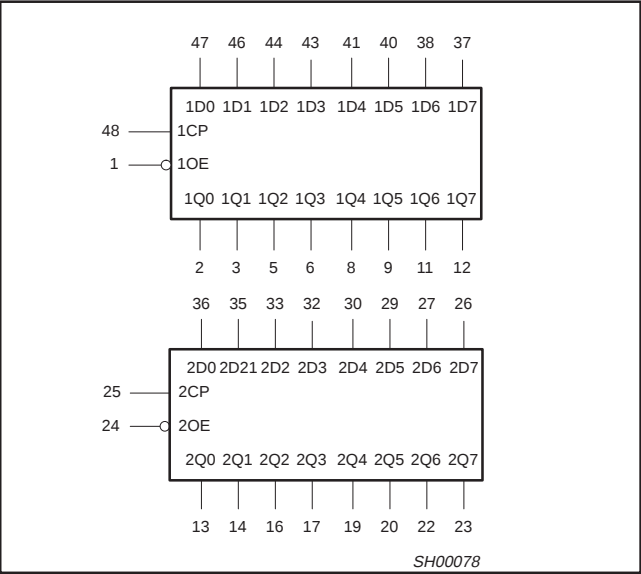
PIN DESCRIPTION

PIN NUMBER		SYMBOL	FUNCTION
TSSOP and SSOP	QFP52		
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	47, 19	1OE, 2OE	Output enable inputs (active-LOW)
48, 25	45, 21	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0 V)
7, 18, 31, 42	1, 13, 27, 39	VCC	Positive supply voltage

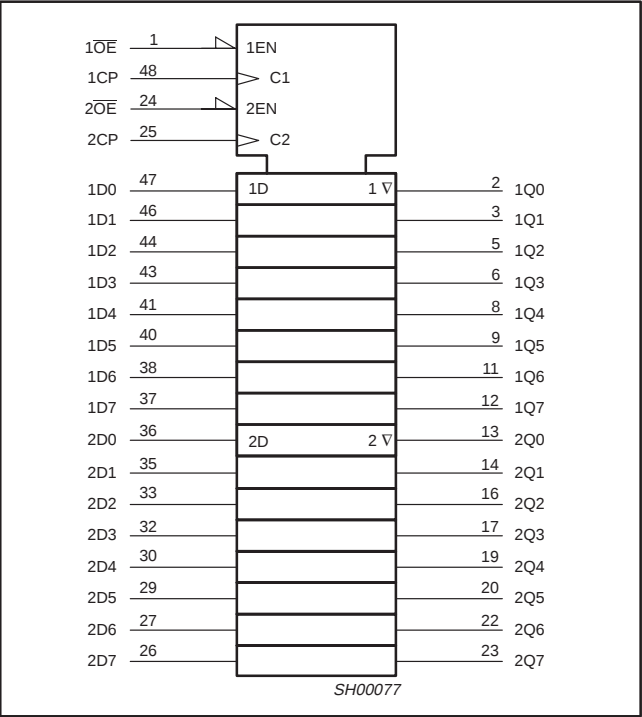
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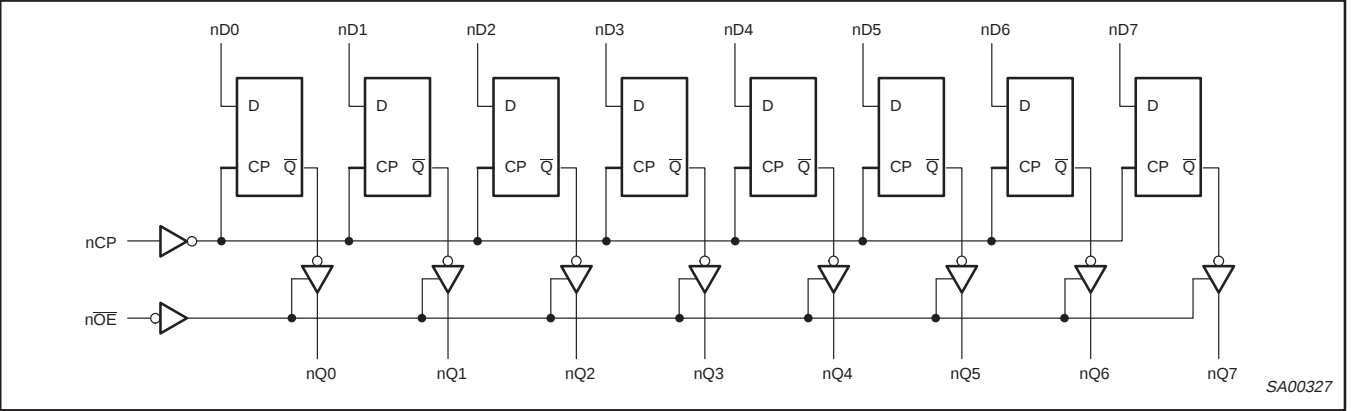
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nCP	nDx		nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↑	X	NC	NC	Hold
H H	↑ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = HIGH voltage level
h = HiIGH voltage level one set-up time prior to the HIGH-to-LOW E transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition
NC= No change
X = Don't care
Z = High-impedance "off" state
↑ = LOW-to-HIGH clock transition
↑ = Not a LOW-to-HIGH clock transition

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	−18	mA
V_I	DC input voltage ³		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	−50	mA
V_{OUT}	DC output voltage ³	output in Off or HIGH state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	−64	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	−32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25 °C			T _{amb} = −40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = −18 mA	—	−0.9	−1.2	—	−1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9	—	2.5	—	V
		V _{CC} = 5.0 V; I _{OH} = −3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4	—	3.0	—	V
		V _{CC} = 4.5 V; I _{OH} = −32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4	—	2.0	—	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}	—	0.42	0.55	—	0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}	—	0.13	0.55	—	0.55	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	—	0.01	±1	—	±1	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V	—	±5.0	±100	—	±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = GND	—	±5.0	±50	—	±50	μA
I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}	—	0.5	10	—	10	μA
I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}	—	−0.5	−10	—	−10	μA
I _{CEX}	Output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	—	5.0	50	—	50	μA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	−50	−70	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs HIGH; V _I = GND or V _{CC}	—	0.5	2	—	2	mA
I _{CCL}		V _{CC} = 5.5 V; Outputs LOW; V _I = GND or V _{CC}	—	8	19	—	19	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}	—	0.5	2	—	2	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND	—	5	100	—	100	μA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$ a transition time of up to 100 μsec is permitted.
- Unused pins at V_{CC} or GND .

AC CHARACTERISTICS

$\text{GND} = 0\text{ V}$, $t_R = t_F = 2.5\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = −40 to +85 °C V _{CC} = +5.0V ± 0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	180	260	—	—	—	MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.7 1.4	2.6 2.2	4.0 3.4	1.7 1.4	4.7 3.9	ns
t _{PZH} t _{PZL}	Output enable time to HIGH and LOW level	3 4	1.3 1.3	2.4 2.3	3.7 3.4	1.3 1.3	4.7 4.6	ns
t _{PHZ} t _{PLZ}	Output disable time from HIGH and LOW level	3 4	1.9 1.7	3.1 2.6	4.6 4.0	1.9 1.7	5.5 4.4	ns

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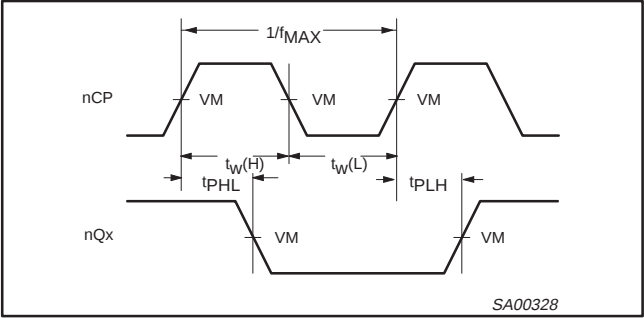
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F = 2.5 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \text{ }\Omega$

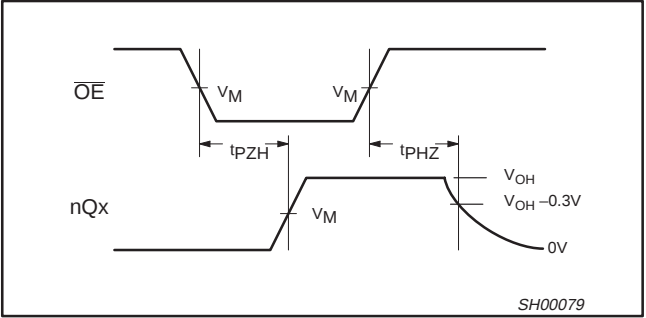
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25 \text{ }^\circ\text{C}$ $V_{\text{CC}} = +5.0 \text{ V}$		$T_{\text{amb}} = -40 \text{ to } +85 \text{ }^\circ\text{C}$ $V_{\text{CC}} = +5.0 \text{ V} \pm 0.5 \text{ V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Set-up time, HIGH or LOW nDx to nCP	2	1.0 1.0	0.3 0.1	1.0 1.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, HIGH or LOW nDx to nCP	2	1.0 1.0	-0.1 -0.3	1.0 1.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	nCP pulse width HIGH or LOW	1	2.8 2.8	1.2 1.5	2.8 2.8	ns

AC WAVEFORMS

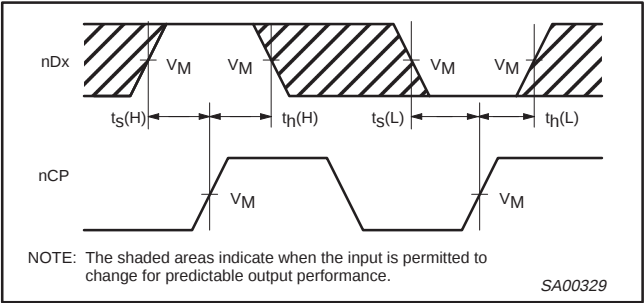
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



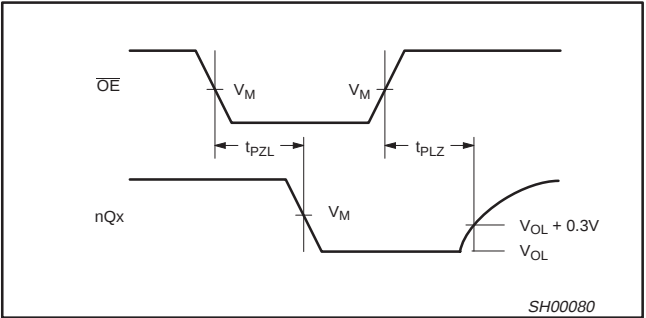
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level



Waveform 2. Data Set-up and Hold Times

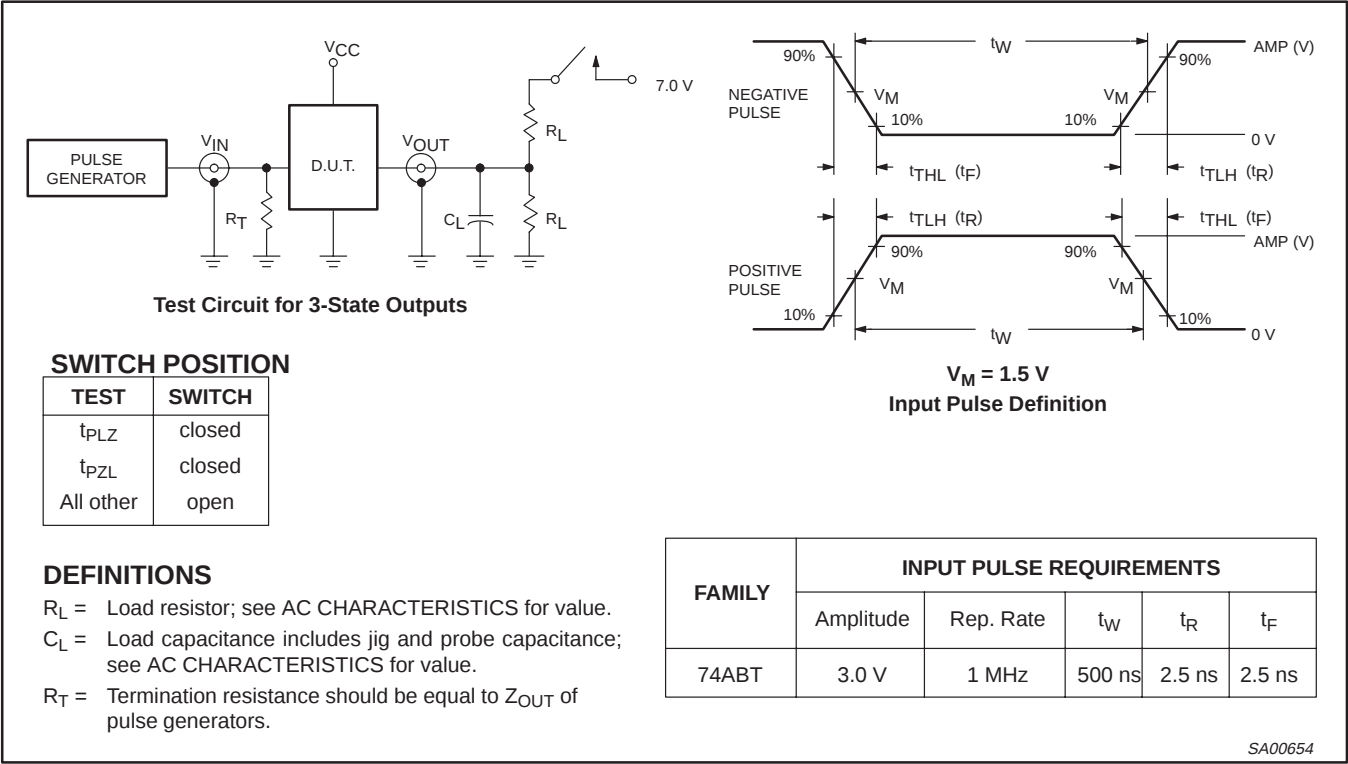


Waveform 4. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

16-bit D-type flip-flop; positive-edge trigger
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TEST CIRCUIT AND WAVEFORM

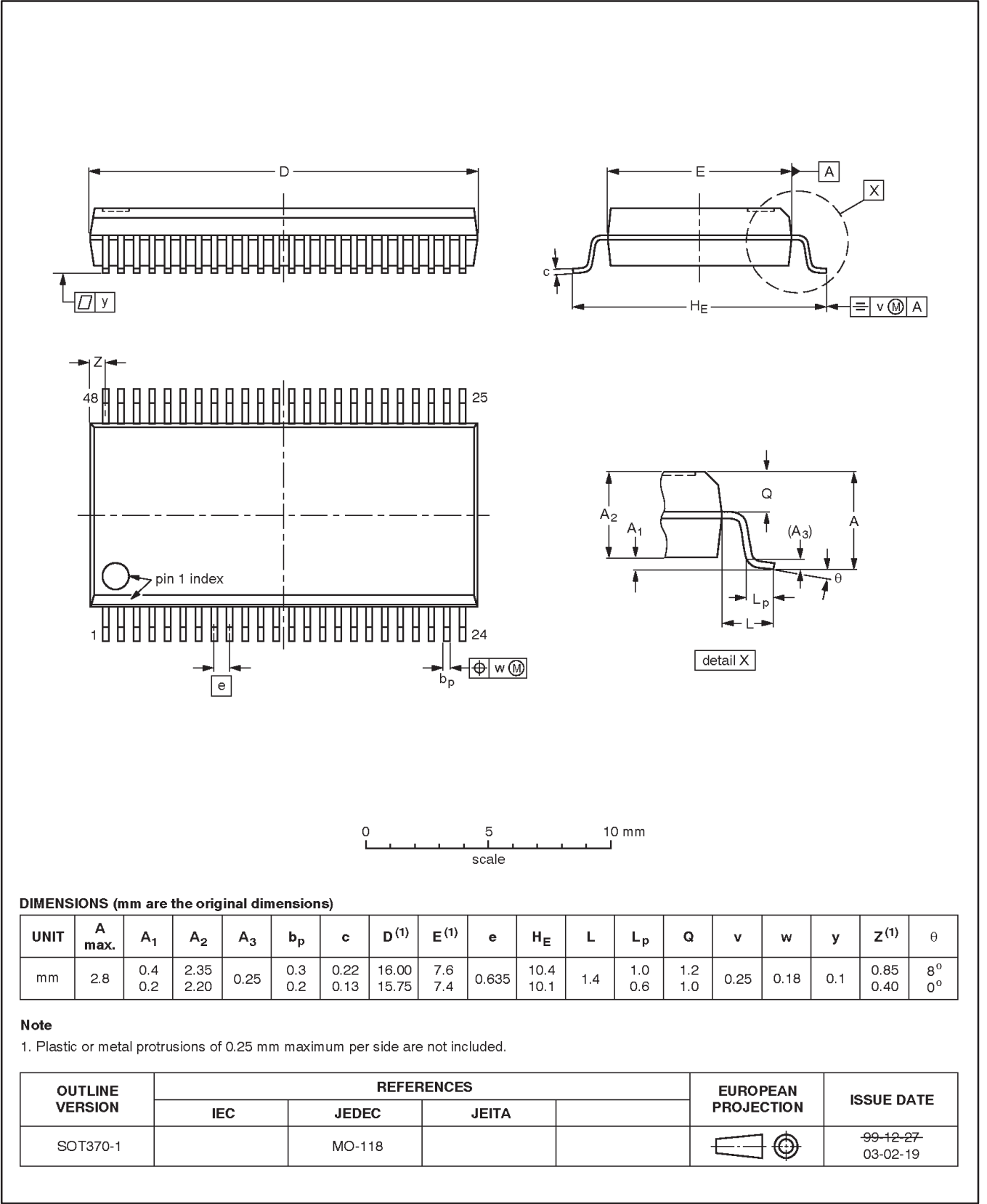


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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

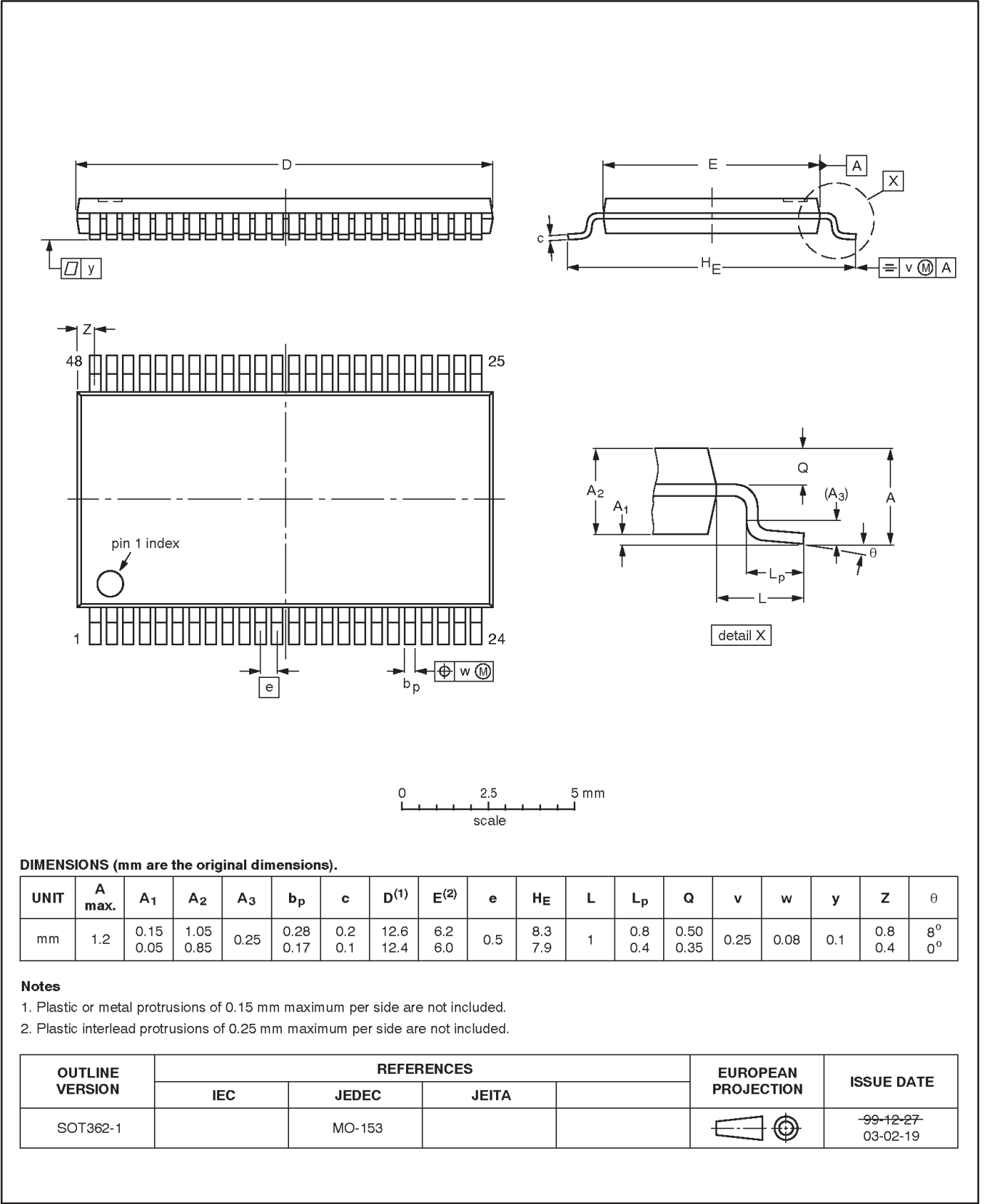


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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

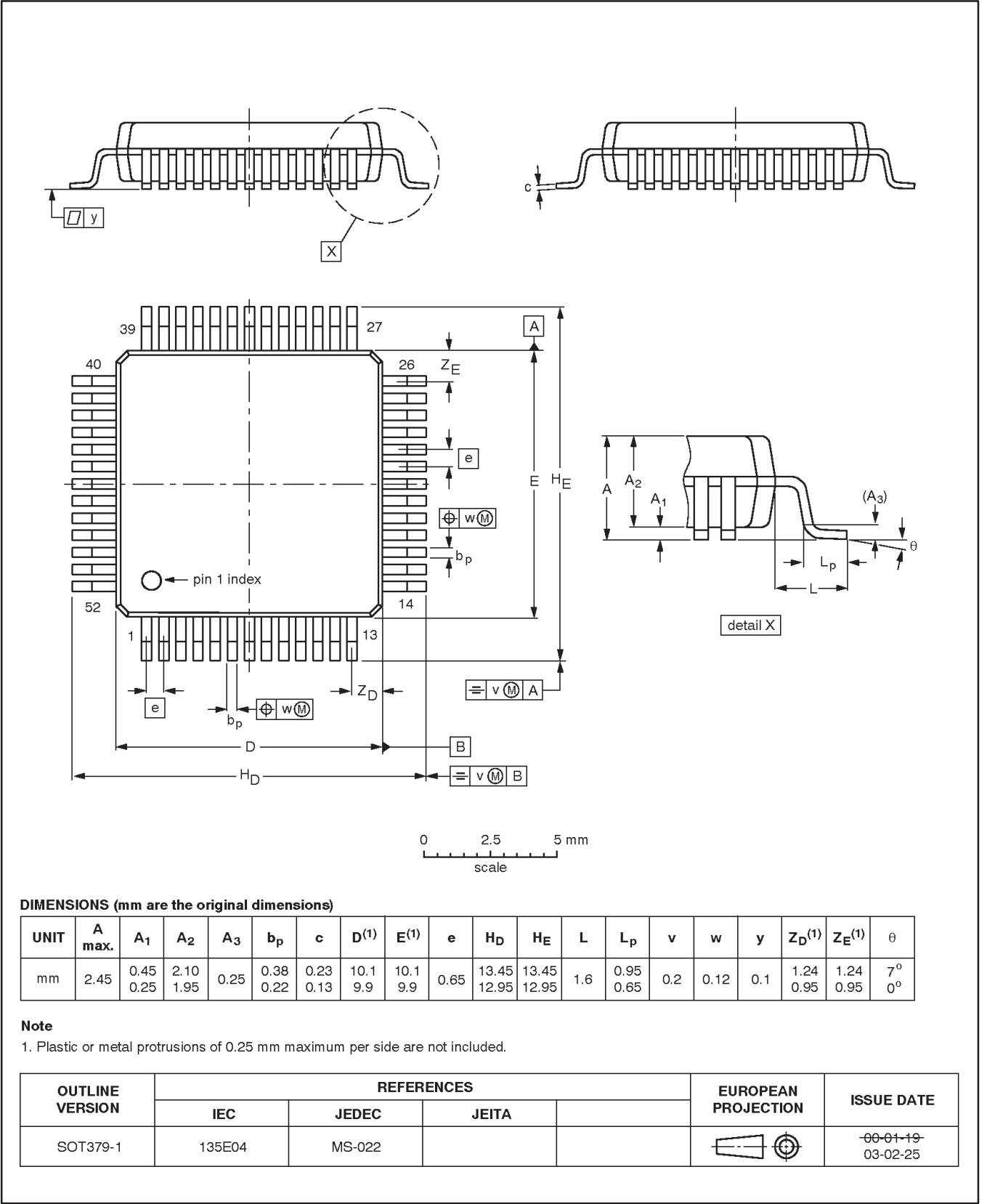


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QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



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REVISION HISTORY

Rev	Date	Description
_4	20040308	Product data (9397 750 13014). Supersedes data of 2004 Mar 01 (9397 750 12988). Modifications: ● Add type number 74ABT16374BB, QFP52 pin configuration, and SOT379-1 package outline.
_3	20040301	Product data (9397 750 12988); 853-1752 ECN 01–A15430 of 27 January 2004. Replaces data sheet 74ABT_H16374B_2 of 1998 Feb 27 (9397 750 03496).
_2	19980227	Product specification (9397 750 03496); ECN 853-1752 19027 of 27 February 1998. Supersedes data of 1995 Sep 28.
_1	19950928	

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Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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