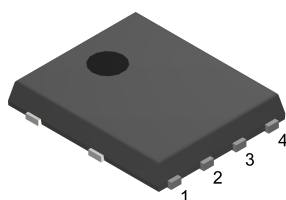
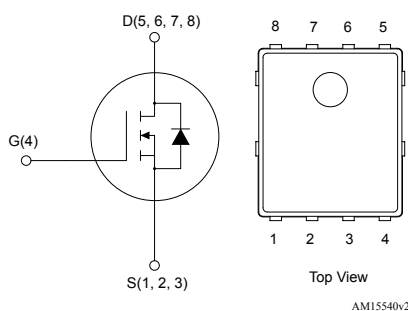


N-channel 100 V, 5 mΩ typ., 107 A, STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL110N10F7	100 V	6 mΩ	107 A	136 W

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link

[STL110N10F7](#)

Product summary

Order code	STL110N10F7
Marking	110N10F7
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	107	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	75	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	428	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	21	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	14	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	136	W
$P_{TOT}^{(3)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	490	mJ
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. This value is rated according to R_{thj-c} .
2. Pulse width limited by safe operating area.
3. This value is rated according to $R_{thj-pcb}$.
4. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 18\text{ A}$, $V_{DD} = 50\text{ V}$.

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.1	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

1. When mounted on an FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			10	
I_{GSS}	Gate body leakage current	$V_{DS} = 0$, $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		5	6	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	5117	-	pF
C_{oss}	Output capacitance		-	992	-	
C_{rss}	Reverse transfer capacitance		-	39	-	
Q_g	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 21\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	72	-	nC
Q_{gs}	Gate-source charge		-	30	-	
Q_{gd}	Gate-drain charge		-	17	-	

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	25	-	ns
t_r	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time		-	52	-	ns
t_f	Fall time		-	21	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 21\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 21\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	77		ns
Q_{rr}	Reverse recovery charge		-	150		nC
I_{RRM}	Reverse recovery current		-	4.3		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

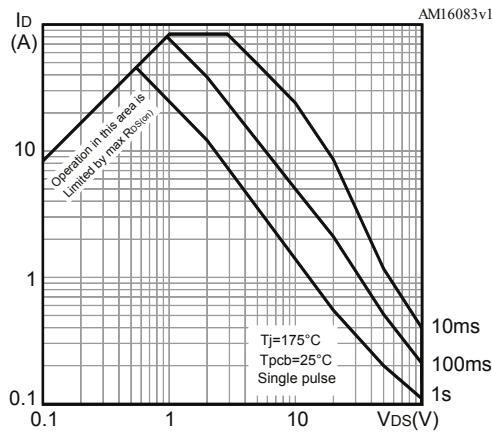
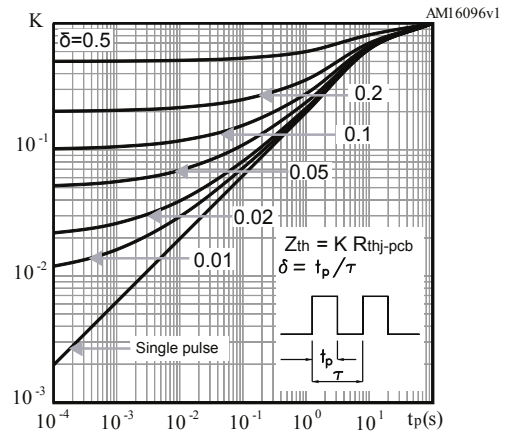
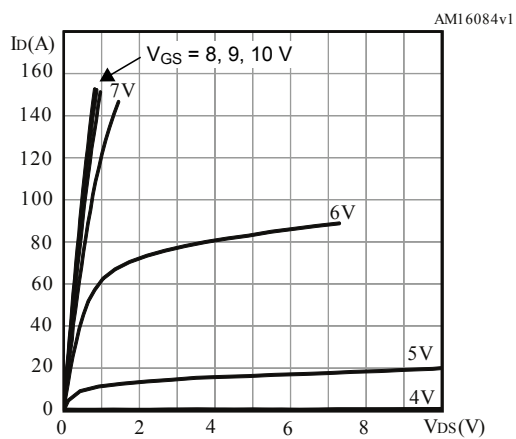
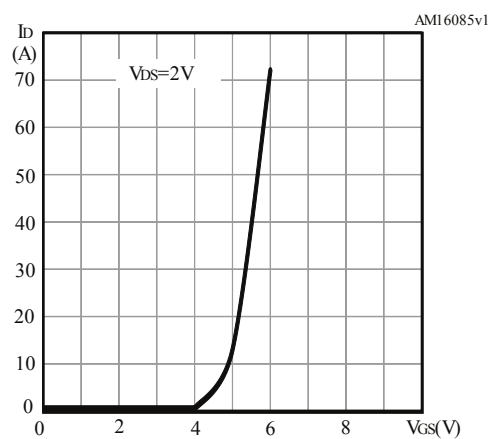
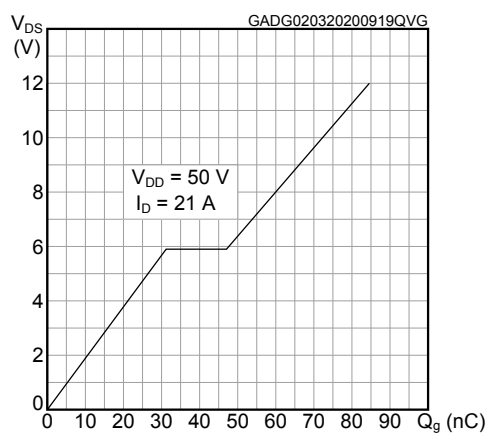
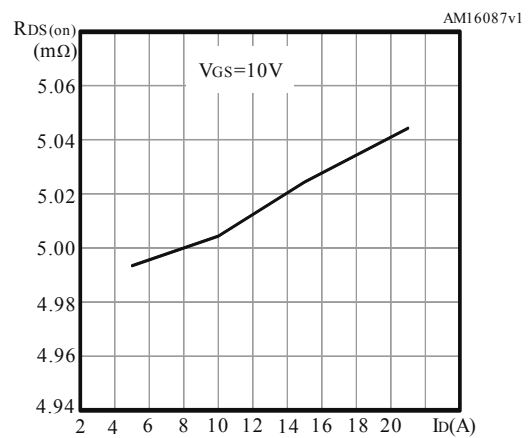
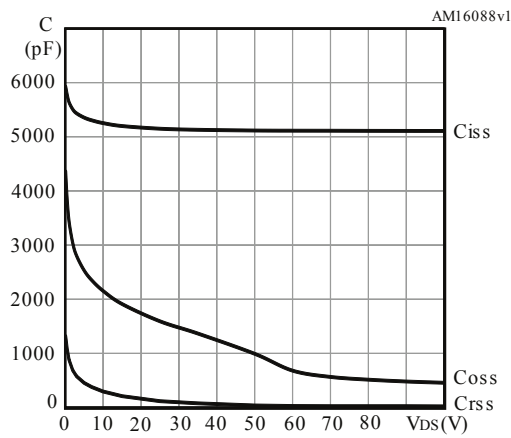
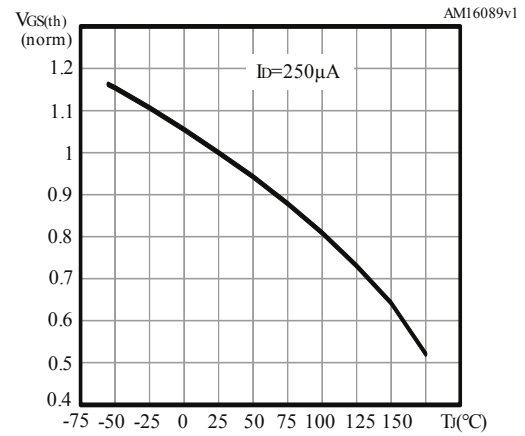
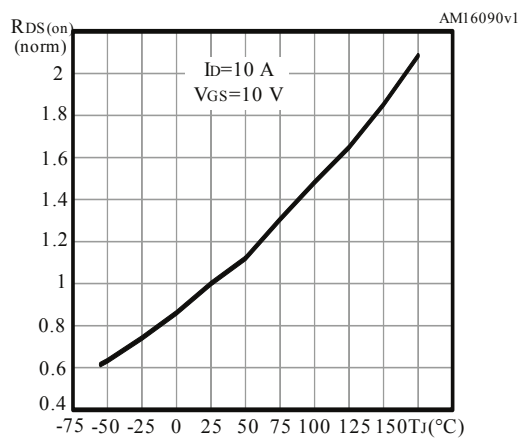
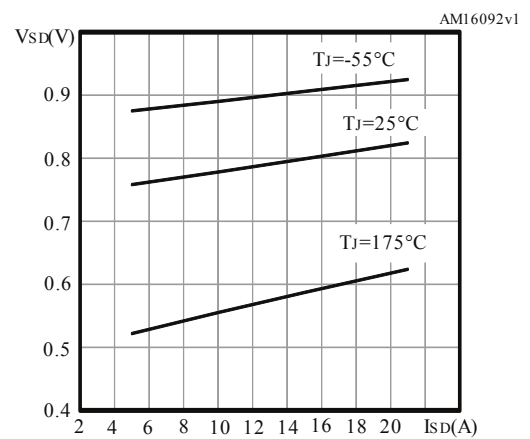
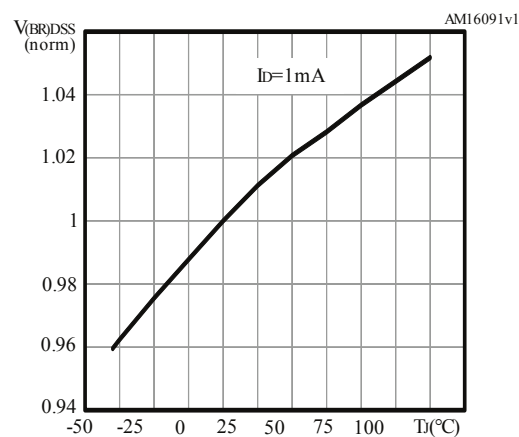
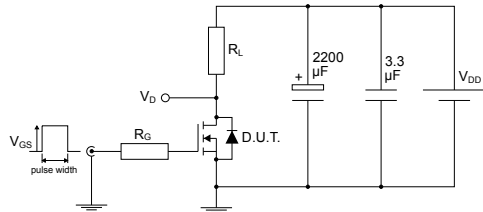
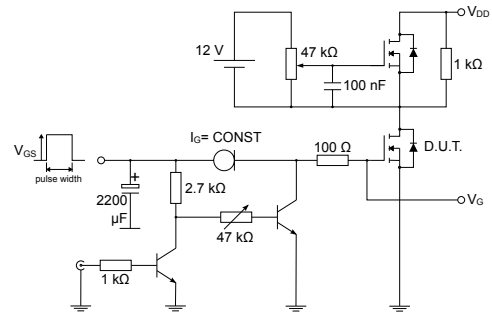
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Source-drain diode forward characteristics

Figure 11. Normalized V(BR)DSS vs temperature


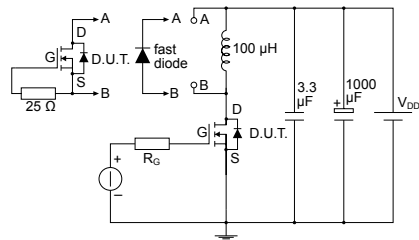
3 Test circuits

Figure 12. Test circuit for resistive load switching times


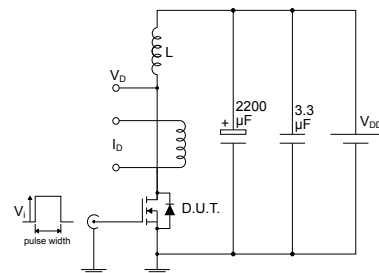
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Figure 13. Test circuit for gate charge behavior


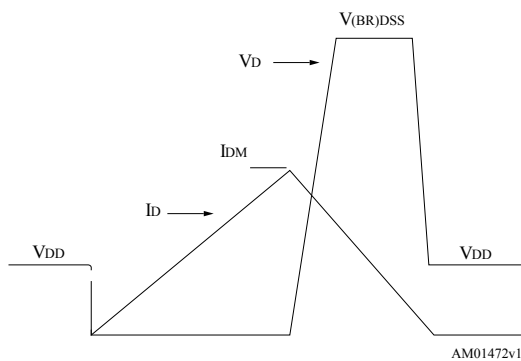
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Figure 14. Test circuit for inductive load switching and diode recovery times


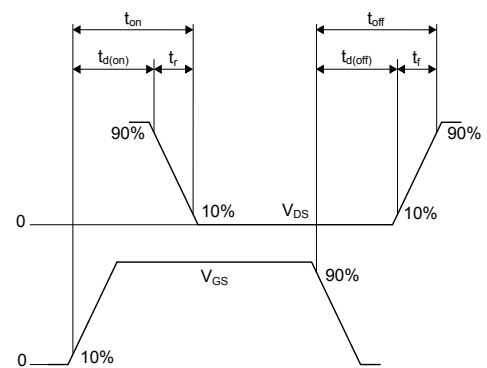
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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


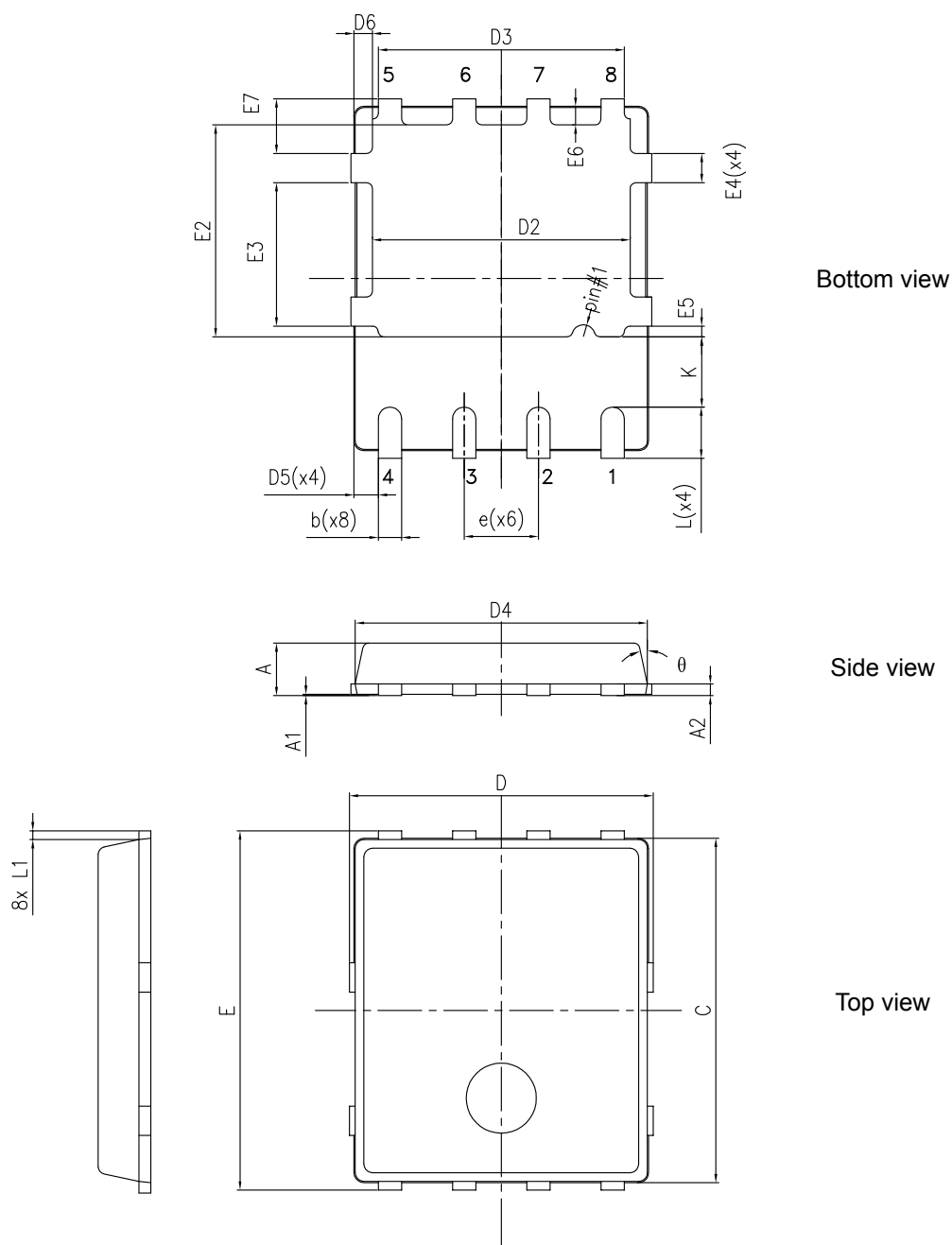
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type C package information

Figure 18. PowerFLAT 5x6 type C package outline

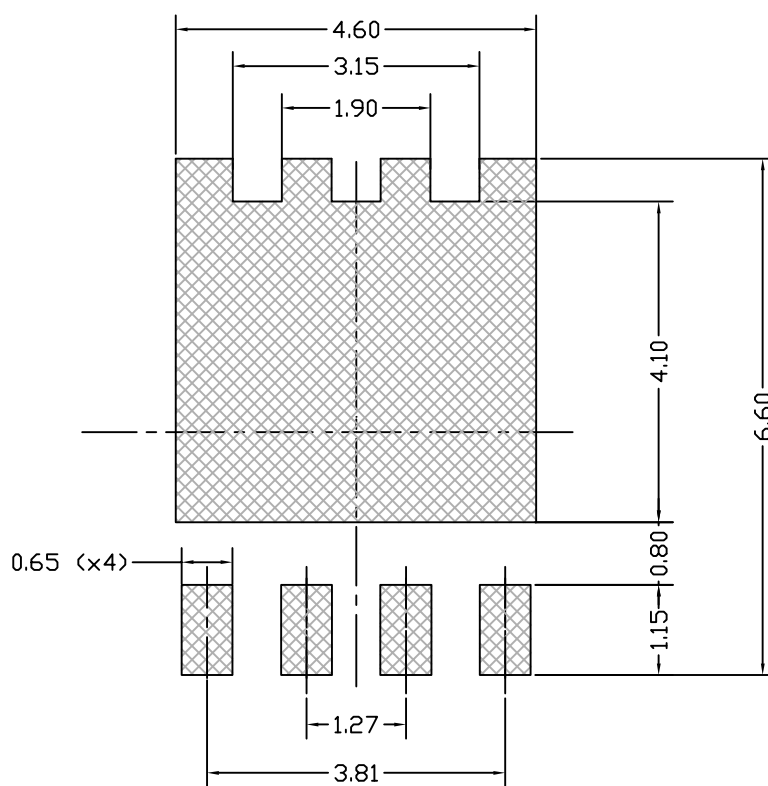


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Table 7. PowerFLAT 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

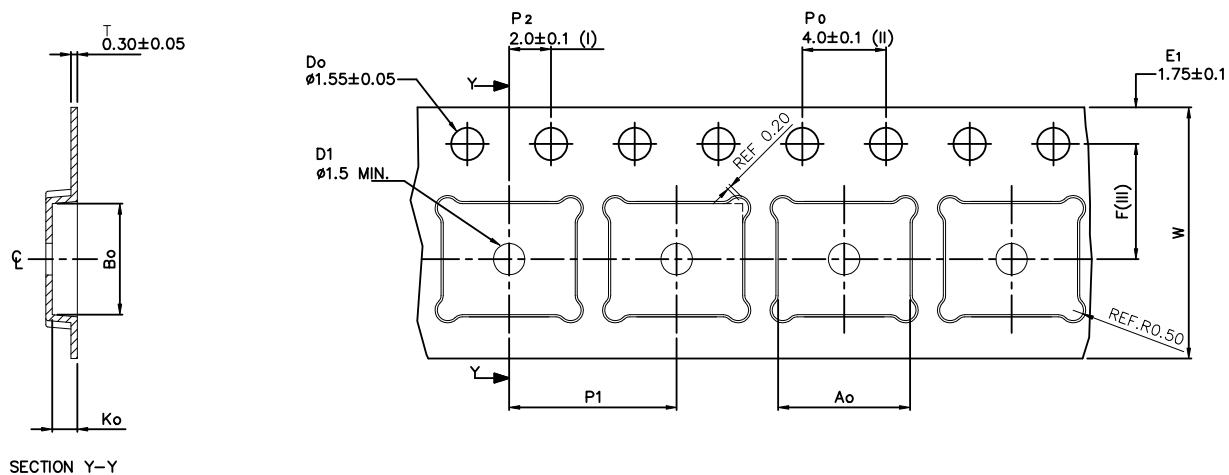
Figure 19. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_20

4.2 PowerFLAT 5x6 packing information

Figure 20. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30 +/− 0.1
Bo	5.30 +/− 0.1
Ko	1.20 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 21. PowerFLAT 5x6 package orientation in carrier tape

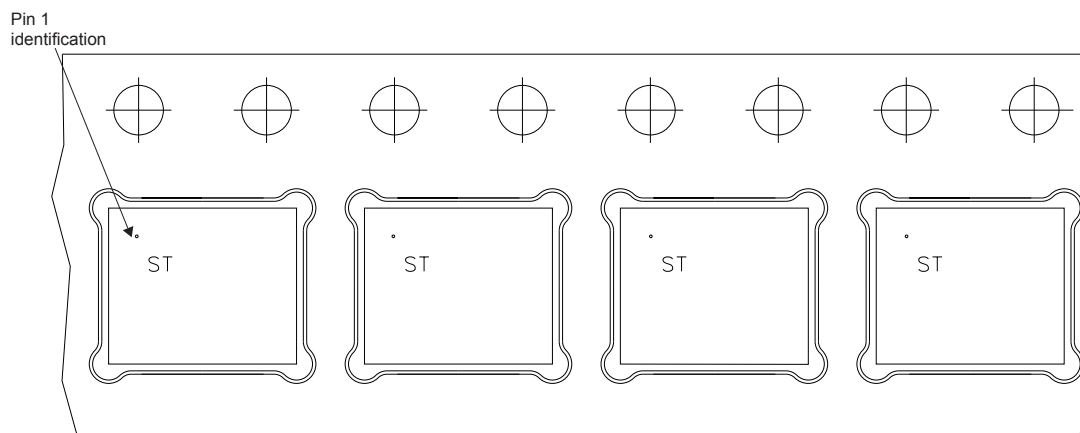
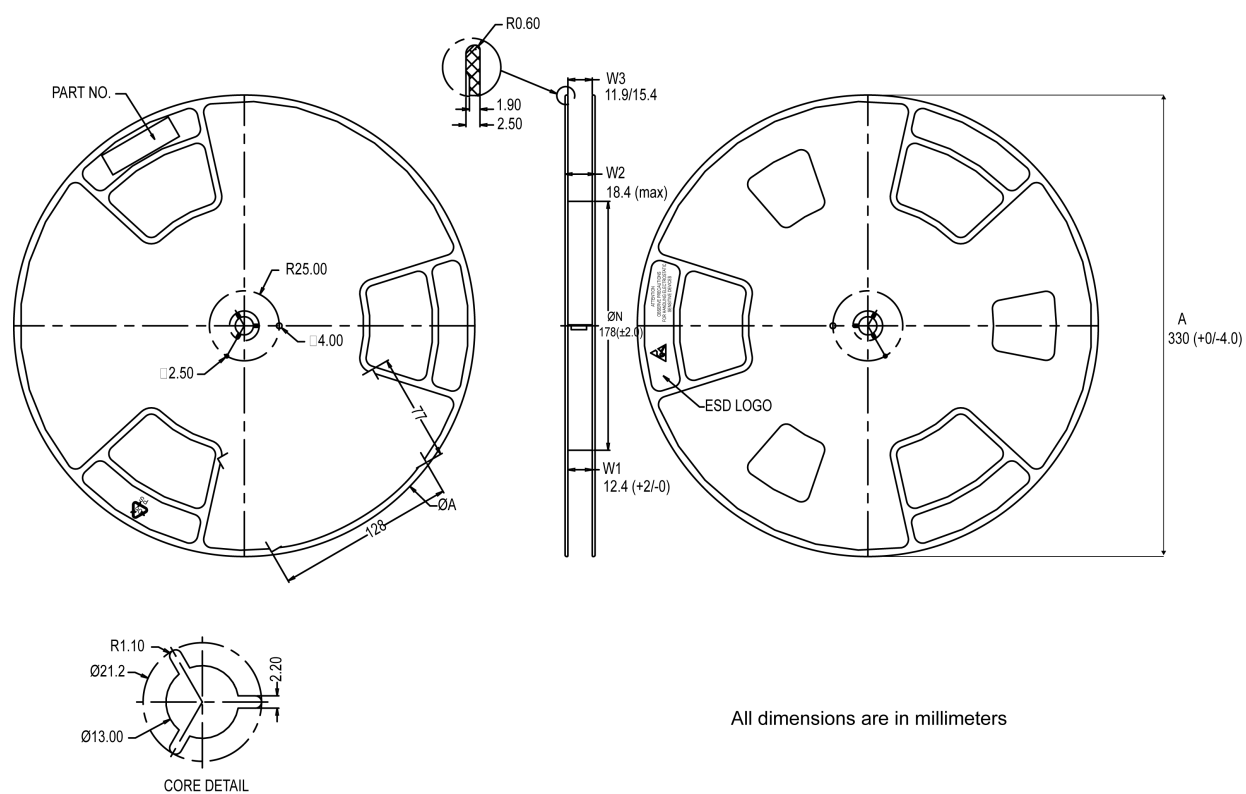


Figure 22. PowerFLAT 5x6 reel



8234350_Reel_rev_C

Revision history

Table 8. Document revision history

Date	Revision	Changes
03-Dec-2012	1	First release.
12-Dec-2013	2	Modified: P_{TOT} value and <i>Figure 1</i> in cover page Modified: I_D , I_{DM} and P_{TOT} values in <i>Table 2</i> Added: E_{AS} value in <i>Table 2</i> Modified: all values in <i>Table 3</i> Modified: I_{DSS} , I_{GSS} and I_D for $R_{DS(on)}$ Updated: the entire typical values in <i>Table 5</i> , <i>6</i> and <i>7</i> Updated: <i>Figure 13</i> , <i>14</i> , <i>15</i> and <i>16</i> Minor text changes
25-Mar-2014	3	Updated title and features on cover page. Added P_{TOT} value at $T_C = 25\text{ °C}$ in <i>Table 2: Absolute maximum ratings</i> . Updated <i>Section 4: Package mechanical data</i> .
20-Aug-2014	4	Modified: title, features and description Modified: <i>Figure 2</i> and <i>3</i> Updated: <i>Section 4: Package mechanical data</i> . Minor text changes
17-Sep-2018	5	Removed maturity status indication. Updated title and description on cover page. Updated <i>Table 1. Absolute maximum ratings</i> and <i>Table 6. Source-drain diode</i> . Updated <i>Section 4.1 PowerFLAT™ 5x6 type C package information</i> . Minor text changes
03-Mar-2020	6	Updated <i>Figure 5. Gate charge vs gate-source voltage</i> . Minor text changes.

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