

November 1996

FM IF Wideband Amplifier
Features

- Exceptionally High Amplifier Gain
 - Power Gain at 4.5MHz 75dB
- Excellent Input Limiting Characteristics
 - Limiting Voltage (Knee) at 10.7MHz 600 μ V (Typ)
- Wide Frequency Capability:
 - Bandwidth 100kHz to 20MHz

Applications

- FM IF Amplifiers
- FM Communication Receivers
- TV IF Amplifiers

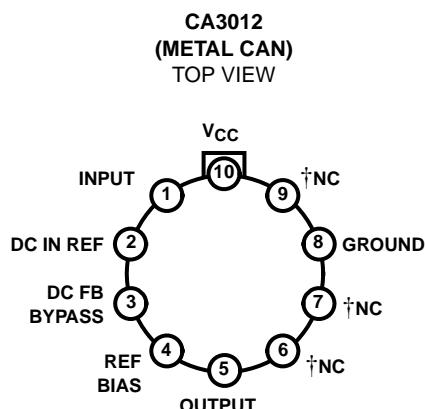
Description

The CA3012 is an FM IF wideband amplifier with 3 limiter gain stages in a bipolar monolithic technology. The pin 1 input is an open base and has a separate feedback bias. The feedback bias pin, DC FB BYPASS, is externally bypassed and provides the means for a tuned coil input to the IF IN pin. The output is a high impedance open collector which may be matched to a tuned transformer, driving an FM detector. Internal regulation circuits provide DC bias to the gain stages and DC feedback circuit.

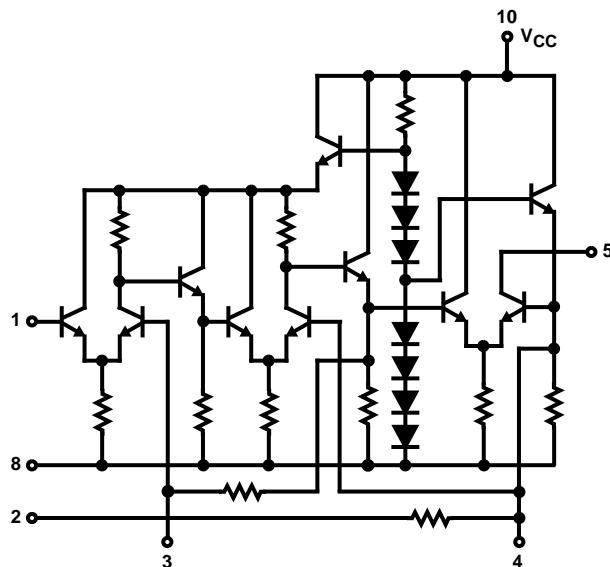
The CA3012 is intended for FM limiting applications requiring high gain.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3012	-55 to 125	10 Ld Metal Can	T10.C

Pinout


† Internal connection, do not use.

Schematic Diagram


Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Maximum Supply Voltage V_{CC} , Pin 10 10V
 Maximum Output Voltage, Pin 5 13V
 Maximum Input Signal Voltage between Pin 1 and Pin 2 $\pm 3\text{VV}$

Operating Conditions

Temperature Range -55°C to 125°C
 Supply Voltage Range (Typical) 5.5V to 10V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS				TEMP ($^\circ\text{C}$)	MIN	TYP	MAX	UNITS
		SETUP AND PROCEDURE (FIGURE)	FREQUENCY f (MHz)	DC SUPPLY VOLTAGE V_{CC} (V)						
Total Device Dissipation (Note 2)	P_T	1	-	6	-55	66	80	135	mW	
					25	66	90	121	mW	
					125	65	70	121	mW	
		-	7.5	7.5	-55	97	130	190	mW	
					25	97	120	167	mW	
					125	95	100	167	mW	
		-	10	10	-55	150	210	275	mW	
					25	150	190	255	mW	
					125	150	160	255	mW	
Voltage Gain (Note 3)	A	3	1	6	-55	50	55	-	dB	
					25	60	66	-	dB	
					125	50	61	-	dB	
		3	1	7.5	-55	55	59	-	dB	
					25	65	70	-	dB	
					125	55	65	-	dB	
		3	1	10	-55	55	61	-	dB	
					25	65	71	-	dB	
					125	55	66	-	dB	
		3	4.5	7.5	25	60	67	-	dB	
					10.7	7.5	25	55	61	-
Input Impedance Components										
Parallel Input Resistance	R_{IN}	6	4.5	7.5	25	-	3	-	$\text{k}\Omega$	
Parallel Input Capacitance	C_{IN}	6	4.5	7.5	25	-	7	-	pF	
Output Impedance Components										
Parallel Output Resistance	R_{OUT}	8	4.5	7.5	25	-	31.5	-	$\text{k}\Omega$	
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	25	-	4.2	-	pF	
Noise Figure	NF	10	4.5	7.5	25	-	8.7	-	dB	
Input Limiting Voltage (Knee)	$V_{I(LIM)}$	3	4.5	7.5	25	-	300	400	μV	

NOTES:

2. The total current drain may be determined by dividing P_T by V_{CC} .
3. Recommended minimum DC supply voltage (V_{CC}) is 5.5V. Nominal load current flowing into terminal 5 is 1.5mA at 7.5V.

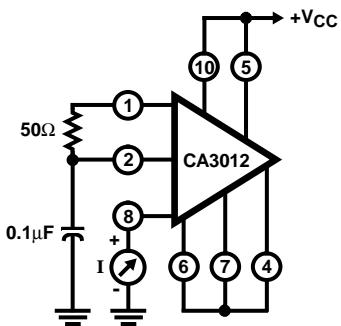
Typical Performance Curves and Test Setups

FIGURE 1. DISSIPATION TEST SETUP

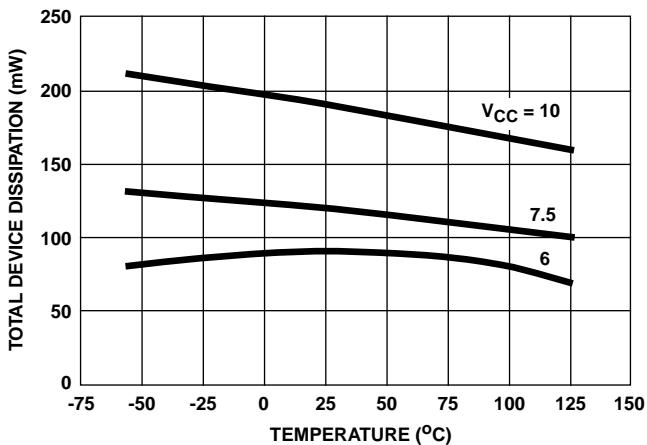


FIGURE 2. DISSIPATION vs TEMPERATURE

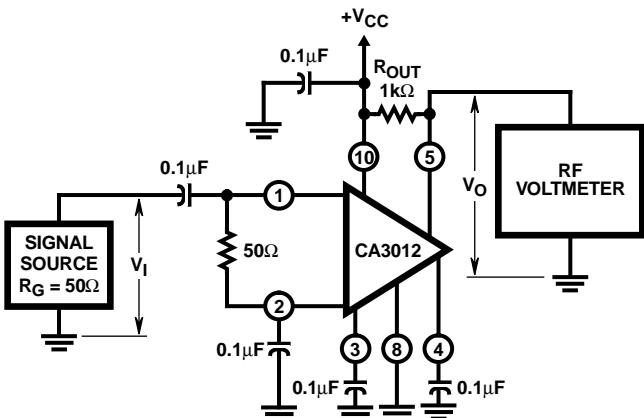


FIGURE 3. VOLTAGE GAIN TEST SETUP

Procedures**A. Voltage Gain**

1. Set input frequency at desired value, $V_I = 100\mu\text{VRMS}$
2. Record V_O
3. Calculate Voltage Gain A from $A = 20 \log_{10} V_O/V_I$
4. Repeat steps 1, 2 and 3 for each frequency and/or for temperature desired

B. Input Limiting Voltage (Knee)

1. Repeat steps A1 and A2, using $V_I = 100\text{mV}$
2. Decrease V_I to the level at which V_O is 3dB below its value for $V_I = 100\text{mV}$
3. Record V_I as Input Limiting Voltage (Knee)

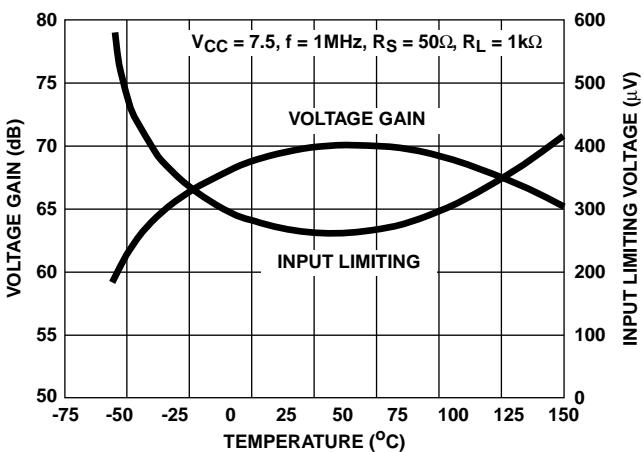


FIGURE 4. VOLTAGE GAIN AND INPUT LIMITING VOLTAGE vs TEMPERATURE

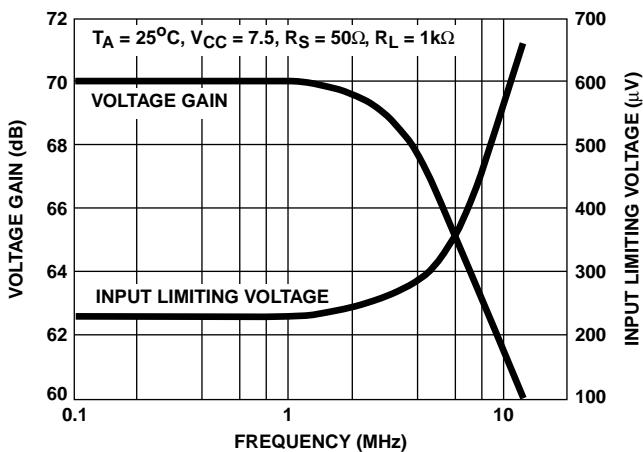


FIGURE 5. VOLTAGE GAIN AND INPUT LIMITING VOLTAGE vs FREQUENCY

Typical Performance Curves and Test Setups (Continued)

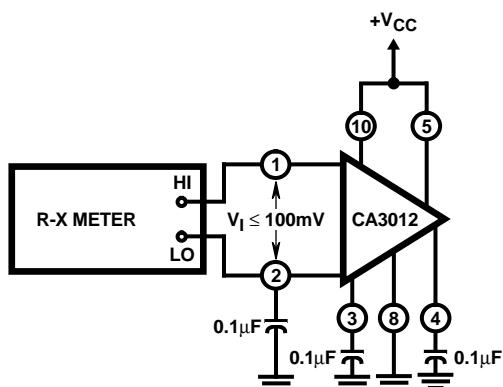


FIGURE 6. INPUT IMPEDANCE TEST SETUP

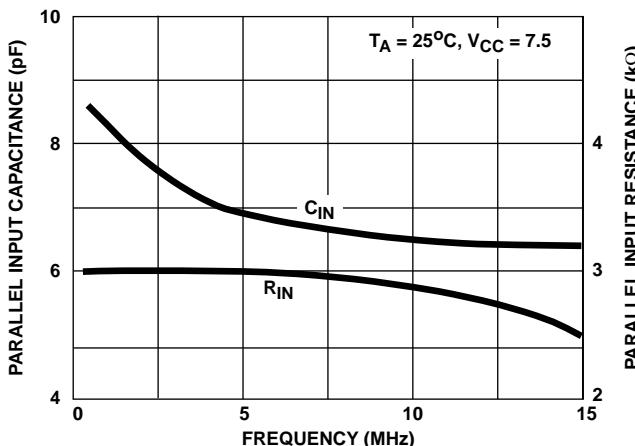


FIGURE 7. INPUT IMPEDANCE vs FREQUENCY

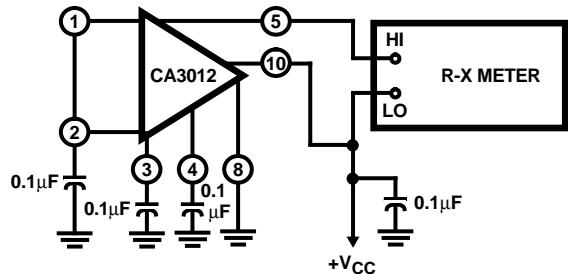


FIGURE 8. OUTPUT IMPEDANCE TEST SETUP

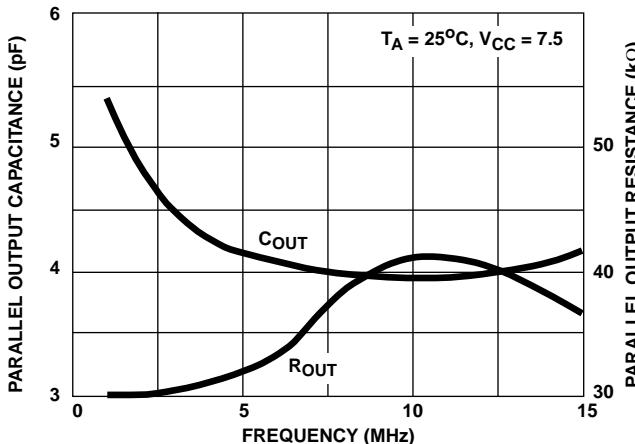


FIGURE 9. OUTPUT IMPEDANCE vs FREQUENCY

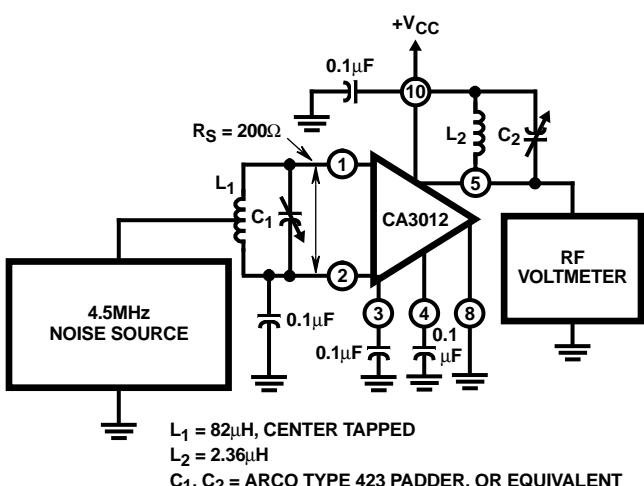


FIGURE 10.

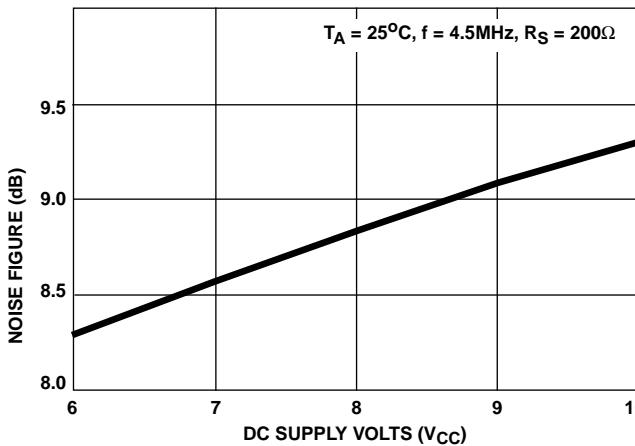


FIGURE 11. NOISE FIGURE vs DC SUPPLY VOLTAGE

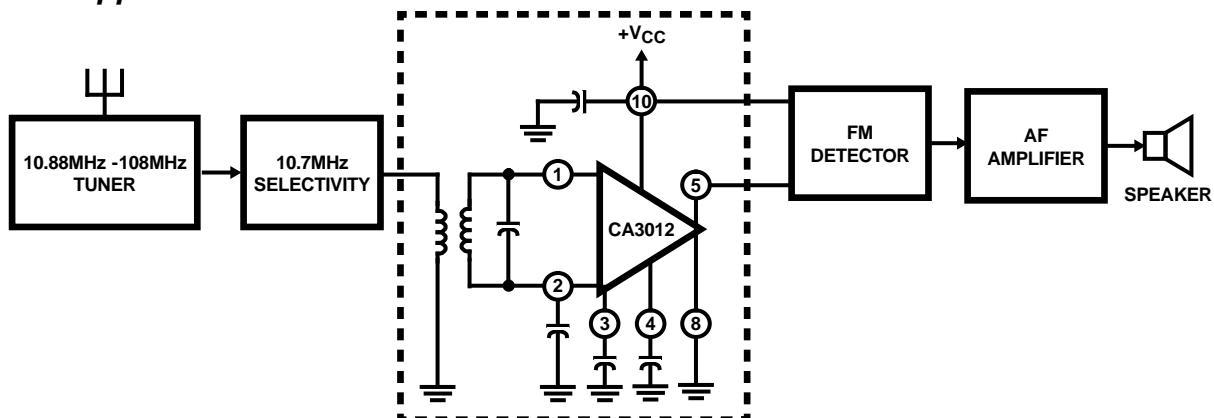
Typical Application

FIGURE 12. BLOCK DIAGRAM OF TYPICAL FM RECEIVER USING THE CA3012 INTEGRATED CIRCUIT WIDEBAND AMPLIFIER

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