

# HiRel FPGAs

## Features

- Highly Predictable Performance with 100% Automatic Placement and Routing
- Device Sizes from 1,200 to 20,000 Gates
- Up to 6 Fast, Low-Skew Clock Networks
- Up to 202 User-Programmable I/O Pins
- More Than 500 Macro Functions
- Up to 1,276 Dedicated Flip-Flops
- I/O Drive to 10 mA
- Devices Available to DSCC SMD
- CQFP and CPGA Packaging
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment
- 100% Military Temperature Tested ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ )
- QML Certified Devices
- Proven Reliability Data Available
- Successful Military/Avionics Supplier for Over 10 Years

## ACT 3 Features

- Highest-Performance, Highest-Capacity FPGA Family
- System Performance to 60 MHz over Military Temperature

- Low-Power 0.8 $\mu$  CMOS Technology

## 3200DX Features

- 100 MHz System Logic Integration
- Highest Speed FPGA SRAM, up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Low-Power 0.6 $\mu$  CMOS Technology

## 1200XL Features

- Pin for Pin Compatible with ACT 2
- System Performance to 50 MHz over Military Temperature
- Low-Power 0.6 $\mu$  CMOS Technology

## ACT 2 Features

- Best-Value, High-Capacity FPGA Family
- System Performance to 40 MHz over Military Temperature
- Low-Power 1.0 $\mu$  CMOS Technology

## ACT 1 Features

- Lowest-Cost FPGA Family
- System Performance to 20 MHz over Military Temperature
- Low-Power 1.0 $\mu$  CMOS Technology

## Product Family Profile (more devices on page 2)

| Family<br>Device               | 3200DX   |          | ACT 3  |        |         | 1200XL  |
|--------------------------------|----------|----------|--------|--------|---------|---------|
|                                | A32100DX | A32200DX | A1425A | A1460A | A14100A | A1280XL |
| <b>Capacity</b>                |          |          |        |        |         |         |
| System Gates                   | 15,000   | 30,000   | 3,750  | 9,000  | 15,000  | 12,000  |
| Logic Gates                    | 10,000   | 20,000   | 2,500  | 6,000  | 10,000  | 8,000   |
| SRAM Bits                      | 2,048    | 2,560    | NA     | NA     | NA      |         |
| <b>Logic Modules</b>           |          |          |        |        |         |         |
| S-Modules                      | 1,362    | 2,414    | 310    | 848    | 1,377   | 1,232   |
| C-Modules                      | 700      | 1,230    | 160    | 432    | 697     | 624     |
| Decode                         | 662      | 1,184    | 150    | 416    | 680     | 608     |
|                                | 20       | 24       | NA     | NA     | NA      | NA      |
| <b>Flip-Flops (Maximum)</b>    | 738      | 1,276    | 435    | 976    | 1,493   | 998     |
| <b>User I/Os (Maximum)</b>     | 152      | 202      | 100    | 168    | 228     | 140     |
| <b>Performance</b>             |          |          |        |        |         |         |
| System Speed (maximum)         | 55 MHz   | 55 MHz   | 60 MHz | 60 MHz | 60 MHz  | 50 MHz  |
| <b>Packages (by Pin Count)</b> |          |          |        |        |         |         |
| CPGA                           |          |          | 133    | 207    | 257     | 176     |
| CQFP                           | 84       | 208, 256 | 132    | 196    | 256     | 172     |

## Product Family Profile

| Family<br>Device               | ACT 2  |        | ACT 1  |        |
|--------------------------------|--------|--------|--------|--------|
|                                | A1240A | A1280A | A1010B | A1020B |
| <b>Capacity</b>                |        |        |        |        |
| System Gates                   | 6,000  | 12,000 | 1,800  | 3,000  |
| Logic Gates                    | 4,000  | 8,000  | 1,200  | 2,000  |
| SRAM Bits                      | NA     | NA     | NA     | NA     |
| <b>Logic Modules</b>           |        |        |        |        |
| S-Modules                      | 684    | 1,232  | 295    | 547    |
| C-Modules                      | 348    | 624    | —      | —      |
| Decode                         | 336    | 608    | 295    | 547    |
|                                | NA     | NA     | NA     | NA     |
| <b>Flip-Flops (maximum)</b>    | 568    | 998    | 147    | 273    |
| <b>User I/Os (maximum)</b>     | 104    | 140    | 57     | 69     |
| <b>Packages (by pin count)</b> |        |        |        |        |
| CPGA                           | 132    | 176    | 84     | 84     |
| CQFP                           | —      | 172    | —      | 84     |
| <b>Performance</b>             |        |        |        |        |
| System Speed (maximum)         | 40 MHz | 40 MHz | 20 MHz | 20 MHz |

### High-Reliability, Low-Risk Solution

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 Failures-In-Time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs have been production proven, with more than five million devices shipped and more than one trillion antifuses manufactured. Actel devices are fully tested prior to shipment, with an outgoing defect level of less than 100 ppm. (Further reliability data is available in the *Actel Device Reliability Report*, at <http://www.actel.com/hirel>).

### Benefits

#### Minimized Cost Risk

With Actel's line of development tools, designers can produce as many chips as they choose for just the cost of the device itself. There will be no NRE charges to cut into the development budget each time a new design is tried.

#### Minimized Time Risk

After the design is entered, placement and routing is automatic, and programming the device takes only about 5 to 15 minutes for an average design. Designers save time in the design entry process by using tools with which they are familiar.

#### Minimized Reliability Risk

The PLICE antifuse is a one-time programmable, nonvolatile connection. Since Actel devices are permanently programmed, no downloading from EPROM or SRAM storage is required. Inadvertent erasure is impossible, and there is no need to reload the program after power disruptions. Fabrication using a low-power CMOS process means cooler

junction temperatures. Actel's non-PLD architecture delivers lower dynamic operating current. Our reliability tests show a very low failure rate of 6.6 FITs at 90°C junction temperature with no degradation in AC performance. Special stress testing at wafer test eliminates infant mortalities prior to packaging.

#### Minimized Security Risk

Reverse engineering of programmed Actel devices from optical or electrical data is extremely difficult. Programmed antifuses cannot be identified from a photograph or by using an SEM. The antifuse map cannot be deciphered either electrically or by microprobing. Each device has a silicon signature that identifies its origins, down to the wafer lot and fabrication facility.

#### Minimized Testing Risk

Unprogrammed Actel parts are extensively tested at the factory. Routing tracks, logic modules, and programming, debug and test circuits are 100 percent tested before shipment. AC performance is ensured by special speed path tests, and programming circuitry is verified on test antifuses. During the programming process, an algorithm is run to ensure that all antifuses are correctly programmed. In addition, Actel's Silicon Explorer diagnostic tool uses ActionProbe circuitry, allowing 100 percent observability of all internal nodes to check and debug the design.

### Actel FPGA Description

The Actel families of FPGAs offer a variety of packages, speed/performance characteristics, and processing levels for use in all high reliability and military applications. Devices are implemented in a silicon gate, two-level metal CMOS process, utilizing Actel's PLICE antifuse technology. This

unique architecture offers gate array flexibility, high performance, and quick turnaround through user programming. Device utilization is typically 95 percent of available logic modules. All Actel devices include on-chip clock drivers and a hard-wired distribution network.

User-definable I/Os are capable of driving at both TTL and CMOS drive levels. Available packages for the military are the Ceramic Quad Flat Pack (CQFP) and the Ceramic Pin Grid Array (CPGA). See the “[Product Plan](#)” section on page 6 for details.

### QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for a quality, reliable and cost-effective logistics support throughout QML products' life cycles.

### Development Tool Support

The HiRel devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP Series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer with DirectTime timing driven place and route and analysis tools, and device programming software.

In addition, the HiRel devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

### ACT 3 Description

The ACT 3 family is the third-generation Actel FPGA family. This family offers the highest-performance and highest-capacity devices, ranging from 2,500 to 10,000 gates, with system performance up to 60 MHz over the military temperature range. The devices have four clock distribution networks, including dedicated array and I/O clocks. In addition, the ACT 3 family offers the highest I/O-to-gate ratio available. ACT 3 devices are manufactured using 0.8 $\mu$  CMOS technology.

### 1200XL/3200DX Description

3200DX and 1200XL FPGAs were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs, and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers the industry's fastest dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage.

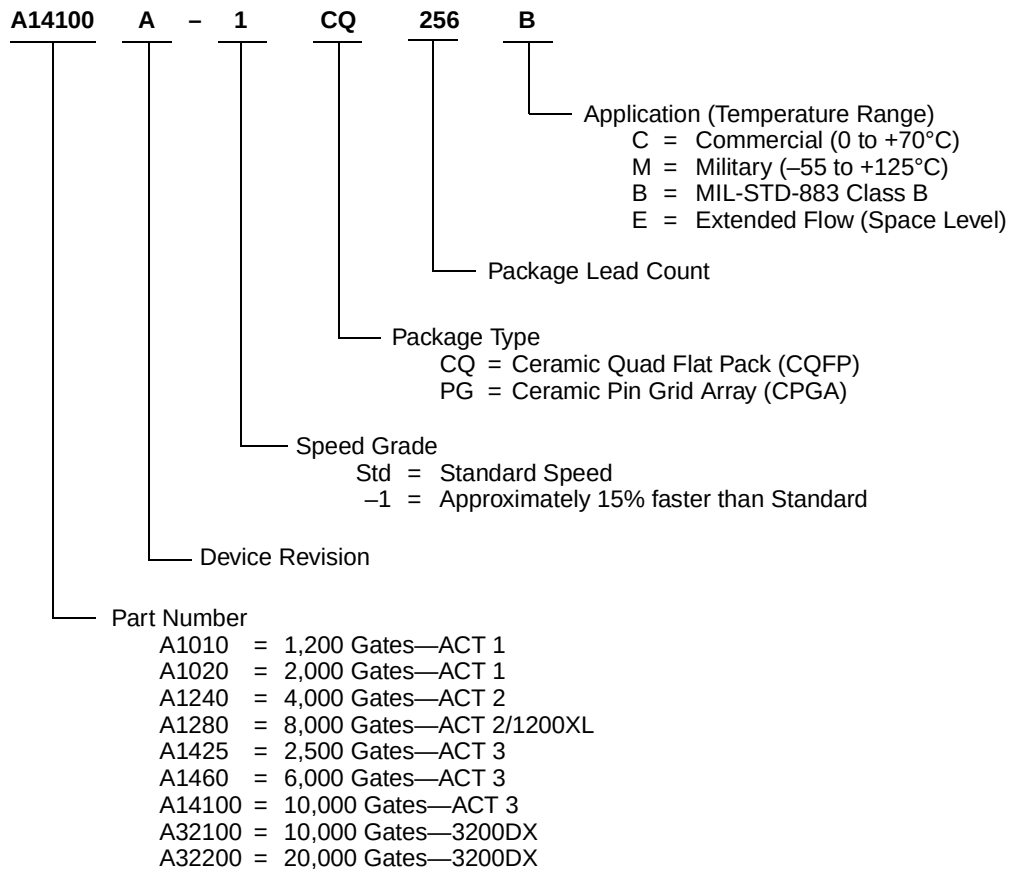
### ACT 2 Description

The ACT 2 family is the second-generation Actel FPGA family. This family offers the best-value, high-capacity devices, ranging from 4,000 to 8,000 gates, with system performance up to 40 MHz over the military temperature range. The devices have two routed array clock distribution networks. ACT 2 devices are manufactured using 1.0 $\mu$  CMOS technology.

### ACT 1 Description

The ACT 1 family is the first Actel FPGA family and the first antifuse-based FPGA. This family offers the lowest-cost logic integration, with devices ranging from 1,200 to 2,000 gates, with system performance up to 20 MHz over the military temperature range. The devices have one routed array clock distribution network. ACT 1 devices are manufactured using 1.0 $\mu$  CMOS technology.

## Military Device Ordering Information



**DESC SMD/Actel Part Number Cross Reference**

| <b>Actel Part Number<br/>(Gold Leads)</b> | <b>DSCC SMD<br/>(Gold Leads)</b> | <b>DSCC SMD<br/>(Solder Dipped)</b> |
|-------------------------------------------|----------------------------------|-------------------------------------|
| A1010B-PG84B                              | 5962-9096403MXC                  | 5962-9096403MXA                     |
| A1010B-1PG84B                             | 5962-9096404MXC                  | 5962-9096404MXA                     |
| A1020B-PG84B                              | 5962-9096503MUC                  | 5962-9096503MUA                     |
| A1020B-1PG84B                             | 5962-9096504MUC                  | 5962-9096504MUA                     |
| A1020B-CQ84B                              | 5962-9096503MTC                  | 5962-9096503MTA                     |
| A1020B-1CQ84B                             | 5962-9096504MTC                  | 5962-9096504MTA                     |
| A1240A-PG132B                             | 5962-9322101MXC                  | 5962-9322101MXA                     |
| A1240A-1PG132B                            | 5962-9322102MXC                  | 5962-9322102MXA                     |
| A1280A-PG176B                             | 5962-9215601MXC                  | 5962-9215601MXA                     |
| A1280A-1PG176B                            | 5962-9215602MXC                  | 5962-9215602MXA                     |
| A1280A-CQ172B                             | 5962-9215601MYC                  | 5962-9215601MYA                     |
| A1280A-1CQ172B                            | 5962-9215602MYC                  | 5962-9215602MYA                     |
| A1425A-PG133B                             | 5962-9552001MXC                  | N/A                                 |
| A1425A-1PG133B                            | 5962-9552002MXC                  | N/A                                 |
| A1425A-CQ132B                             | 5962-9552001MYC                  | N/A                                 |
| A1425A-1CQ132B                            | 5962-9552002MYC                  | N/A                                 |
| A1460A-PG207B                             | 5962-9550801MXC                  | N/A                                 |
| A1460A-1PG207B                            | 5962-9550802MXC                  | N/A                                 |
| A1460A-CQ196B                             | 5962-9550801MYC                  | N/A                                 |
| A1460A-1CQ196B                            | 5962-9550802MYC                  | N/A                                 |
| A14100A-PG257B                            | 5962-9552101MXC                  | N/A                                 |
| A14100A-1PG257B                           | 5962-9552102MXC                  | N/A                                 |
| A14100A-CQ256B                            | 5962-9552101MYC                  | N/A                                 |
| A14100A-1CQ256B                           | 5962-9552102MYC                  | N/A                                 |
| A32100DX-CQ84B                            | 5962-9875901QXC                  | N/A                                 |
| A32100DX-1CQ84B                           | 5962-9857902QXC                  | N/A                                 |
| A32200DX-CQ256B                           | 5962-9952701QXC                  | N/A                                 |
| A32200DX-1CQ256B                          | 5962-9952702QXC                  | N/A                                 |
| A32200DX-CQ208B                           | 5962-9952701QYC                  | N/A                                 |
| A32200DX-1CQ208B                          | 5962-9952702QYC                  | N/A                                 |

## Product Plan

| 3200DX Family                         | Speed Grade |     | Application |   |   |   |
|---------------------------------------|-------------|-----|-------------|---|---|---|
|                                       | Std         | −1* | C           | M | B | E |
| A32100DX Device                       |             |     |             |   |   |   |
| 84-pin Ceramic Quad Flat Pack (CQFP)  | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| A32200DX Device                       |             |     |             |   |   |   |
| 208-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| 256-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| ACT 3 Family                          |             |     |             |   |   |   |
| A1425A Device                         |             |     |             |   |   |   |
| 132-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| 133-pin Ceramic Pin Grid Array (CPGA) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| A1460A Device                         |             |     |             |   |   |   |
| 196-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| 207-pin Ceramic Pin Grid Array (CPGA) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| A14100A Device                        |             |     |             |   |   |   |
| 256-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| 257-pin Ceramic Pin Grid Array (CPGA) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| 1200XL Family                         |             |     |             |   |   |   |
| A1280XL Device                        |             |     |             |   |   |   |
| 172-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| 176-pin Ceramic Pin Grid Array (CPGA) | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| ACT 2 Family                          |             |     |             |   |   |   |
| A1240A Device                         |             |     |             |   |   |   |
| 132-pin Ceramic Pin Grid Array (CPGA) | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| A1280A Device                         |             |     |             |   |   |   |
| 172-pin Ceramic Quad Flat Pack (CQFP) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| 176-pin Ceramic Pin Grid Array (CPGA) | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| ACT 1 Family                          |             |     |             |   |   |   |
| A1010B Device                         |             |     |             |   |   |   |
| 84-pin Ceramic Pin Grid Array (CPGA)  | ✓           | ✓   | ✓           | ✓ | ✓ | — |
| A1020B Device                         |             |     |             |   |   |   |
| 84-pin Ceramic Quad Flat Pack (CQFP)  | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |
| 84-pin Ceramic Pin Grid Array (CPGA)  | ✓           | ✓   | ✓           | ✓ | ✓ | ✓ |

*Applications:* *C* = Commercial      *Availability:* ✓ = Available      \**Speed Grade:* -1 = Approx. 15% faster than Standard  
*M* = Military                                      — = Not Planned  
*B* = MIL-STD-883  
*E* = Extended Flow

**3200DX Device Resources**

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os |         |         |
|------------------|---------------|-----------------------------|-----------|---------|---------|
|                  |               |                             | CQFP      |         |         |
|                  |               |                             | 84-pin    | 208-pin | 256-pin |
| A32100DX         | 1,362         | 10,000                      | 60        | —       | —       |
| A32200DX         | 2,414         | 20,000                      | —         | 176     | 202     |

**ACT 3 Device Resources**

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os |         |         |         |         |         |
|------------------|---------------|-----------------------------|-----------|---------|---------|---------|---------|---------|
|                  |               |                             | CQFP      |         |         | CPGA    |         |         |
|                  |               |                             | 132-pin   | 196-pin | 256-pin | 133-pin | 207-pin | 257-pin |
| A1425A           | 310           | 2,500                       | 100       | —       | —       | 100     | —       | —       |
| A1460A           | 848           | 6,000                       | —         | 168     | —       | —       | 168     | —       |
| A14100A          | 1,377         | 10,000                      | —         | —       | 228     | —       | —       | 228     |

**1200XL Device Resources**

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os       |                 |
|------------------|---------------|-----------------------------|-----------------|-----------------|
|                  |               |                             | CQFP<br>172-pin | CPGA<br>176-pin |
| A1280XL          | 1,232         | 8,000                       | 140             | 140             |

**ACT 2 Device Resources**

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os       |                         |
|------------------|---------------|-----------------------------|-----------------|-------------------------|
|                  |               |                             | CQFP<br>172-pin | CPGA<br>132-pin 176-pin |
| A1240A           | 684           | 4,000                       | —               | 104 —                   |
| A1280A           | 1,232         | 8,000                       | 140             | — 140                   |

**ACT 1 Device Resources**

| FPGA Device Type | Logic Modules | Gate Array Equivalent Gates | User I/Os      |                |
|------------------|---------------|-----------------------------|----------------|----------------|
|                  |               |                             | CQFP<br>84-pin | CPGA<br>84-pin |
| A1010B           | 295           | 1,200                       | —              | 57             |
| A1020B           | 547           | 2,000                       | 69             | 69             |

## Actel MIL-STD-883 Product Flow

| Step | Screen                                              | 883 Method                                                                            | 883—Class B Requirement |
|------|-----------------------------------------------------|---------------------------------------------------------------------------------------|-------------------------|
| 1.   | Internal Visual                                     | 2010, Test Condition B                                                                | 100%                    |
| 2.   | Temperature Cycling                                 | 1010, Test Condition C                                                                | 100%                    |
| 3.   | Constant Acceleration                               | 2001, Test Condition D or E, Y <sub>1</sub> , Orientation Only                        | 100%                    |
| 4.   | Seal                                                | 1014                                                                                  |                         |
|      | a. Fine                                             |                                                                                       | 100%                    |
|      | b. Gross                                            |                                                                                       | 100%                    |
| 5.   | Visual Inspection                                   | 2009                                                                                  | 100%                    |
| 6.   | Pre-Burn-In Electrical Parameters                   | In accordance with applicable Actel device specification                              | 100%                    |
| 7.   | Burn-in Test                                        | 1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C                              | 100%                    |
| 8.   | Interim (Post-Burn-In) Electrical Parameters        | In accordance with applicable Actel device specification                              | 100%                    |
| 9.   | Percent Defective Allowable                         | 5%                                                                                    | All Lots                |
| 10.  | Final Electrical Test                               | In accordance with applicable Actel device specification, which includes a, b, and c: |                         |
|      | a. Static Tests                                     |                                                                                       | 100%                    |
|      | (1) 25°C (Subgroup 1, Table I)                      | 5005                                                                                  |                         |
|      | (2) –55°C and +125°C (Subgroups 2, 3, Table I)      | 5005                                                                                  |                         |
|      | b. Functional Tests                                 |                                                                                       | 100%                    |
|      | (1) 25°C (Subgroup 7, Table I)                      | 5005                                                                                  |                         |
|      | (2) –55°C and +125°C (Subgroups 8A and 8B, Table I) | 5005                                                                                  |                         |
|      | c. Switching Tests at 25°C (Subgroup 9, Table I)    | 5005                                                                                  | 100%                    |
| 11.  | External Visual                                     | 2009                                                                                  | 100%                    |

**Note:** When Destructive Physical Analysis (DPA) is performed on Class B devices, the step coverage requirement as specified in Method 2018 must be waived.

**Actel Extended Flow<sup>1</sup>**

| Step | Screen                                                | Method                                                                               | Requirement |
|------|-------------------------------------------------------|--------------------------------------------------------------------------------------|-------------|
| 1.   | Wafer Lot Acceptance <sup>2</sup>                     | 5007 with Step Coverage Waiver                                                       | All Lots    |
| 2.   | Destructive In-Line Bond Pull <sup>3</sup>            | 2011, Condition D                                                                    | Sample      |
| 3.   | Internal Visual                                       | 2010, Condition A                                                                    | 100%        |
| 4.   | Serialization                                         |                                                                                      | 100%        |
| 5.   | Temperature Cycling                                   | 1010, Condition C                                                                    | 100%        |
| 6.   | Constant Acceleration                                 | 2001, Condition D or E, Y <sub>1</sub> Orientation Only                              | 100%        |
| 7.   | Particle Impact Noise Detection                       | 2020, Condition A                                                                    | 100%        |
| 8.   | Radiographic                                          | 2012 (one view only)                                                                 | 100%        |
| 9.   | Pre-Burn-In Test                                      | In accordance with applicable Actel device specification                             | 100%        |
| 10.  | Burn-in Test                                          | 1015, Condition D, 240 hours @ 125°C minimum                                         | 100%        |
| 11.  | Interim (Post-Burn-In) Electrical Parameters          | In accordance with applicable Actel device specification                             | 100%        |
| 12.  | Reverse Bias Burn-In                                  | 1015, Condition C, 72 hours @ 150°C minimum                                          | 100%        |
| 13.  | Interim (Post-Burn-In) Electrical Parameters          | In accordance with applicable Actel device specification                             | 100%        |
| 14.  | Percent Defective Allowable (PDA) Calculation         | 5%, 3% Functional Parameters @ 25°C                                                  | All Lots    |
| 15.  | Final Electrical Test                                 | In accordance with Actel applicable device specification which includes a, b, and c: | 100%        |
|      | a. Static Tests                                       |                                                                                      | 100%        |
|      | (1) 25°C<br>(Subgroup 1, Table 1)                     | 5005                                                                                 |             |
|      | (2) -55°C and +125°C<br>(Subgroups 2, 3, Table 1)     | 5005                                                                                 |             |
|      | b. Functional Tests                                   |                                                                                      | 100%        |
|      | (1) 25°C<br>(Subgroup 7, Table 15)                    | 5005                                                                                 |             |
|      | (2) -55°C and +125°C<br>(Subgroups 8A and B, Table 1) | 5005                                                                                 |             |
|      | c. Switching Tests at 25°C<br>(Subgroup 9, Table 1)   | 5005                                                                                 | 100%        |
| 16.  | Seal                                                  | 1014                                                                                 | 100%        |
|      | a. Fine                                               |                                                                                      |             |
|      | b. Gross                                              |                                                                                      |             |
| 17.  | External Visual                                       | 2009                                                                                 | 100%        |

**Notes:**

1. Actel offers the extended flow for customers who require additional screening beyond the requirements of the MIL-STD-883, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 3 below.
2. Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be waived.
3. MIL-STD-883, Method 5004 requires 100 percent Radiation latch-up testing (Method 1020). Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.

## Absolute Maximum Ratings<sup>1</sup>

Free air temperature range

| Symbol           | Parameter                            | Limits                        | Units |
|------------------|--------------------------------------|-------------------------------|-------|
| V <sub>CC</sub>  | DC Supply Voltage <sup>2, 3, 4</sup> | −0.5 to +7.0                  | V     |
| V <sub>I</sub>   | Input Voltage                        | −0.5 to V <sub>CC</sub> + 0.5 | V     |
| V <sub>O</sub>   | Output Voltage                       | −0.5 to V <sub>CC</sub> + 0.5 | V     |
| I <sub>IO</sub>  | I/O Source Sink Current <sup>5</sup> | ±20                           | mA    |
| T <sub>STG</sub> | Storage Temperature                  | −65 to +150                   | °C    |

### Notes:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.
2. V<sub>PP</sub> = V<sub>CC</sub>, except during device programming.
3. V<sub>SV</sub> = V<sub>CC</sub>, except during device programming.
4. V<sub>KS</sub> = GND, except during device programming.
5. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V<sub>CC</sub> + 0.5V or less than GND − 0.5V, the internal protection diode will be forward biased and can draw excessive current.

## Recommended Operating Conditions

| Parameter                           | Commercial | Military    | Units            |
|-------------------------------------|------------|-------------|------------------|
| Temperature Range <sup>1</sup>      | 0 to +70   | −55 to +125 | °C               |
| Power Supply Tolerance <sup>2</sup> | ±5         | ±10         | %V <sub>CC</sub> |

### Notes:

1. Ambient temperature (T<sub>A</sub>) is used for commercial and industrial; case temperature (T<sub>C</sub>) is used for military.
2. All power supplies must be in the recommended operating range. For more information, refer to the Power-Up Design Considerations application note at <http://www.actel.com/appnotes>.

## Electrical Specifications

| Symbol                          | Parameter                              | Test Condition                                                 | Commercial |                       | Military |                       | Units |
|---------------------------------|----------------------------------------|----------------------------------------------------------------|------------|-----------------------|----------|-----------------------|-------|
|                                 |                                        |                                                                | Min.       | Max.                  | Min.     | Max.                  |       |
| V <sub>OH</sub> <sup>1, 2</sup> | HIGH Level Output                      | I <sub>OH</sub> = −4 mA (CMOS)                                 |            |                       | 3.7      |                       | V     |
|                                 |                                        | I <sub>OH</sub> = −6 mA (CMOS)                                 | 3.84       |                       |          |                       | V     |
| V <sub>OL</sub> <sup>1, 2</sup> | LOW Level Output                       | I <sub>OL</sub> = +6 mA (CMOS)                                 |            | 0.33                  |          | 0.4                   | V     |
| V <sub>IH</sub>                 | HIGH Level Input                       | TTL Inputs                                                     | 2.0        | V <sub>CC</sub> + 0.3 | 2.0      | V <sub>CC</sub> + 0.3 | V     |
| V <sub>IL</sub>                 | LOW Level Input                        | TTL Inputs                                                     | −0.3       | 0.8                   | −0.3     | 0.8                   | V     |
| I <sub>IN</sub>                 | Input Leakage                          | V <sub>I</sub> = V <sub>CC</sub> or GND                        | −10        | +10                   | −10      | +10                   | μA    |
| I <sub>OZ</sub>                 | 3-state Output Leakage                 | V <sub>O</sub> = V <sub>CC</sub> or GND                        | −10        | +10                   | −10      | +10                   | μA    |
| C <sub>IO</sub>                 | I/O Capacitance <sup>3, 4</sup>        |                                                                |            | 10                    |          | 10                    | pF    |
| I <sub>CC(S)</sub>              | Standby V <sub>CC</sub> Supply Current | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 mA |            |                       |          |                       |       |
|                                 |                                        | ACT 1                                                          |            | 3                     |          | 20                    | mA    |
|                                 |                                        | ACT 2/3/1200XL/3200DX                                          |            | 2                     |          | 20                    | mA    |
| I <sub>CC(D)</sub>              | Dynamic V <sub>CC</sub> Supply Current | See the “Power Dissipation” section on page 11.                |            |                       |          |                       |       |

### Notes:

1. Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.
2. Tested one output at a time, V<sub>CC</sub> = min.
3. Not tested; for information only.
4. V<sub>OUT</sub> = 0V, f = 1 MHz

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 176-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 125^\circ\text{C}}{23^\circ\text{C/W}} = 1.1 \text{ W}$$

| Package Type           | Pin Count | $\theta_{jc}$ | $\theta_{ja}$<br>Still Air | $\theta_{ja}$<br>300 ft/min | Units |
|------------------------|-----------|---------------|----------------------------|-----------------------------|-------|
| Ceramic Pin Grid Array | 84        | 6.0           | 33                         | 20                          | °C/W  |
|                        | 132       | 4.8           | 25                         | 16                          | °C/W  |
|                        | 133       | 4.8           | 25                         | 15                          | °C/W  |
|                        | 176       | 4.6           | 23                         | 12                          | °C/W  |
|                        | 207       | 3.5           | 21                         | 10                          | °C/W  |
|                        | 257       | 2.8           | 15                         | 8                           | °C/W  |
| Ceramic Quad Flat Pack | 84        | 7.8           | 40                         | 30                          | °C/W  |
|                        | 132       | 7.2           | 35                         | 25                          | °C/W  |
|                        | 172       | 6.8           | 25                         | 20                          | °C/W  |
|                        | 196       | 6.4           | 23                         | 15                          | °C/W  |
|                        | 256       | 6.2           | 20                         | 10                          | °C/W  |

## Power Dissipation

### General Power Equation

$$P = [I_{CC\text{standby}} + I_{CC\text{active}}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

$I_{CC\text{standby}}$  is the current flowing when no inputs or outputs are changing.

$I_{CC\text{active}}$  is the current flowing due to CMOS switching.

$I_{OL}$ ,  $I_{OH}$  are TTL sink/source currents.

$V_{OL}$ ,  $V_{OH}$  are TTL level output voltages.

$N$  equals the number of outputs driving TTL loads to  $V_{OL}$ .

$M$  equals the number of outputs driving TTL loads to  $V_{OH}$ .

Accurate values for  $N$  and  $M$  are difficult to determine because they depend on the family type, on the design, and on the system I/O. The power can be divided into two components—static and active.

### Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than that of PALs or PLDs. By integrating multiple PALs or PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

| Family        | $I_{CC}$ | $V_{CC}$ | Power   |
|---------------|----------|----------|---------|
| ACT 3         | 2 mA     | 5.25V    | 10.5 mW |
| 1200XL/3200DX | 2 mA     | 5.25V    | 10.5 mW |
| ACT 2         | 2 mA     | 5.25V    | 10.5 mW |
| ACT 1         | 3 mA     | 5.25V    | 15.8 mW |

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high.

### Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that

can be combined with frequency and voltage to represent active power dissipation.

### Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1:

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

$C_{EQ}$  = Equivalent capacitance in pF

$V_{CC}$  = Power supply in volts (V)

$F$  = Switching frequency in MHz

Equivalent capacitance is calculated by measuring  $I_{CC}$  active at a specified frequency and voltage for each circuit component of interest. Measurements are made over a range of frequencies at a fixed value of  $V_{CC}$ . Equivalent capacitance is frequency independent so that the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

### CEQ Values for Actel FPGAs

|                                                | 1200XL |        |       |       |
|------------------------------------------------|--------|--------|-------|-------|
|                                                | ACT 3  | 3200DX | ACT 2 | ACT 1 |
| Modules ( $C_{EQM}$ )                          | 6.7    | 5.2    | 5.8   | 3.7   |
| Input Buffers ( $C_{EQI}$ )                    | 7.2    | 11.6   | 12.9  | 22.1  |
| Output Buffers ( $C_{EQO}$ )                   | 10.4   | 23.8   | 23.8  | 31.2  |
| Routed Array Clock Buffer Loads ( $C_{EQCR}$ ) | 1.6    | 3.5    | 3.9   | 4.6   |
| Dedicated Clock Buffer Loads ( $C_{EQCD}$ )    | 0.7    | N/A    | N/A   | N/A   |
| I/O Clock Buffer Loads ( $C_{EQCI}$ )          | 0.9    | N/A    | N/A   | N/A   |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piecewise linear summation over all components that applies to all ACT 1, 1200XL, 3200DX, ACT 2, and ACT 3 devices. Since the ACT 1 family has only one routed array clock, the terms labeled routed\_Clk2, dedicated\_Clk, and IO\_Clk do not apply. Similarly, the ACT 2 family has two routed array clocks, and the dedicated\_Clk and IO\_Clk terms do not apply. For ACT 3 devices, all terms will apply.

$$\begin{aligned} \text{Power} = & V_{CC}^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} + \\ & (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{\text{routed\_Clk1}} + \\ & (r_1 * f_{q1})_{\text{routed\_Clk1}} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{\text{routed\_Clk2}} + \\ & (r_2 * f_{q2})_{\text{routed\_Clk2}} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{\text{dedicated\_Clk}} + \\ & (s_2 * C_{EQCI} * f_{s2})_{\text{IO\_Clk}}] \end{aligned} \quad (2)$$

where:

|            |   |                                                                                            |
|------------|---|--------------------------------------------------------------------------------------------|
| $m$        | = | Number of logic modules switching at $f_m$                                                 |
| $n$        | = | Number of input buffers switching at $f_n$                                                 |
| $p$        | = | Number of output buffers switching at $f_p$                                                |
| $q_1$      | = | Number of clock loads on the first routed array clock (all families)                       |
| $q_2$      | = | Number of clock loads on the second routed array clock (ACT 2, 1200XL, 3200DX, ACT 3 only) |
| $r_1$      | = | Fixed capacitance due to first routed array clock (all families)                           |
| $r_2$      | = | Fixed capacitance due to second routed array clock (ACT 2, 1200XL, 3200DX, ACT 3 only)     |
| $s_1$      | = | Fixed number of clock loads on the dedicated array clock (ACT 3 only)                      |
| $s_2$      | = | Fixed number of clock loads on the dedicated I/O clock (ACT 3 only)                        |
| $C_{EQM}$  | = | Equivalent capacitance of logic modules in pF                                              |
| $C_{EQI}$  | = | Equivalent capacitance of input buffers in pF                                              |
| $C_{EQO}$  | = | Equivalent capacitance of output buffers in pF                                             |
| $C_{EQCR}$ | = | Equivalent capacitance of routed array clock in pF                                         |
| $C_{EQCD}$ | = | Equivalent capacitance of dedicated array clock in pF                                      |
| $C_{EQCI}$ | = | Equivalent capacitance of dedicated I/O clock in pF                                        |
| $C_L$      | = | Output lead capacitance in pF                                                              |
| $f_m$      | = | Average logic module switching rate in MHz                                                 |
| $f_n$      | = | Average input buffer switching rate in MHz                                                 |
| $f_p$      | = | Average output buffer switching rate in MHz                                                |
| $f_{q1}$   | = | Average first routed array clock rate in MHz (all families)                                |
| $f_{q2}$   | = | Average second routed array clock rate in MHz (ACT 2, 1200XL, 3200DX, ACT 3 only)          |
| $f_{s1}$   | = | Average dedicated array clock rate in MHz (ACT 3 only)                                     |
| $f_{s2}$   | = | Average dedicated I/O clock rate in MHz (ACT 3 only)                                       |

**Fixed Capacitance Values for Actel FPGAs (pF)**

| Device Type | $r_1$<br>routed_Clk1 | $r_2$<br>routed_Clk2 |
|-------------|----------------------|----------------------|
| A1010B      | 41                   | n/a                  |
| A1020B      | 69                   | n/a                  |
| A1240A      | 134                  | 134                  |
| A1280A      | 168                  | 168                  |
| A1280XL     | 168                  | 168                  |
| A1425A      | 75                   | 75                   |
| A1460A      | 165                  | 165                  |
| A14100A     | 195                  | 195                  |
| A32100DX    | 178                  | 178                  |
| A32200DX    | 230                  | 230                  |

**Fixed Clock Loads ( $s_1/s_2$ —ACT 3 Only)**

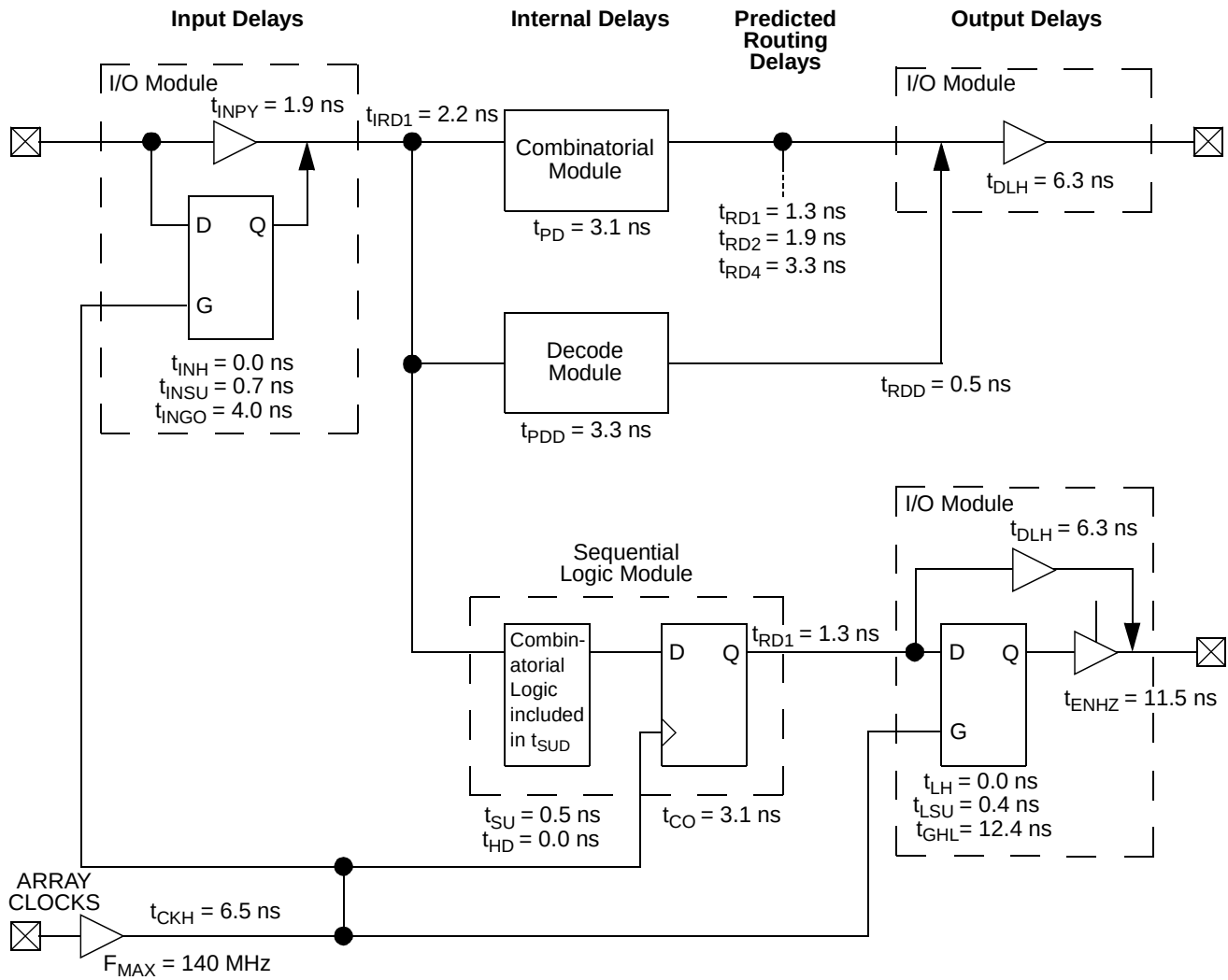
| Device Type | $s_1$<br>Clock Loads on<br>Dedicated<br>Array Clock | $s_2$<br>Clock Loads on<br>Dedicated<br>I/O Clock |
|-------------|-----------------------------------------------------|---------------------------------------------------|
| A1425A      | 160                                                 | 100                                               |
| A1460A      | 432                                                 | 168                                               |
| A14100A     | 697                                                 | 228                                               |

**Determining Average Switching Frequency**

To determine the switching frequency for a design, you must have a detailed understanding of the data values input to the circuit. The guidelines in the table below are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation.

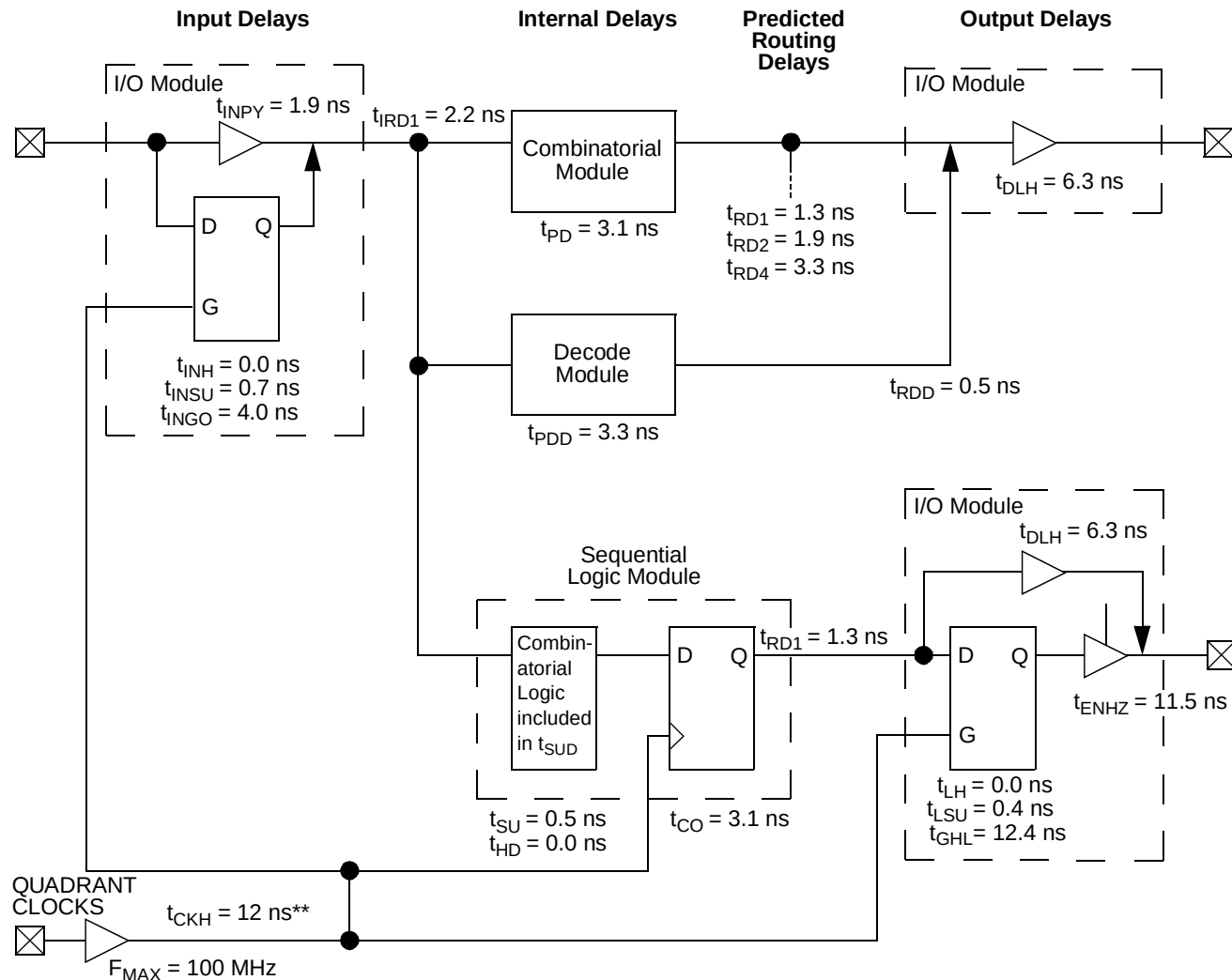
| Type                                                | ACT 3                     | 3200DX/ACT 2/1200XL       | ACT 1          |
|-----------------------------------------------------|---------------------------|---------------------------|----------------|
| Logic modules (m)                                   | 80% of modules            | 80% of modules            | 90% of modules |
| Input switching (n)                                 | # inputs/4                | # inputs/4                | # inputs/4     |
| Outputs switching (p)                               | #outputs/4                | #outputs/4                | #outputs/4     |
| First routed array clock loads ( $q_1$ )            | 40% of sequential modules | 40% of sequential modules | 40% of modules |
| Second routed array clock loads ( $q_2$ )           | 40% of sequential modules | 40% of sequential modules | n/a            |
| Load capacitance ( $C_L$ )                          | 35 pF                     | 35 pF                     | 35 pF          |
| Average logic module switching rate ( $f_m$ )       | F/10                      | F/10                      | F/10           |
| Average input switching rate ( $f_n$ )              | F/5                       | F/5                       | F/5            |
| Average output switching rate ( $f_p$ )             | F/10                      | F/10                      | F/10           |
| Average first routed array clock rate ( $f_{q1}$ )  | F/2                       | F                         | F              |
| Average second routed array clock rate ( $f_{q2}$ ) | F/2                       | F/2                       | n/a            |
| Average dedicated array clock rate ( $f_{s1}$ )     | F                         | n/a                       | n/a            |
| Average dedicated I/O clock rate ( $f_{s2}$ )       | F                         | n/a                       | n/a            |

## 3200DX Timing Model (Logic Functions using Array Clocks)\*



\*Values shown for A32100DX-1 at worst-case military conditions.

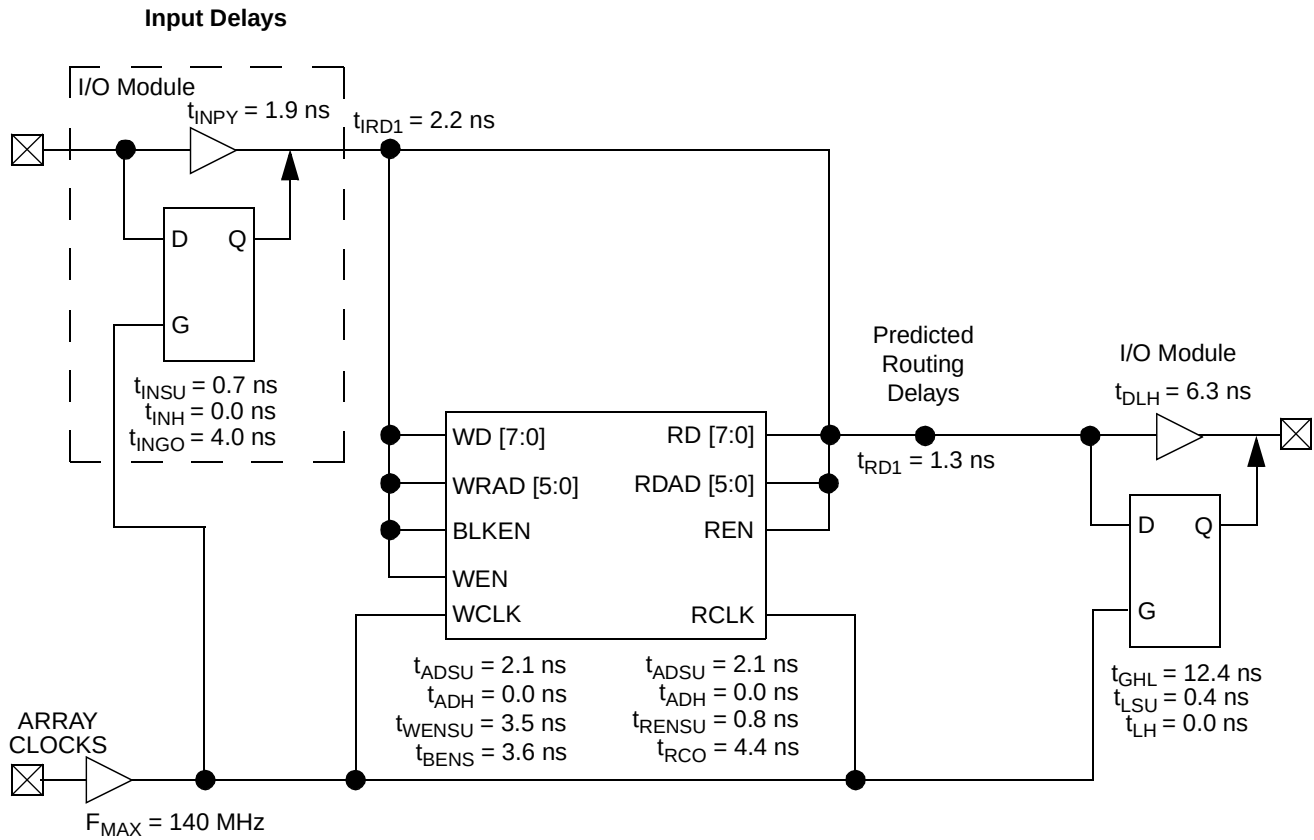
### 3200DX Timing Model (Logic Functions using Quadrant Clocks)\*



\* Values shown for A32100DX-1 at worst-case military conditions.

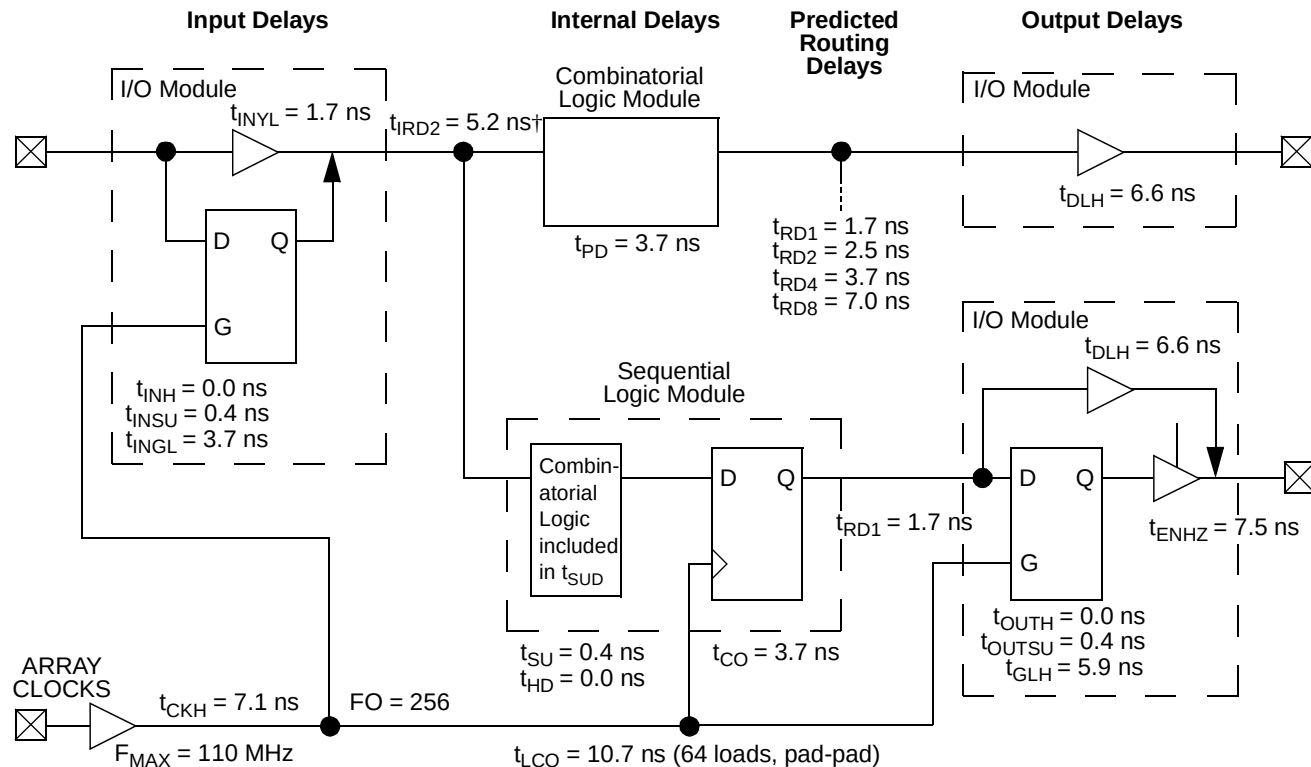
\*\* Load dependent.

## 3200DX Timing Model (SRAM Functions)\*



\*Values shown for A32100DX-1 at worst-case military conditions.

## 1200XL Timing Model\*

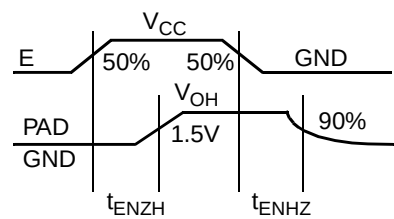
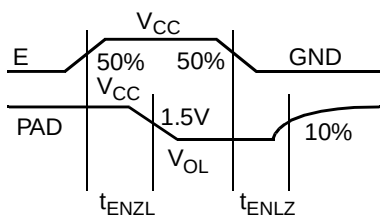
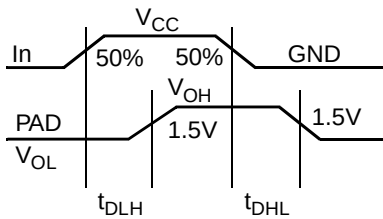
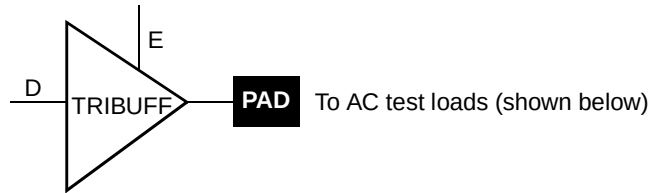


\*Values shown for A1280XL-1 at worst-case military conditions.

† Input module predicted routing delay.

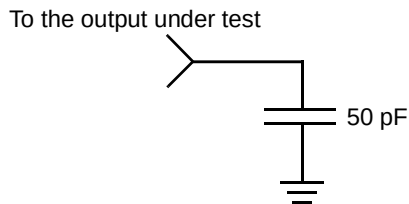
## Parameter Measurement

### Output Buffer Delays

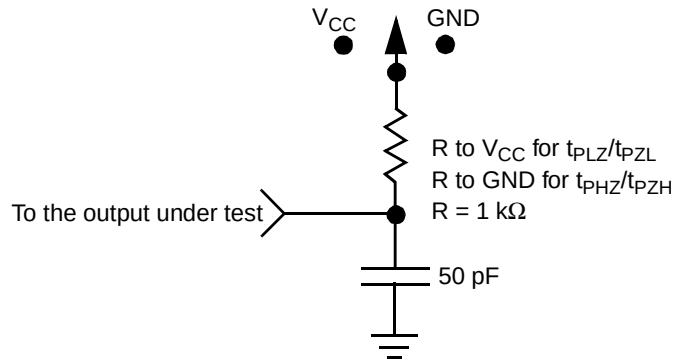


### AC Test Load

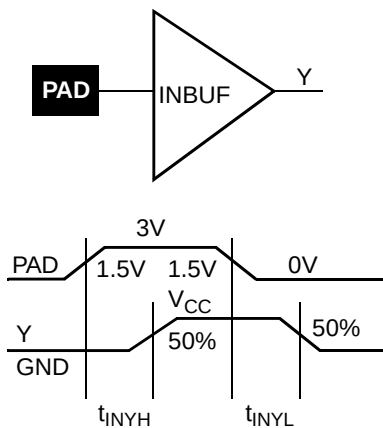
**Load 1**  
(Used to measure propagation delay)



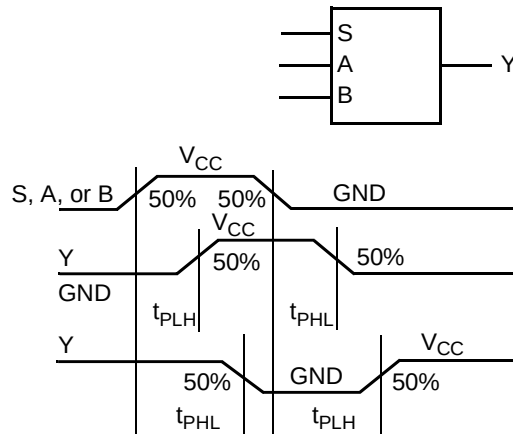
**Load 2**  
(Used to measure rising/falling edges)



### Input Buffer Delays

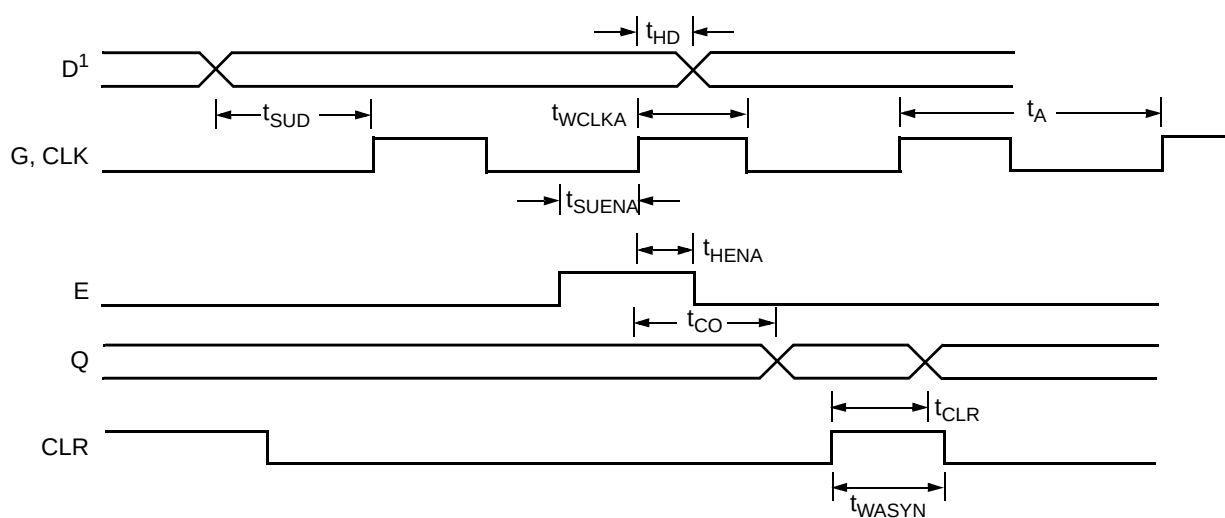
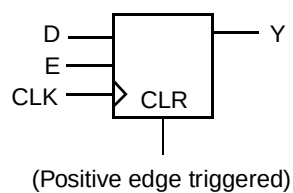


### Combinatorial Macro Delays



## Sequential Timing Characteristics

### Flip-Flops and Latches (ACT 3)

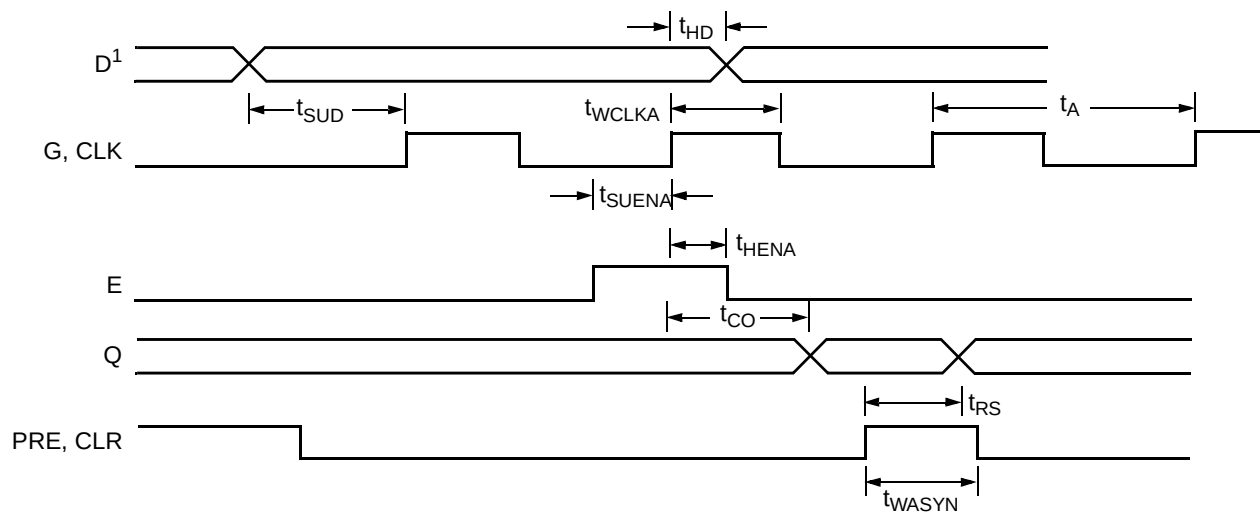
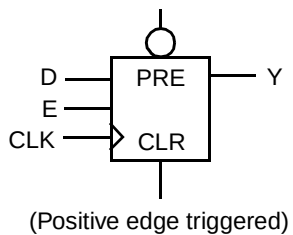


**Note:**

1. *D* represents all data functions involving A, B, and S for multiplexed flip-flops.

## Sequential Timing Characteristics (continued)

### Flip-Flops and Latches (1200XL/3200DX, ACT 2, and ACT 1)

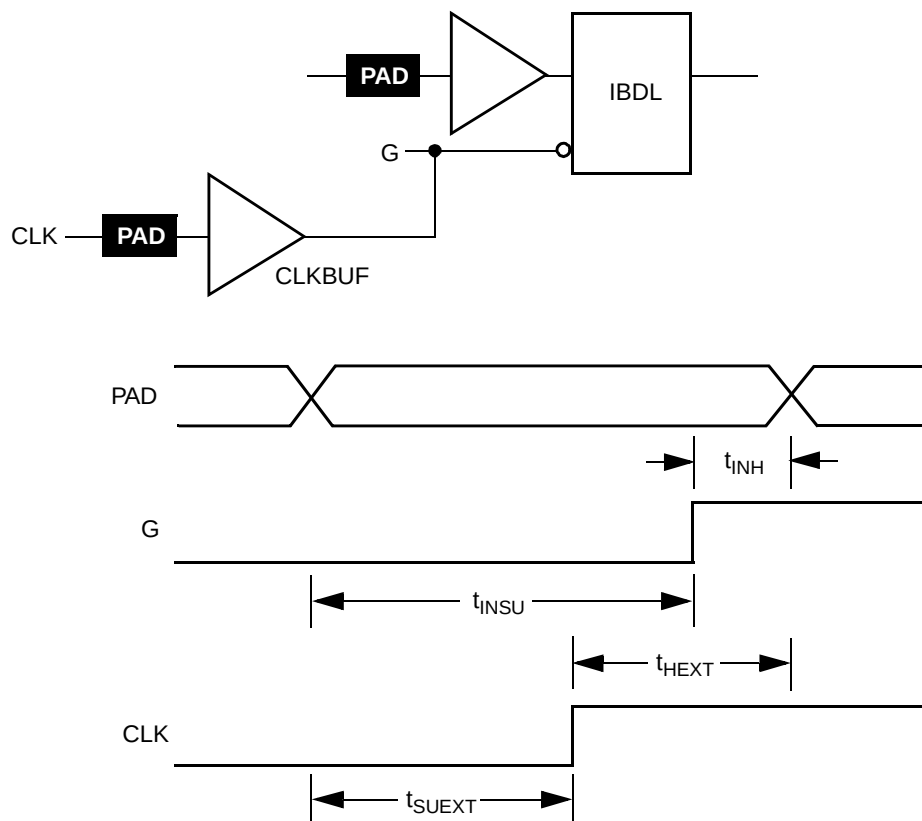


**Note:**

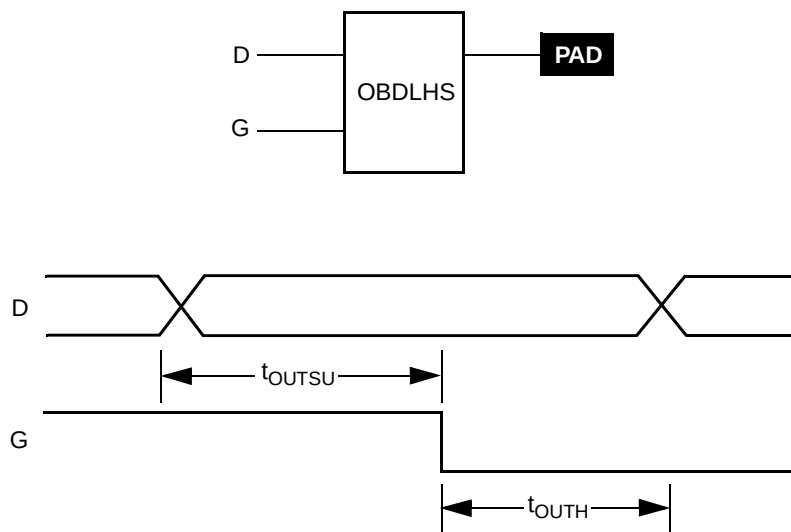
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

## Sequential Timing Characteristics (continued)

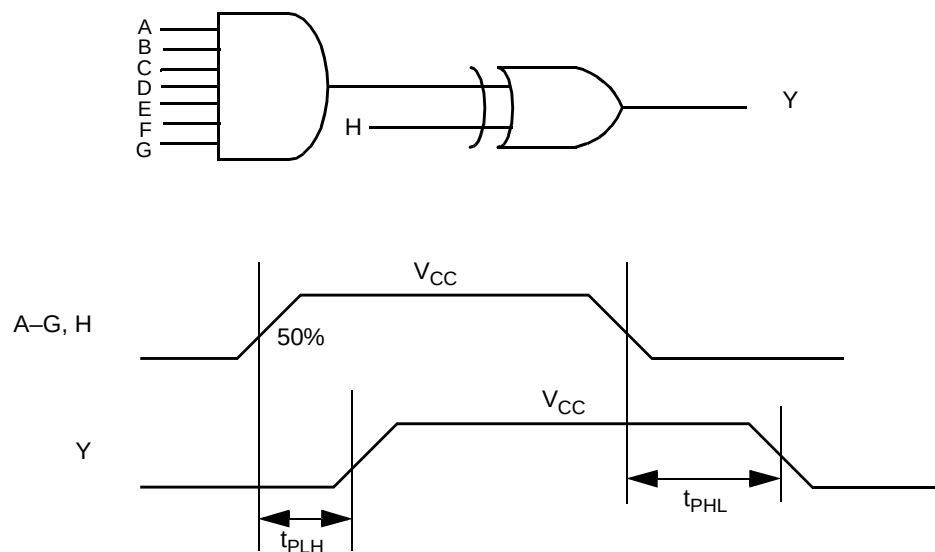
### Input Buffer Latches (ACT 2 and 1200XL/3200DX)



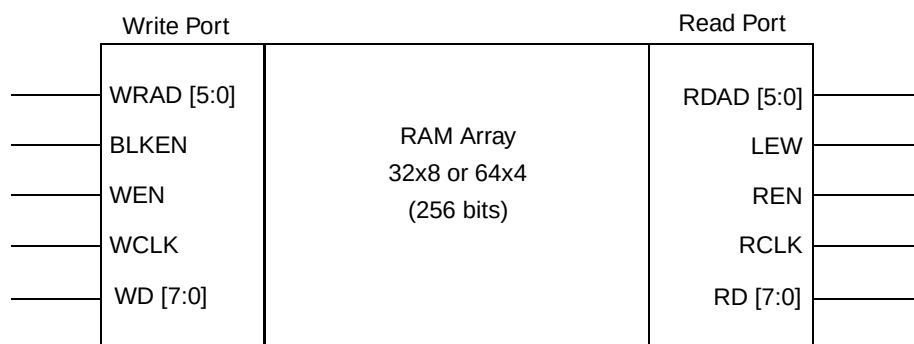
### Output Buffer Latches (ACT 2 and 1200XL/3200DX)



## Decode Module Timing

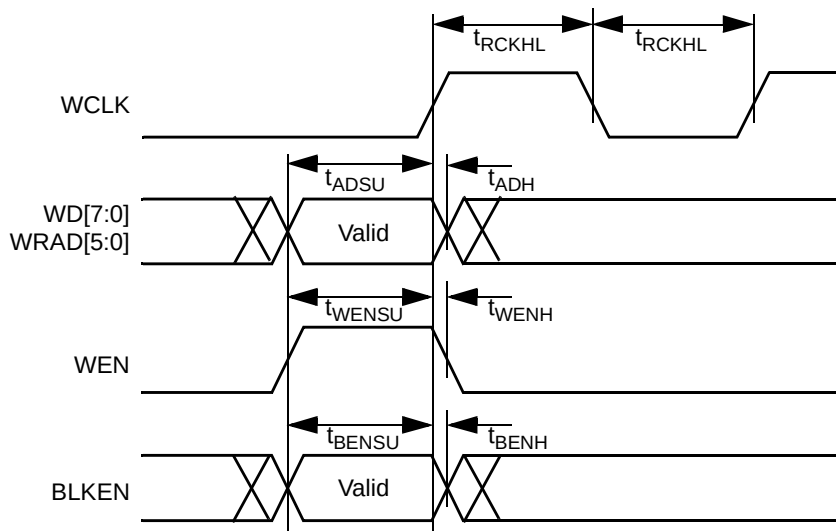


## SRAM Timing Characteristics



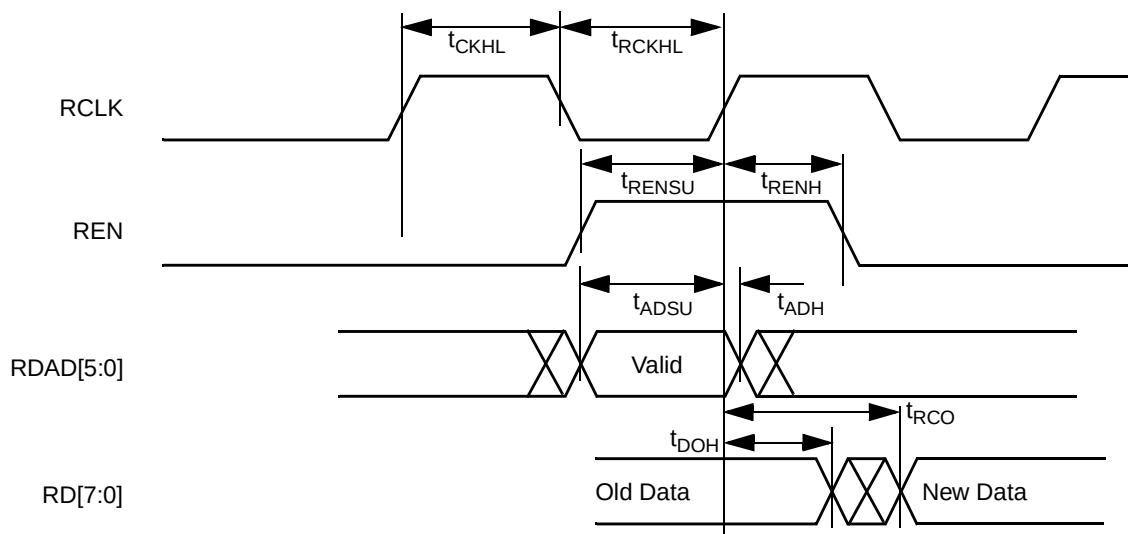
## Dual-Port SRAM Timing Waveforms

### 3200DX SRAM Write Operation



**Note:** Identical timing for falling-edge clock.

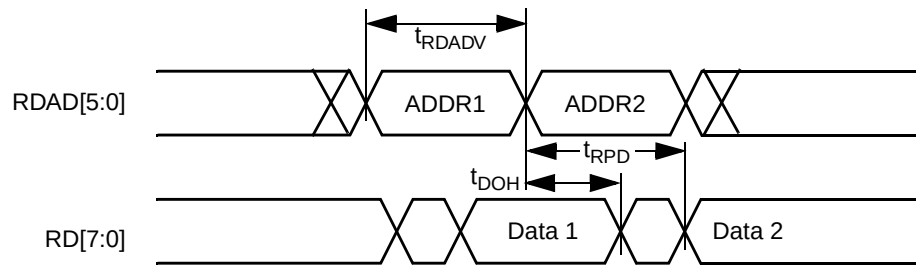
### 3200DX SRAM Synchronous Read Operation



**Note:** Identical timing for falling-edge clock.

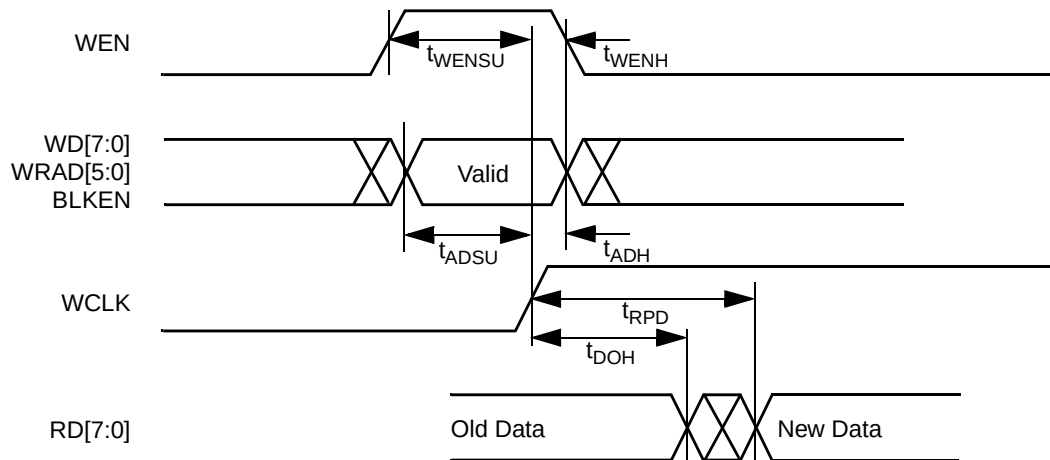
### 3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



### 3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



**ACT 1 Timing Characteristics****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                                             |                                            | '-1' Speed |      | 'Std' Speed |      |       |
|-------------------------------------------------------------|--------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                   | Description                                | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Propagation Delays</b>                      |                                            |            |      |             |      |       |
| $t_{PD1}$                                                   | Single Module                              |            | 4.7  |             | 5.5  | ns    |
| $t_{PD2}$                                                   | Dual Module Macros                         |            | 10.8 |             | 12.7 | ns    |
| $t_{CO}$                                                    | Sequential Clk to Q                        |            | 4.7  |             | 5.5  | ns    |
| $t_{GO}$                                                    | Latch G to Q                               |            | 4.7  |             | 5.5  | ns    |
| $t_{RS}$                                                    | Flip-Flop (Latch) Reset to Q               |            | 4.7  |             | 5.5  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b>    |                                            |            |      |             |      |       |
| $t_{RD1}$                                                   | FO=1 Routing Delay                         |            | 1.5  |             | 1.7  | ns    |
| $t_{RD2}$                                                   | FO=2 Routing Delay                         |            | 2.3  |             | 2.7  | ns    |
| $t_{RD3}$                                                   | FO=3 Routing Delay                         |            | 3.4  |             | 4.0  | ns    |
| $t_{RD4}$                                                   | FO=4 Routing Delay                         |            | 5.0  |             | 5.9  | ns    |
| $t_{RD8}$                                                   | FO=8 Routing Delay                         |            | 10.6 |             | 12.5 | ns    |
| <b>Logic Module Sequential Timing <sup>2</sup></b>          |                                            |            |      |             |      |       |
| $t_{SUD}$                                                   | Flip-Flop (Latch) Data Input Setup         | 8.8        |      | 10.4        |      | ns    |
| $t_{HD}$                                                    | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0         |      | ns    |
| $t_{SUENA}$                                                 | Flip-Flop (Latch) Enable Setup             | 8.8        |      | 10.4        |      | ns    |
| $t_{HENA}$                                                  | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$                                                 | Flip-Flop (Latch) Clock Active Pulse Width | 10.9       |      | 12.9        |      | ns    |
| $t_{WASYN}$                                                 | Flip-Flop (Latch) Asynchronous Pulse Width | 10.9       |      | 12.9        |      | ns    |
| $t_A$                                                       | Flip-Flop Clock Input Period               | 23.2       |      | 27.3        |      | ns    |
| $f_{MAX}$                                                   | Flip-Flop (Latch) Clock Frequency          |            | 44   |             | 37   | MHz   |
| <b>Input Module Propagation Delays</b>                      |                                            |            |      |             |      |       |
| $t_{INYH}$                                                  | Pad to Y High                              |            | 4.9  |             | 5.8  | ns    |
| $t_{INYL}$                                                  | Pad to Y Low                               |            | 4.9  |             | 5.8  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1, 3</sup></b> |                                            |            |      |             |      |       |
| $t_{IRD1}$                                                  | FO=1 Routing Delay                         |            | 1.5  |             | 1.7  | ns    |
| $t_{IRD2}$                                                  | FO=2 Routing Delay                         |            | 2.3  |             | 2.7  | ns    |
| $t_{IRD3}$                                                  | FO=3 Routing Delay                         |            | 3.4  |             | 4.0  | ns    |
| $t_{IRD4}$                                                  | FO=4 Routing Delay                         |            | 5.0  |             | 5.9  | ns    |
| $t_{IRD8}$                                                  | FO=8 Routing Delay                         |            | 10.6 |             | 12.5 | ns    |

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
2. Setup times assume fanout of 3. Further derating information can be obtained from the DirectTime Analyzer utility.
3. Optimization techniques may further reduce delays by 0 to 4 ns.

## ACT 1 Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                              |                          |                     | '-1' Speed   |              | 'Std' Speed  |              |       |
|----------------------------------------------|--------------------------|---------------------|--------------|--------------|--------------|--------------|-------|
| Parameter                                    | Description              |                     | Min.         | Max.         | Min.         | Max.         | Units |
| <b>Global Clock Network</b>                  |                          |                     |              |              |              |              |       |
| $t_{CKH}$                                    | Input Low to High        | FO = 16<br>FO = 128 |              | 7.8<br>8.9   |              | 9.2<br>10.5  | ns    |
| $t_{CKL}$                                    | Input High to Low        | FO = 16<br>FO = 128 |              | 10.3<br>11.2 |              | 12.1<br>13.2 | ns    |
| $t_{PWH}$                                    | Minimum Pulse Width High | FO = 16<br>FO = 128 | 10.4<br>10.9 |              | 12.2<br>12.9 |              | ns    |
| $t_{PWL}$                                    | Minimum Pulse Width Low  | FO = 16<br>FO = 128 | 10.4<br>10.9 |              | 12.2<br>12.9 |              | ns    |
| $t_{CKSW}$                                   | Maximum Skew             | FO = 16<br>FO = 128 |              | 1.9<br>2.9   |              | 2.2<br>3.4   | ns    |
| $t_P$                                        | Minimum Period           | FO = 16<br>FO = 128 | 21.7<br>23.2 |              | 25.6<br>27.3 |              | ns    |
| $f_{MAX}$                                    | Maximum Frequency        | FO = 16<br>FO = 128 |              | 46<br>44     |              | 40<br>37     | MHz   |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                          |                     |              |              |              |              |       |
| $t_{DLH}$                                    | Data to Pad High         |                     |              | 12.1         |              | 14.2         | ns    |
| $t_{DHL}$                                    | Data to Pad Low          |                     |              | 13.8         |              | 16.3         | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High     |                     |              | 12.0         |              | 14.1         | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low      |                     |              | 14.6         |              | 17.1         | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z     |                     |              | 16.0         |              | 18.8         | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z      |                     |              | 14.5         |              | 17.0         | ns    |
| $d_{TLH}$                                    | Delta Low to High        |                     |              | 0.09         |              | 0.11         | ns/pF |
| $d_{THL}$                                    | Delta High to Low        |                     |              | 0.12         |              | 0.15         | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                          |                     |              |              |              |              |       |
| $t_{DLH}$                                    | Data to Pad High         |                     |              | 15.1         |              | 17.7         | ns    |
| $t_{DHL}$                                    | Data to Pad Low          |                     |              | 11.5         |              | 13.6         | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High     |                     |              | 12.0         |              | 14.1         | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low      |                     |              | 14.6         |              | 17.1         | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z     |                     |              | 16.0         |              | 18.8         | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z      |                     |              | 14.5         |              | 17.0         | ns    |
| $d_{TLH}$                                    | Delta Low to High        |                     |              | 0.16         |              | 0.18         | ns/pF |
| $d_{THL}$                                    | Delta High to Low        |                     |              | 0.09         |              | 0.11         | ns/pF |

### Notes:

1. Delays based on 50 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

**A1240A Timing Characteristics****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                                          |                                            | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|--------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                | Description                                | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>       |                                            |            |      |             |      |       |
| $t_{PD1}$                                                | Single Module                              |            | 5.2  |             | 6.1  | ns    |
| $t_{CO}$                                                 | Sequential Clk to Q                        |            | 5.2  |             | 6.1  | ns    |
| $t_{GO}$                                                 | Latch G to Q                               |            | 5.2  |             | 6.1  | ns    |
| $t_{RS}$                                                 | Flip-Flop (Latch) Reset to Q               |            | 5.2  |             | 6.1  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |                                            |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay                         |            | 1.9  |             | 2.2  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay                         |            | 2.4  |             | 2.8  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay                         |            | 3.1  |             | 3.7  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay                         |            | 4.3  |             | 5.0  | ns    |
| $t_{RD8}$                                                | FO=8 Routing Delay                         |            | 6.6  |             | 7.7  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |                                            |            |      |             |      |       |
| $t_{SUD}$                                                | Flip-Flop (Latch) Data Input Setup         | 0.5        |      | 0.5         |      | ns    |
| $t_{HD}$                                                 | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0         |      | ns    |
| $t_{SUENA}$                                              | Flip-Flop (Latch) Enable Setup             | 1.3        |      | 1.3         |      | ns    |
| $t_{HENA}$                                               | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$                                              | Flip-Flop (Latch) Clock Active Pulse Width | 7.4        |      | 8.1         |      | ns    |
| $t_{WASYN}$                                              | Flip-Flop (Latch) Asynchronous Pulse Width | 7.4        |      | 8.1         |      | ns    |
| $t_A$                                                    | Flip-Flop Clock Input Period               | 14.8       |      | 18.6        |      | ns    |
| $t_{INH}$                                                | Input Buffer Latch Hold                    | 2.5        |      | 2.5         |      | ns    |
| $t_{INSU}$                                               | Input Buffer Latch Setup                   | -3.5       |      | -3.5        |      | ns    |
| $t_{OUTH}$                                               | Output Buffer Latch Hold                   | 0.0        |      | 0.0         |      | ns    |
| $t_{OUTSU}$                                              | Output Buffer Latch Setup                  | 0.5        |      | 0.5         |      | ns    |
| $f_{MAX}$                                                | Flip-Flop (Latch) Clock Frequency          |            | 63   |             | 54   | MHz   |

**Notes:**

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1240A Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                            |          | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|----------------------------|----------|------------|------|-------------|------|-------|
| Parameter                                                | Description                |          | Min.       | Max. | Min.        | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                            |          |            |      |             |      |       |
| $t_{INYH}$                                               | Pad to Y High              |          |            | 4.0  |             | 4.7  | ns    |
| $t_{INYL}$                                               | Pad to Y Low               |          |            | 3.6  |             | 4.3  | ns    |
| $t_{INGH}$                                               | G to Y High                |          |            | 6.9  |             | 8.1  | ns    |
| $t_{INGL}$                                               | G to Y Low                 |          |            | 6.6  |             | 7.7  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                            |          |            |      |             |      |       |
| $t_{IRD1}$                                               | FO=1 Routing Delay         |          |            | 5.8  |             | 6.9  | ns    |
| $t_{IRD2}$                                               | FO=2 Routing Delay         |          |            | 6.7  |             | 7.8  | ns    |
| $t_{IRD3}$                                               | FO=3 Routing Delay         |          |            | 7.5  |             | 8.8  | ns    |
| $t_{IRD4}$                                               | FO=4 Routing Delay         |          |            | 8.2  |             | 9.7  | ns    |
| $t_{IRD8}$                                               | FO=8 Routing Delay         |          |            | 10.9 |             | 12.9 | ns    |
| <b>Global Clock Network</b>                              |                            |          |            |      |             |      |       |
| $t_{CKH}$                                                | Input Low to High          | FO = 32  |            | 13.3 |             | 15.7 | ns    |
|                                                          |                            | FO = 256 |            | 16.3 |             | 19.2 |       |
| $t_{CKL}$                                                | Input High to Low          | FO = 32  |            | 13.3 |             | 15.7 | ns    |
|                                                          |                            | FO = 256 |            | 16.5 |             | 19.5 |       |
| $t_{PWH}$                                                | Minimum Pulse Width High   | FO = 32  | 5.7        |      | 6.7         |      | ns    |
|                                                          |                            | FO = 256 | 6.0        |      | 7.1         |      |       |
| $t_{PWL}$                                                | Minimum Pulse Width Low    | FO = 32  | 5.7        |      | 6.7         |      | ns    |
|                                                          |                            | FO = 256 | 6.0        |      | 7.1         |      |       |
| $t_{CKSW}$                                               | Maximum Skew               | FO = 32  |            | 0.6  |             | 0.6  | ns    |
|                                                          |                            | FO = 256 |            | 3.1  |             | 3.1  |       |
| $t_{SUEXT}$                                              | Input Latch External Setup | FO = 32  | 0.0        |      | 0.0         |      | ns    |
|                                                          |                            | FO = 256 | 0.0        |      | 0.0         |      |       |
| $t_{HEXT}$                                               | Input Latch External Hold  | FO = 32  | 8.6        |      | 8.6         |      | ns    |
|                                                          |                            | FO = 256 | 13.8       |      | 13.8        |      |       |
| $t_P$                                                    | Minimum Period             | FO = 32  | 11.5       |      | 13.5        |      | ns    |
|                                                          |                            | FO = 256 | 12.2       |      | 14.3        |      |       |
| $f_{MAX}$                                                | Maximum Frequency          | FO = 32  |            | 87   |             | 74   | MHz   |
|                                                          |                            | FO = 256 |            | 82   |             | 70   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

**A1240A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                              |                      | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------|----------------------|------------|------|-------------|------|-------|
| Parameter                                    | Description          | Min.       | Max. | Min.        | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                      |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High     |            | 11.0 |             | 13.0 | ns    |
| $t_{DHL}$                                    | Data to Pad Low      |            | 13.9 |             | 16.4 | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High |            | 12.3 |             | 14.4 | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low  |            | 16.1 |             | 19.0 | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z |            | 9.8  |             | 11.5 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z  |            | 11.5 |             | 13.6 | ns    |
| $t_{GLH}$                                    | G to Pad High        |            | 12.4 |             | 14.6 | ns    |
| $t_{GHL}$                                    | G to Pad Low         |            | 15.5 |             | 18.2 | ns    |
| $d_{TLH}$                                    | Delta Low to High    |            | 0.09 |             | 0.11 | ns/pF |
| $d_{THL}$                                    | Delta High to Low    |            | 0.17 |             | 0.20 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                      |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High     |            | 14.0 |             | 16.5 | ns    |
| $t_{DHL}$                                    | Data to Pad Low      |            | 11.7 |             | 13.7 | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High |            | 12.3 |             | 14.4 | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low  |            | 16.1 |             | 19.0 | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z |            | 9.8  |             | 11.5 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z  |            | 11.5 |             | 13.6 | ns    |
| $t_{GLH}$                                    | G to Pad High        |            | 12.4 |             | 14.6 | ns    |
| $t_{GHL}$                                    | G to Pad Low         |            | 15.5 |             | 18.2 | ns    |
| $d_{TLH}$                                    | Delta Low to High    |            | 0.17 |             | 0.20 | ns/pF |
| $d_{THL}$                                    | Delta High to Low    |            | 0.12 |             | 0.15 | ns/pF |

**Notes:**

1. Delays based on 50 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

## A1280A Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                                            | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|--------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                | Description                                | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>       |                                            |            |      |             |      |       |
| $t_{PD1}$                                                | Single Module                              |            | 5.2  |             | 6.1  | ns    |
| $t_{CO}$                                                 | Sequential Clk to Q                        |            | 5.2  |             | 6.1  | ns    |
| $t_{GO}$                                                 | Latch G to Q                               |            | 5.2  |             | 6.1  | ns    |
| $t_{RS}$                                                 | Flip-Flop (Latch) Reset to Q               |            | 5.2  |             | 6.1  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |                                            |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay                         |            | 2.4  |             | 2.8  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay                         |            | 3.4  |             | 4.0  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay                         |            | 4.2  |             | 4.9  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay                         |            | 5.1  |             | 6.0  | ns    |
| $t_{RD8}$                                                | FO=8 Routing Delay                         |            | 9.2  |             | 10.8 | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |                                            |            |      |             |      |       |
| $t_{SUD}$                                                | Flip-Flop (Latch) Data Input Setup         | 0.5        |      | 0.5         |      | ns    |
| $t_{HD}$                                                 | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0         |      | ns    |
| $t_{SUENA}$                                              | Flip-Flop (Latch) Enable Setup             | 1.3        |      | 1.3         |      | ns    |
| $t_{HENA}$                                               | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$                                              | Flip-Flop (Latch) Clock Active Pulse Width | 7.4        |      | 8.6         |      | ns    |
| $t_{WASYN}$                                              | Flip-Flop (Latch) Asynchronous Pulse Width | 7.4        |      | 8.6         |      | ns    |
| $t_A$                                                    | Flip-Flop Clock Input Period               | 16.4       |      | 22.1        |      | ns    |
| $t_{INH}$                                                | Input Buffer Latch Hold                    | 2.5        |      | 2.5         |      | ns    |
| $t_{INSU}$                                               | Input Buffer Latch Setup                   | -3.5       |      | -3.5        |      | ns    |
| $t_{OUTH}$                                               | Output Buffer Latch Hold                   | 0.0        |      | 0.0         |      | ns    |
| $t_{OUTSU}$                                              | Output Buffer Latch Setup                  | 0.5        |      | 0.5         |      | ns    |
| $f_{MAX}$                                                | Flip-Flop (Latch) Clock Frequency          |            | 60   |             | 41   | MHz   |

### Notes:

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
4. Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A1280A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                                          |                            |          | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|----------------------------|----------|------------|------|-------------|------|-------|
| Parameter                                                | Description                |          | Min.       | Max. | Min.        | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                            |          |            |      |             |      |       |
| $t_{INYH}$                                               | Pad to Y High              |          |            | 4.0  |             | 4.7  | ns    |
| $t_{INYL}$                                               | Pad to Y Low               |          |            | 3.6  |             | 4.3  | ns    |
| $t_{INGH}$                                               | G to Y High                |          |            | 6.9  |             | 8.1  | ns    |
| $t_{INGL}$                                               | G to Y Low                 |          |            | 6.6  |             | 7.7  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                            |          |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay         |          |            | 6.2  |             | 7.3  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay         |          |            | 7.2  |             | 8.4  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay         |          |            | 7.7  |             | 9.1  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay         |          |            | 8.9  |             | 10.5 | ns    |
| $t_{RD8}$                                                | FO=8 Routing Delay         |          |            | 12.9 |             | 15.2 | ns    |
| <b>Global Clock Network</b>                              |                            |          |            |      |             |      |       |
| $t_{CKH}$                                                | Input Low to High          | FO = 32  |            | 13.3 |             | 15.7 | ns    |
|                                                          |                            | FO = 384 |            | 17.9 |             | 21.1 |       |
| $t_{CKL}$                                                | Input High to Low          | FO = 32  |            | 13.3 |             | 15.7 | ns    |
|                                                          |                            | FO = 384 |            | 18.2 |             | 21.4 |       |
| $t_{PWH}$                                                | Minimum Pulse Width High   | FO = 32  | 6.9        |      | 8.1         |      | ns    |
|                                                          |                            | FO = 384 | 7.9        |      | 9.3         |      |       |
| $t_{PWL}$                                                | Minimum Pulse Width Low    | FO = 32  | 6.9        |      | 8.1         |      | ns    |
|                                                          |                            | FO = 384 | 7.9        |      | 9.3         |      |       |
| $t_{CKSW}$                                               | Maximum Skew               | FO = 32  |            | 0.6  |             | 0.6  | ns    |
|                                                          |                            | FO = 384 |            | 3.1  |             | 3.1  |       |
| $t_{SUEXT}$                                              | Input Latch External Setup | FO = 32  | 0.0        |      | 0.0         |      | ns    |
|                                                          |                            | FO = 384 | 0.0        |      | 0.0         |      |       |
| $t_{HEXT}$                                               | Input Latch External Hold  | FO = 32  | 8.6        |      | 8.6         |      | ns    |
|                                                          |                            | FO = 384 | 13.8       |      | 13.8        |      |       |
| $t_P$                                                    | Minimum Period             | FO = 32  | 13.7       |      | 16.2        |      | ns    |
|                                                          |                            | FO = 384 | 16.0       |      | 18.9        |      |       |
| $f_{MAX}$                                                | Maximum Frequency          | FO = 32  |            | 73   |             | 62   | MHz   |
|                                                          |                            | FO = 384 |            | 63   |             | 53   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

## A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                              |                      | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|----------------------------------------------|----------------------|------------|------|-------------|------|-------|
| Parameter                                    | Description          | Min.       | Max. | Min.        | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                      |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High     |            | 11.0 |             | 13.0 | ns    |
| $t_{DHL}$                                    | Data to Pad Low      |            | 13.9 |             | 16.4 | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High |            | 12.3 |             | 14.4 | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low  |            | 16.1 |             | 19.0 | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z |            | 9.8  |             | 11.5 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z  |            | 11.5 |             | 13.6 | ns    |
| $t_{GLH}$                                    | G to Pad High        |            | 12.4 |             | 14.6 | ns    |
| $t_{GHL}$                                    | G to Pad Low         |            | 15.5 |             | 18.2 | ns    |
| $d_{TLH}$                                    | Delta Low to High    |            | 0.09 |             | 0.11 | ns/pF |
| $d_{THL}$                                    | Delta High to Low    |            | 0.17 |             | 0.20 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                      |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High     |            | 14.0 |             | 16.5 | ns    |
| $t_{DHL}$                                    | Data to Pad Low      |            | 11.7 |             | 13.7 | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High |            | 12.3 |             | 14.4 | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low  |            | 16.1 |             | 19.0 | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z |            | 9.8  |             | 11.5 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z  |            | 11.5 |             | 13.6 | ns    |
| $t_{GLH}$                                    | G to Pad High        |            | 12.4 |             | 14.6 | ns    |
| $t_{GHL}$                                    | G to Pad Low         |            | 15.5 |             | 18.2 | ns    |
| $d_{TLH}$                                    | Delta Low to High    |            | 0.17 |             | 0.20 | ns/pF |
| $d_{THL}$                                    | Delta High to Low    |            | 0.12 |             | 0.15 | ns/pF |

**Notes:**

1. Delays based on 50 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

## A1280XL Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                                            | '–1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|--------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                | Description                                | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>       |                                            |            |      |             |      |       |
| $t_{PD1}$                                                | Single Module                              |            | 3.7  |             | 4.3  | ns    |
| $t_{CO}$                                                 | Sequential Clk to Q                        |            | 3.7  |             | 4.3  | ns    |
| $t_{GO}$                                                 | Latch G to Q                               |            | 3.7  |             | 4.3  | ns    |
| $t_{RS}$                                                 | Flip-Flop (Latch) Reset to Q               |            | 3.7  |             | 4.3  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |                                            |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay                         |            | 1.7  |             | 2.1  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay                         |            | 2.5  |             | 3.0  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay                         |            | 3.1  |             | 3.6  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay                         |            | 3.7  |             | 4.3  | ns    |
| $t_{RD8}$                                                | FO=8 Routing Delay                         |            | 7.0  |             | 8.3  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |                                            |            |      |             |      |       |
| $t_{SUD}$                                                | Flip-Flop (Latch) Data Input Setup         | 0.4        |      | 0.5         |      | ns    |
| $t_{HD}$                                                 | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0         |      | ns    |
| $t_{SUENA}$                                              | Flip-Flop (Latch) Enable Setup             | 1.1        |      | 1.2         |      | ns    |
| $t_{HENA}$                                               | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$                                              | Flip-Flop (Latch) Clock Active Pulse Width | 5.3        |      | 6.1         |      | ns    |
| $t_{WASYN}$                                              | Flip-Flop (Latch) Asynchronous Pulse Width | 5.3        |      | 6.1         |      | ns    |
| $t_A$                                                    | Flip-Flop Clock Input Period               | 10.7       |      | 12.3        |      | ns    |
| $t_{INH}$                                                | Input Buffer Latch Hold                    | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$                                               | Input Buffer Latch Setup                   | 0.4        |      | 0.4         |      | ns    |
| $t_{OUTH}$                                               | Output Buffer Latch Hold                   | 0.0        |      | 0.0         |      | ns    |
| $t_{OUTSU}$                                              | Output Buffer Latch Setup                  | 0.4        |      | 0.4         |      | ns    |
| $f_{MAX}$                                                | Flip-Flop (Latch) Clock Frequency          |            | 90   |             | 75   | MHz   |

### Notes:

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.
- Setup and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

## A1280XL Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                            |          | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|----------------------------|----------|------------|------|-------------|------|-------|
| Parameter                                                | Description                |          | Min.       | Max. | Min.        | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                            |          |            |      |             |      |       |
| $t_{INYH}$                                               | Pad to Y High              |          |            | 1.5  |             | 1.7  | ns    |
| $t_{INYL}$                                               | Pad to Y Low               |          |            | 1.7  |             | 2.1  | ns    |
| $t_{INGH}$                                               | G to Y High                |          |            | 2.8  |             | 3.3  | ns    |
| $t_{INGL}$                                               | G to Y Low                 |          |            | 3.7  |             | 4.3  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                            |          |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay         |          |            | 4.6  |             | 5.3  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay         |          |            | 5.2  |             | 6.1  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay         |          |            | 5.5  |             | 6.5  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay         |          |            | 6.4  |             | 7.5  | ns    |
| $t_{RD8}$                                                | FO=8 Routing Delay         |          |            | 9.2  |             | 10.8 | ns    |
| <b>Global Clock Network</b>                              |                            |          |            |      |             |      |       |
| $t_{CKH}$                                                | Input Low to High          | FO = 32  |            | 7.1  |             | 8.4  | ns    |
|                                                          |                            | FO = 384 |            | 8.0  |             | 9.5  |       |
| $t_{CKL}$                                                | Input High to Low          | FO = 32  |            | 7.0  |             | 8.3  | ns    |
|                                                          |                            | FO = 384 |            | 8.0  |             | 9.5  |       |
| $t_{PWH}$                                                | Minimum Pulse Width High   | FO = 32  | 4.3        |      | 5.3         |      | ns    |
|                                                          |                            | FO = 384 | 4.8        |      | 5.7         |      |       |
| $t_{PWL}$                                                | Minimum Pulse Width Low    | FO = 32  | 4.3        |      | 5.3         |      | ns    |
|                                                          |                            | FO = 384 | 4.8        |      | 5.7         |      |       |
| $t_{CKSW}$                                               | Maximum Skew               | FO = 32  |            | 1.1  |             | 1.2  | ns    |
|                                                          |                            | FO = 384 |            | 1.1  |             | 1.2  |       |
| $t_{SUEXT}$                                              | Input Latch External Setup | FO = 32  | 0.0        |      | 0.0         |      | ns    |
|                                                          |                            | FO = 384 | 0.0        |      | 0.0         |      |       |
| $t_{HEXT}$                                               | Input Latch External Hold  | FO = 32  | 3.6        |      | 4.2         |      | ns    |
|                                                          |                            | FO = 384 | 4.6        |      | 5.3         |      |       |
| $t_P$                                                    | Minimum Period             | FO = 32  | 9.1        |      | 10.7        |      | ns    |
|                                                          |                            | FO = 384 | 9.8        |      | 11.8        |      |       |
| $f_{MAX}$                                                | Maximum Frequency          | FO = 32  |            | 110  |             | 90   | MHz   |
|                                                          |                            | FO = 384 |            | 100  |             | 85   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

**A1280XL Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                              |                      | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------|----------------------|------------|------|-------------|------|-------|
| Parameter                                    | Description          | Min.       | Max. | Min.        | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                      |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High     |            | 5.3  |             | 6.2  | ns    |
| $t_{DHL}$                                    | Data to Pad Low      |            | 5.7  |             | 6.6  | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High |            | 5.3  |             | 6.2  | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low  |            | 5.8  |             | 6.8  | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z |            | 7.5  |             | 8.9  | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z  |            | 7.5  |             | 8.9  | ns    |
| $t_{GLH}$                                    | G to Pad High        |            | 5.9  |             | 6.9  | ns    |
| $t_{GHL}$                                    | G to Pad Low         |            | 6.6  |             | 7.8  | ns    |
| $d_{TLH}$                                    | Delta Low to High    |            | 0.05 |             | 0.06 | ns/pF |
| $d_{THL}$                                    | Delta High to Low    |            | 0.05 |             | 0.09 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                      |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High     |            | 6.6  |             | 7.9  | ns    |
| $t_{DHL}$                                    | Data to Pad Low      |            | 4.7  |             | 5.5  | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High |            | 5.3  |             | 6.2  | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low  |            | 5.8  |             | 6.8  | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z |            | 7.5  |             | 8.9  | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z  |            | 7.5  |             | 8.9  | ns    |
| $t_{GLH}$                                    | G to Pad High        |            | 5.9  |             | 6.9  | ns    |
| $t_{GHL}$                                    | G to Pad Low         |            | 6.6  |             | 7.8  | ns    |
| $d_{TLH}$                                    | Delta Low to High    |            | 0.07 |             | 0.09 | ns/pF |
| $d_{THL}$                                    | Delta High to Low    |            | 0.06 |             | 0.09 | ns/pF |

**Notes:**

1. Delays based on 50 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

## A1425A Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^\circ C$ )

|                                                             |                                    | '-1' Speed |      | 'Std' Speed |      |       |
|-------------------------------------------------------------|------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                   | Description                        | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>          |                                    |            |      |             |      |       |
| $t_{PD}$                                                    | Internal Array Module              |            | 3.0  |             | 3.5  | ns    |
| $t_{CO}$                                                    | Sequential Clock to Q              |            | 3.0  |             | 3.5  | ns    |
| $t_{CLR}$                                                   | Asynchronous Clear to Q            |            | 3.0  |             | 3.5  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b>    |                                    |            |      |             |      |       |
| $t_{RD1}$                                                   | FO=1 Routing Delay                 |            | 1.3  |             | 1.5  | ns    |
| $t_{RD2}$                                                   | FO=2 Routing Delay                 |            | 1.9  |             | 2.1  | ns    |
| $t_{RD3}$                                                   | FO=3 Routing Delay                 |            | 2.1  |             | 2.5  | ns    |
| $t_{RD4}$                                                   | FO=4 Routing Delay                 |            | 2.6  |             | 2.9  | ns    |
| $t_{RD8}$                                                   | FO=8 Routing Delay                 |            | 4.2  |             | 4.9  | ns    |
| <b>Logic Module Sequential Timing</b>                       |                                    |            |      |             |      |       |
| $t_{SUD}$                                                   | Flip-Flop (Latch) Data Input Setup | 0.9        |      | 1.0         |      | ns    |
| $t_{HD}$                                                    | Flip-Flop (Latch) Data Input Hold  | 0.0        |      | 0.0         |      | ns    |
| $t_{SUENA}$                                                 | Flip-Flop (Latch) Enable Setup     | 0.9        |      | 1.0         |      | ns    |
| $t_{HENA}$                                                  | Flip-Flop (Latch) Enable Hold      | 0.0        |      | 0.0         |      | ns    |
| $t_{WASYN}$                                                 | Asynchronous Pulse Width           | 3.8        |      | 4.4         |      | ns    |
| $t_{WCLKA}$                                                 | Flip-Flop Clock Pulse Width        | 3.8        |      | 4.4         |      | ns    |
| $t_A$                                                       | Flip-Flop Clock Input Period       | 7.9        |      | 9.3         |      | ns    |
| $f_{MAX}$                                                   | Flip-Flop Clock Frequency          |            | 125  |             | 100  | MHz   |
| <b>Input Module Propagation Delays</b>                      |                                    |            |      |             |      |       |
| $t_{INY}$                                                   | Input Data Pad to Y                |            | 4.2  |             | 4.9  | ns    |
| $t_{ICKY}$                                                  | Input Reg IOCLK Pad to Y           |            | 7.0  |             | 8.2  | ns    |
| $t_{OCKY}$                                                  | Output Reg IOCLK Pad to Y          |            | 7.0  |             | 8.2  | ns    |
| $t_{ICLRY}$                                                 | Input Asynchronous Clear to Y      |            | 7.0  |             | 8.2  | ns    |
| $t_{OCLRY}$                                                 | Output Asynchronous Clear to Y     |            | 7.0  |             | 8.2  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1, 3</sup></b> |                                    |            |      |             |      |       |
| $t_{IRD1}$                                                  | FO=1 Routing Delay                 |            | 1.3  |             | 1.5  | ns    |
| $t_{IRD2}$                                                  | FO=2 Routing Delay                 |            | 1.9  |             | 2.1  | ns    |
| $t_{IRD3}$                                                  | FO=3 Routing Delay                 |            | 2.1  |             | 2.5  | ns    |
| $t_{IRD4}$                                                  | FO=4 Routing Delay                 |            | 2.6  |             | 2.9  | ns    |
| $t_{IRD8}$                                                  | FO=8 Routing Delay                 |            | 4.2  |             | 4.9  | ns    |

### Notes:

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Optimization techniques may further reduce delays by 0 to 4 ns.

**A1425A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                             |                                                | '-1' Speed |      | 'Std' Speed |      |       |
|---------------------------------------------|------------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                   | Description                                    | Min.       | Max. | Min.        | Max. | Units |
| <b>I/O Module Sequential Timing</b>         |                                                |            |      |             |      |       |
| $t_{INH}$                                   | Input F-F Data Hold<br>(w.r.t. IOCLK Pad)      | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$                                  | Input F-F Data Setup<br>(w.r.t. IOCLK Pad)     | 2.1        |      | 2.4         |      | ns    |
| $t_{IDEH}$                                  | Input Data Enable Hold<br>(w.r.t. IOCLK Pad)   | 0.0        |      | 0.0         |      | ns    |
| $t_{IDESU}$                                 | Input Data Enable Setup<br>(w.r.t. IOCLK Pad)  | 8.7        |      | 10.0        |      | ns    |
| $t_{OUTH}$                                  | Output F-F Data Hold<br>(w.r.t. IOCLK Pad)     | 1.1        |      | 1.2         |      | ns    |
| $t_{OUTSU}$                                 | Output F-F Data Setup<br>(w.r.t. IOCLK Pad)    | 1.1        |      | 1.2         |      | ns    |
| $t_{ODEH}$                                  | Output Data Enable Hold<br>(w.r.t. IOCLK Pad)  | 0.5        |      | 0.6         |      | ns    |
| $t_{ODESU}$                                 | Output Data Enable Setup<br>(w.r.t. IOCLK Pad) | 2.0        |      | 2.4         |      | ns    |
| <b>TTL Output Module Timing<sup>1</sup></b> |                                                |            |      |             |      |       |
| $t_{DHS}$                                   | Data to Pad, High Slew                         |            | 7.5  |             | 8.9  | ns    |
| $t_{DLS}$                                   | Data to Pad, Low Slew                          |            | 11.9 |             | 14.0 | ns    |
| $t_{ENZHS}$                                 | Enable to Pad, Z to H/L, High Slew             |            | 6.0  |             | 7.0  | ns    |
| $t_{ENZLS}$                                 | Enable to Pad, Z to H/L, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| $t_{ENHSZ}$                                 | Enable to Pad, H/L to Z, High Slew             |            | 9.9  |             | 11.6 | ns    |
| $t_{ENLSZ}$                                 | Enable to Pad, H/L to Z, Low Slew              |            | 9.9  |             | 11.6 | ns    |
| $t_{CKHS}$                                  | IOCLK Pad to Pad H/L, High Slew                |            | 10.5 |             | 11.6 | ns    |
| $t_{CKLS}$                                  | IOCLK Pad to Pad H/L, Low Slew                 |            | 15.7 |             | 17.4 | ns    |
| $d_{TLHHS}$                                 | Delta Low to High, High Slew                   |            | 0.04 |             | 0.04 | ns/pF |
| $d_{TLHLS}$                                 | Delta Low to High, Low Slew                    |            | 0.07 |             | 0.08 | ns/pF |
| $d_{THLHS}$                                 | Delta High to Low, High Slew                   |            | 0.05 |             | 0.06 | ns/pF |
| $d_{THLLS}$                                 | Delta High to Low, Low Slew                    |            | 0.07 |             | 0.08 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

## A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                   |                                                | '-1' Speed |      | 'Std' Speed |      |       |
|---------------------------------------------------|------------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                         | Description                                    | Min.       | Max. | Min.        | Max. | Units |
| <b>CMOS Output Module Timing<sup>1</sup></b>      |                                                |            |      |             |      |       |
| $t_{DHS}$                                         | Data to Pad, High Slew                         |            | 9.2  |             | 10.8 | ns    |
| $t_{DLS}$                                         | Data to Pad, Low Slew                          |            | 17.3 |             | 20.3 | ns    |
| $t_{ENZHS}$                                       | Enable to Pad, Z to H/L, High Slew             |            | 7.7  |             | 9.1  | ns    |
| $t_{ENZLS}$                                       | Enable to Pad, Z to H/L, Low Slew              |            | 13.1 |             | 15.5 | ns    |
| $t_{ENHSZ}$                                       | Enable to Pad, H/L to Z, High Slew             |            | 9.9  |             | 11.6 | ns    |
| $t_{ENLSZ}$                                       | Enable to Pad, H/L to Z, Low Slew              |            | 10.5 |             | 11.6 | ns    |
| $t_{CKHS}$                                        | IOCLK Pad to Pad H/L, High Slew                |            | 12.5 |             | 13.7 | ns    |
| $t_{CKLS}$                                        | IOCLK Pad to Pad H/L, Low Slew                 |            | 18.1 |             | 20.1 | ns    |
| $d_{TLHHS}$                                       | Delta Low to High, High Slew                   |            | 0.06 |             | 0.07 | ns/pF |
| $d_{TLHLS}$                                       | Delta Low to High, Low Slew                    |            | 0.11 |             | 0.13 | ns/pF |
| $d_{THLHS}$                                       | Delta High to Low, High Slew                   |            | 0.04 |             | 0.05 | ns/pF |
| $d_{THLLS}$                                       | Delta High to Low, Low Slew                    |            | 0.05 |             | 0.06 | ns/pF |
| <b>Dedicated (Hard-Wired) I/O Clock Network</b>   |                                                |            |      |             |      |       |
| $t_{IOCKH}$                                       | Input Low to High<br>(Pad to I/O Module Input) |            | 3.0  |             | 3.5  | ns    |
| $t_{IOPWH}$                                       | Minimum Pulse Width High                       | 3.9        |      | 4.4         |      | ns    |
| $t_{IOPWL}$                                       | Minimum Pulse Width Low                        | 3.9        |      | 4.4         |      | ns    |
| $t_{IOSAPW}$                                      | Minimum Asynchronous Pulse Width               | 3.9        |      | 4.4         |      | ns    |
| $t_{IOCKSW}$                                      | Maximum Skew                                   |            | 0.5  |             | 0.5  | ns    |
| $t_{IOP}$                                         | Minimum Period                                 | 7.9        |      | 9.3         |      | ns    |
| $f_{IOMAX}$                                       | Maximum Frequency                              |            | 125  |             | 100  | MHz   |
| <b>Dedicated (Hard-Wired) Array Clock Network</b> |                                                |            |      |             |      |       |
| $t_{HCKH}$                                        | Input Low to High<br>(Pad to S-Module Input)   |            | 4.6  |             | 5.3  | ns    |
| $t_{HCKL}$                                        | Input High to Low<br>(Pad to S-Module Input)   |            | 4.6  |             | 5.3  | ns    |
| $t_{HPWH}$                                        | Minimum Pulse Width High                       | 3.9        |      | 4.4         |      | ns    |
| $t_{HPWL}$                                        | Minimum Pulse Width Low                        | 3.9        |      | 4.4         |      | ns    |
| $t_{HCKSW}$                                       | Maximum Skew                                   |            | 0.4  |             | 0.4  | ns    |
| $t_{HP}$                                          | Minimum Period                                 | 7.9        |      | 9.3         |      | ns    |
| $f_{HMAX}$                                        | Maximum Frequency                              |            | 125  |             | 100  | MHz   |

### Notes:

- Delays based on 35 pF loading.
- SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

**A1425A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                    |                               | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|------------------------------------|-------------------------------|------------|------|-------------|------|-------|
| Parameter                          | Description                   | Min.       | Max. | Min.        | Max. | Units |
| <b>Routed Array Clock Networks</b> |                               |            |      |             |      |       |
| $t_{RCKH}$                         | Input Low to High (FO=64)     |            | 5.5  |             | 6.4  | ns    |
| $t_{RCKL}$                         | Input High to Low (FO=64)     |            | 6.0  |             | 7.0  | ns    |
| $t_{RPWH}$                         | Min. Pulse Width High (FO=64) | 4.9        |      | 5.7         |      | ns    |
| $t_{RPWL}$                         | Min. Pulse Width Low (FO=64)  | 4.9        |      | 5.7         |      | ns    |
| $t_{RCKSW}$                        | Maximum Skew (FO=128)         |            | 1.1  |             | 1.2  | ns    |
| $t_{RP}$                           | Minimum Period (FO=64)        | 10.1       |      | 11.6        |      | ns    |
| $f_{RMAX}$                         | Maximum Frequency (FO=64)     |            | 100  |             | 85   | MHz   |
| <b>Clock-to-Clock Skews</b>        |                               |            |      |             |      |       |
| $t_{IOHCKSW}$                      | I/O Clock to H-Clock Skew     | 0.0        | 3.0  | 0.0         | 3.0  | ns    |
| $t_{IORCKSW}$                      | I/O Clock to R-Clock Skew     | 0.0        | 3.0  | 0.0         | 3.0  | ns    |
| $t_{HRCKSW}$                       | H-Clock to R-Clock Skew       |            |      |             |      |       |
|                                    | (FO = 64)                     | 0.0        | 1.0  | 0.0         | 1.0  | ns    |
|                                    | (FO = 50% max.)               | 0.0        | 3.0  | 0.0         | 3.0  | ns    |

## A1460A Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^\circ C$ )

|                                                       |                                    | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|-------------------------------------------------------|------------------------------------|------------|------|-------------|------|-------|
| Parameter                                             | Description                        | Min.       | Max. | Min.        | Max. | Units |
| Logic Module Propagation Delays <sup>1</sup>          |                                    |            |      |             |      |       |
| t <sub>PD</sub>                                       | Internal Array Module              |            | 3.0  |             | 3.5  | ns    |
| t <sub>CO</sub>                                       | Sequential Clock to Q              |            | 3.0  |             | 3.5  | ns    |
| t <sub>CLR</sub>                                      | Asynchronous Clear to Q            |            | 3.0  |             | 3.5  | ns    |
| Logic Module Predicted Routing Delays <sup>2</sup>    |                                    |            |      |             |      |       |
| t <sub>RD1</sub>                                      | FO=1 Routing Delay                 |            | 1.3  |             | 1.5  | ns    |
| t <sub>RD2</sub>                                      | FO=2 Routing Delay                 |            | 1.9  |             | 2.1  | ns    |
| t <sub>RD3</sub>                                      | FO=3 Routing Delay                 |            | 2.1  |             | 2.5  | ns    |
| t <sub>RD4</sub>                                      | FO=4 Routing Delay                 |            | 2.6  |             | 2.9  | ns    |
| t <sub>RD8</sub>                                      | FO=8 Routing Delay                 |            | 4.2  |             | 4.9  | ns    |
| Logic Module Sequential Timing                        |                                    |            |      |             |      |       |
| t <sub>SUD</sub>                                      | Flip-Flop (Latch) Data Input Setup | 0.9        |      | 1.0         |      | ns    |
| t <sub>HD</sub>                                       | Flip-Flop (Latch) Data Input Hold  | 0.0        |      | 0.0         |      | ns    |
| t <sub>SUENA</sub>                                    | Flip-Flop (Latch) Enable Setup     | 0.9        |      | 1.0         |      | ns    |
| t <sub>HENA</sub>                                     | Flip-Flop (Latch) Enable Hold      | 0.0        |      | 0.0         |      | ns    |
| t <sub>WASYN</sub>                                    | Asynchronous Pulse Width           | 4.8        |      | 5.6         |      | ns    |
| t <sub>WCLKA</sub>                                    | Flip-Flop Clock Pulse Width        | 4.8        |      | 5.6         |      | ns    |
| t <sub>A</sub>                                        | Flip-Flop Clock Input Period       | 9.9        |      | 11.6        |      | ns    |
| f <sub>MAX</sub>                                      | Flip-Flop Clock Frequency          |            | 100  |             | 85   | MHz   |
| Input Module Propagation Delays                       |                                    |            |      |             |      |       |
| t <sub>INY</sub>                                      | Input Data Pad to Y                |            | 4.2  |             | 4.9  | ns    |
| t <sub>ICKY</sub>                                     | Input Reg IOCLK Pad to Y           |            | 7.0  |             | 8.2  | ns    |
| t <sub>OCKY</sub>                                     | Output Reg IOCLK Pad to Y          |            | 7.0  |             | 8.2  | ns    |
| t <sub>ICLRY</sub>                                    | Input Asynchronous Clear to Y      |            | 7.0  |             | 8.2  | ns    |
| t <sub>OCLRY</sub>                                    | Output Asynchronous Clear to Y     |            | 7.0  |             | 8.2  | ns    |
| Input Module Predicted Routing Delays <sup>2, 3</sup> |                                    |            |      |             |      |       |
| t <sub>IRD1</sub>                                     | FO=1 Routing Delay                 |            | 1.3  |             | 1.5  | ns    |
| t <sub>IRD2</sub>                                     | FO=2 Routing Delay                 |            | 1.9  |             | 2.1  | ns    |
| t <sub>IRD3</sub>                                     | FO=3 Routing Delay                 |            | 2.1  |             | 2.5  | ns    |
| t <sub>IRD4</sub>                                     | FO=4 Routing Delay                 |            | 2.6  |             | 2.9  | ns    |
| t <sub>IRD8</sub>                                     | FO=8 Routing Delay                 |            | 4.2  |             | 4.9  | ns    |

### Notes:

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Optimization techniques may further reduce delays by 0 to 4 ns.

**A1460A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                             |                                                | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|---------------------------------------------|------------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                   | Description                                    | Min.       | Max. | Min.        | Max. | Units |
| <b>I/O Module Sequential Timing</b>         |                                                |            |      |             |      |       |
| $t_{INH}$                                   | Input F-F Data Hold<br>(w.r.t. IOCLK Pad)      | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$                                  | Input F-F Data Setup<br>(w.r.t. IOCLK Pad)     | 2.1        |      | 2.4         |      | ns    |
| $t_{IDEH}$                                  | Input Data Enable Hold<br>(w.r.t. IOCLK Pad)   | 0.0        |      | 0.0         |      | ns    |
| $t_{IDESU}$                                 | Input Data Enable Setup<br>(w.r.t. IOCLK Pad)  | 8.7        |      | 10.0        |      | ns    |
| $t_{OUTH}$                                  | Output F-F Data Hold<br>(w.r.t. IOCLK Pad)     | 1.1        |      | 1.2         |      | ns    |
| $t_{OUTSU}$                                 | Output F-F Data Setup<br>(w.r.t. IOCLK Pad)    | 1.1        |      | 1.2         |      | ns    |
| $t_{ODEH}$                                  | Output Data Enable Hold<br>(w.r.t. IOCLK Pad)  | 0.5        |      | 0.6         |      | ns    |
| $t_{ODESU}$                                 | Output Data Enable Setup<br>(w.r.t. IOCLK Pad) | 2.0        |      | 2.4         |      | ns    |
| <b>TTL Output Module Timing<sup>1</sup></b> |                                                |            |      |             |      |       |
| $t_{DHS}$                                   | Data to Pad, High Slew                         |            | 7.5  |             | 8.9  | ns    |
| $t_{DLS}$                                   | Data to Pad, Low Slew                          |            | 11.9 |             | 14.0 | ns    |
| $t_{ENZHS}$                                 | Enable to Pad, Z to H/L, High Slew             |            | 6.0  |             | 7.0  | ns    |
| $t_{ENZLS}$                                 | Enable to Pad, Z to H/L, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| $t_{ENHSZ}$                                 | Enable to Pad, H/L to Z, High Slew             |            | 11.5 |             | 13.5 | ns    |
| $t_{ENLSZ}$                                 | Enable to Pad, H/L to Z, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| $t_{CKHS}$                                  | IOCLK Pad to Pad H/L, High Slew                |            | 11.6 |             | 13.4 | ns    |
| $t_{CKLS}$                                  | IOCLK Pad to Pad H/L, Low Slew                 |            | 17.8 |             | 19.8 | ns    |
| $d_{TLHHS}$                                 | Delta Low to High, High Slew                   |            | 0.04 |             | 0.04 | ns/pF |
| $d_{TLHLS}$                                 | Delta Low to High, Low Slew                    |            | 0.07 |             | 0.08 | ns/pF |
| $d_{THLHS}$                                 | Delta High to Low, High Slew                   |            | 0.05 |             | 0.06 | ns/pF |
| $d_{THLLS}$                                 | Delta High to Low, Low Slew                    |            | 0.07 |             | 0.08 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

## A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                            |                                                | ‘–1’ Speed |      | ‘Std’ Speed |      |       |
|--------------------------------------------|------------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                  | Description                                    | Min.       | Max. | Min.        | Max. | Units |
| CMOS Output Module Timing <sup>1</sup>     |                                                |            |      |             |      |       |
| t <sub>DHS</sub>                           | Data to Pad, High Slew                         |            | 9.2  |             | 10.8 | ns    |
| t <sub>DLS</sub>                           | Data to Pad, Low Slew                          |            | 17.3 |             | 20.3 | ns    |
| t <sub>ENZHS</sub>                         | Enable to Pad, Z to H/L, High Slew             |            | 7.7  |             | 9.1  | ns    |
| t <sub>ENZLS</sub>                         | Enable to Pad, Z to H/L, Low Slew              |            | 13.1 |             | 15.5 | ns    |
| t <sub>ENHSZ</sub>                         | Enable to Pad, H/L to Z, High Slew             |            | 10.9 |             | 12.8 | ns    |
| t <sub>ENLSZ</sub>                         | Enable to Pad, H/L to Z, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| t <sub>CKHS</sub>                          | IOCLK Pad to Pad H/L, High Slew                |            | 14.1 |             | 16.0 | ns    |
| t <sub>CKLS</sub>                          | IOCLK Pad to Pad H/L, Low Slew                 |            | 20.2 |             | 22.4 | ns    |
| d <sub>TLHHS</sub>                         | Delta Low to High, High Slew                   |            | 0.06 |             | 0.07 | ns/pF |
| d <sub>TLHLS</sub>                         | Delta Low to High, Low Slew                    |            | 0.11 |             | 0.13 | ns/pF |
| d <sub>THLHS</sub>                         | Delta High to Low, High Slew                   |            | 0.04 |             | 0.05 | ns/pF |
| d <sub>THLLS</sub>                         | Delta High to Low, Low Slew                    |            | 0.05 |             | 0.06 | ns/pF |
| Dedicated (Hard-Wired) I/O Clock Network   |                                                |            |      |             |      |       |
| t <sub>IOCKH</sub>                         | Input Low to High<br>(Pad to I/O Module Input) |            | 3.5  |             | 4.1  | ns    |
| t <sub>IOPWH</sub>                         | Minimum Pulse Width High                       | 4.8        |      | 5.7         |      | ns    |
| t <sub>IOPWL</sub>                         | Minimum Pulse Width Low                        | 4.8        |      | 5.7         |      | ns    |
| t <sub>IOSAPW</sub>                        | Minimum Asynchronous Pulse Width               | 3.9        |      | 4.4         |      | ns    |
| t <sub>IOCKSW</sub>                        | Maximum Skew                                   |            | 0.9  |             | 1.0  | ns    |
| t <sub>IOP</sub>                           | Minimum Period                                 | 9.9        |      | 11.6        |      | ns    |
| f <sub>IOMAX</sub>                         | Maximum Frequency                              |            | 100  |             | 85   | MHz   |
| Dedicated (Hard-Wired) Array Clock Network |                                                |            |      |             |      |       |
| t <sub>HCKH</sub>                          | Input Low to High<br>(Pad to S-Module Input)   |            | 5.5  |             | 6.4  | ns    |
| t <sub>HCKL</sub>                          | Input High to Low<br>(Pad to S-Module Input)   |            | 5.5  |             | 6.4  | ns    |
| t <sub>HPWH</sub>                          | Minimum Pulse Width High                       | 4.8        |      | 5.7         |      | ns    |
| t <sub>HPWL</sub>                          | Minimum Pulse Width Low                        | 4.8        |      | 5.7         |      | ns    |
| t <sub>HCKSW</sub>                         | Maximum Skew                                   |            | 0.9  |             | 1.0  | ns    |
| t <sub>HP</sub>                            | Minimum Period                                 | 9.9        |      | 11.6        |      | ns    |
| f <sub>HMAX</sub>                          | Maximum Frequency                              |            | 100  |             | 85   | MHz   |

### Notes:

1. Delays based on 35 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

**A1460A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                    |                                | '-1' Speed |      | 'Std' Speed |      |       |
|------------------------------------|--------------------------------|------------|------|-------------|------|-------|
| Parameter                          | Description                    | Min.       | Max. | Min.        | Max. | Units |
| <b>Routed Array Clock Networks</b> |                                |            |      |             |      |       |
| $t_{RCKH}$                         | Input Low to High (FO=256)     |            | 9.0  |             | 10.5 | ns    |
| $t_{RCKL}$                         | Input High to Low (FO=256)     |            | 9.0  |             | 10.5 | ns    |
| $t_{RPWH}$                         | Min. Pulse Width High (FO=256) | 6.3        |      | 7.1         |      | ns    |
| $t_{RPWL}$                         | Min. Pulse Width Low (FO=256)  | 6.3        |      | 7.1         |      | ns    |
| $t_{RCKSW}$                        | Maximum Skew (FO=128)          |            | 1.9  |             | 2.1  | ns    |
| $t_{RP}$                           | Minimum Period (FO=256)        | 12.9       |      | 14.5        |      | ns    |
| $f_{RMAX}$                         | Maximum Frequency (FO=256)     |            | 75   |             | 65   | MHz   |
| <b>Clock-to-Clock Skews</b>        |                                |            |      |             |      |       |
| $t_{IOHCKSW}$                      | I/O Clock to H-Clock Skew      | 0.0        | 3.0  | 0.0         | 3.0  | ns    |
| $t_{IORCKSW}$                      | I/O Clock to R-Clock Skew      | 0.0        | 5.0  | 0.0         | 5.0  | ns    |
| $t_{HRCKSW}$                       | H-Clock to R-Clock Skew        |            |      |             |      |       |
|                                    | (FO = 64)                      | 0.0        | 1.0  | 0.0         | 1.0  | ns    |
|                                    | (FO = 50% max.)                | 0.0        | 3.0  | 0.0         | 3.0  | ns    |

## A14100A Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                             |                                    | '-1' Speed |      | 'Std' Speed |      |       |
|-------------------------------------------------------------|------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                   | Description                        | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>          |                                    |            |      |             |      |       |
| $t_{PD}$                                                    | Internal Array Module              |            | 3.0  |             | 3.5  | ns    |
| $t_{CO}$                                                    | Sequential Clock to Q              |            | 3.0  |             | 3.5  | ns    |
| $t_{CLR}$                                                   | Asynchronous Clear to Q            |            | 3.0  |             | 3.5  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b>    |                                    |            |      |             |      |       |
| $t_{RD1}$                                                   | FO=1 Routing Delay                 |            | 1.3  |             | 1.5  | ns    |
| $t_{RD2}$                                                   | FO=2 Routing Delay                 |            | 1.9  |             | 2.1  | ns    |
| $t_{RD3}$                                                   | FO=3 Routing Delay                 |            | 2.1  |             | 2.5  | ns    |
| $t_{RD4}$                                                   | FO=4 Routing Delay                 |            | 2.6  |             | 2.9  | ns    |
| $t_{RD8}$                                                   | FO=8 Routing Delay                 |            | 4.2  |             | 4.9  | ns    |
| <b>Logic Module Sequential Timing</b>                       |                                    |            |      |             |      |       |
| $t_{SUD}$                                                   | Flip-Flop (Latch) Data Input Setup | 1.0        |      | 1.0         |      | ns    |
| $t_{HD}$                                                    | Flip-Flop (Latch) Data Input Hold  | 0.6        |      | 0.6         |      | ns    |
| $t_{SUENA}$                                                 | Flip-Flop (Latch) Enable Setup     | 1.0        |      | 1.0         |      | ns    |
| $t_{HENA}$                                                  | Flip-Flop (Latch) Enable Hold      | 0.6        |      | 0.6         |      | ns    |
| $t_{WASYN}$                                                 | Asynchronous Pulse Width           | 4.8        |      | 5.6         |      | ns    |
| $t_{WCLKA}$                                                 | Flip-Flop Clock Pulse Width        | 4.8        |      | 5.6         |      | ns    |
| $t_A$                                                       | Flip-Flop Clock Input Period       | 9.9        |      | 11.6        |      | ns    |
| $f_{MAX}$                                                   | Flip-Flop Clock Frequency          |            | 100  |             | 85   | MHz   |
| <b>Input Module Propagation Delays</b>                      |                                    |            |      |             |      |       |
| $t_{INY}$                                                   | Input Data Pad to Y                |            | 4.2  |             | 4.9  | ns    |
| $t_{ICKY}$                                                  | Input Reg IOCLK Pad to Y           |            | 7.0  |             | 8.2  | ns    |
| $t_{OCKY}$                                                  | Output Reg IOCLK Pad to Y          |            | 7.0  |             | 8.2  | ns    |
| $t_{ICLRY}$                                                 | Input Asynchronous Clear to Y      |            | 7.0  |             | 8.2  | ns    |
| $t_{OCLRY}$                                                 | Output Asynchronous Clear to Y     |            | 7.0  |             | 8.2  | ns    |
| <b>Input Module Predicted Routing Delays<sup>2, 3</sup></b> |                                    |            |      |             |      |       |
| $t_{IRD1}$                                                  | FO=1 Routing Delay                 |            | 1.3  |             | 1.5  | ns    |
| $t_{IRD2}$                                                  | FO=2 Routing Delay                 |            | 1.9  |             | 2.1  | ns    |
| $t_{IRD3}$                                                  | FO=3 Routing Delay                 |            | 2.1  |             | 2.5  | ns    |
| $t_{IRD4}$                                                  | FO=4 Routing Delay                 |            | 2.6  |             | 2.9  | ns    |
| $t_{IRD8}$                                                  | FO=8 Routing Delay                 |            | 4.2  |             | 4.9  | ns    |

### Notes:

1. For dual-module macros, use  $t_{PD} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Optimization techniques may further reduce delays by 0 to 4 ns.

**A14100A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                             |                                                | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|---------------------------------------------|------------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                   | Description                                    | Min.       | Max. | Min.        | Max. | Units |
| <b>I/O Module Sequential Timing</b>         |                                                |            |      |             |      |       |
| $t_{INH}$                                   | Input F-F Data Hold<br>(w.r.t. IOCLK Pad)      | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$                                  | Input F-F Data Setup<br>(w.r.t. IOCLK Pad)     | 2.1        |      | 2.4         |      | ns    |
| $t_{IDEH}$                                  | Input Data Enable Hold<br>(w.r.t. IOCLK Pad)   | 0.0        |      | 0.0         |      | ns    |
| $t_{IDESU}$                                 | Input Data Enable Setup<br>(w.r.t. IOCLK Pad)  | 8.7        |      | 10.0        |      | ns    |
| $t_{OUTH}$                                  | Output F-F Data Hold<br>(w.r.t. IOCLK Pad)     | 1.2        |      | 1.2         |      | ns    |
| $t_{OUTSU}$                                 | Output F-F Data Setup<br>(w.r.t. IOCLK Pad)    | 1.2        |      | 1.2         |      | ns    |
| $t_{ODEH}$                                  | Output Data Enable Hold<br>(w.r.t. IOCLK Pad)  | 0.6        |      | 0.6         |      | ns    |
| $t_{ODESU}$                                 | Output Data Enable Setup<br>(w.r.t. IOCLK Pad) | 2.4        |      | 2.4         |      | ns    |
| <b>TTL Output Module Timing<sup>1</sup></b> |                                                |            |      |             |      |       |
| $t_{DHS}$                                   | Data to Pad, High Slew                         |            | 7.5  |             | 8.9  | ns    |
| $t_{DLS}$                                   | Data to Pad, Low Slew                          |            | 11.9 |             | 14.0 | ns    |
| $t_{ENZHS}$                                 | Enable to Pad, Z to H/L, High Slew             |            | 6.0  |             | 7.0  | ns    |
| $t_{ENZLS}$                                 | Enable to Pad, Z to H/L, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| $t_{ENHSZ}$                                 | Enable to Pad, H/L to Z, High Slew             |            | 11.9 |             | 14.0 | ns    |
| $t_{ENLSZ}$                                 | Enable to Pad, H/L to Z, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| $t_{CKHS}$                                  | IOCLK Pad to Pad H/L, High Slew                |            | 12.2 |             | 14.0 | ns    |
| $t_{CKLS}$                                  | IOCLK Pad to Pad H/L, Low Slew                 |            | 17.8 |             | 17.8 | ns    |
| $d_{TLHHS}$                                 | Delta Low to High, High Slew                   |            | 0.04 |             | 0.04 | ns/pF |
| $d_{TLHLS}$                                 | Delta Low to High, Low Slew                    |            | 0.07 |             | 0.08 | ns/pF |
| $d_{THLHS}$                                 | Delta High to Low, High Slew                   |            | 0.05 |             | 0.06 | ns/pF |
| $d_{THLLS}$                                 | Delta High to Low, Low Slew                    |            | 0.07 |             | 0.08 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

## A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                   |                                                | '-1' Speed |      | 'Std' Speed |      |       |
|---------------------------------------------------|------------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                         | Description                                    | Min.       | Max. | Min.        | Max. | Units |
| <b>CMOS Output Module Timing<sup>1</sup></b>      |                                                |            |      |             |      |       |
| $t_{DHS}$                                         | Data to Pad, High Slew                         |            | 9.2  |             | 10.8 | ns    |
| $t_{DLS}$                                         | Data to Pad, Low Slew                          |            | 17.3 |             | 20.3 | ns    |
| $t_{ENZHS}$                                       | Enable to Pad, Z to H/L, High Slew             |            | 7.7  |             | 9.1  | ns    |
| $t_{ENZLS}$                                       | Enable to Pad, Z to H/L, Low Slew              |            | 13.1 |             | 15.5 | ns    |
| $t_{ENHSZ}$                                       | Enable to Pad, H/L to Z, High Slew             |            | 11.6 |             | 14.0 | ns    |
| $t_{ENLSZ}$                                       | Enable to Pad, H/L to Z, Low Slew              |            | 10.9 |             | 12.8 | ns    |
| $t_{CKHS}$                                        | IOCLK Pad to Pad H/L, High Slew                |            | 14.4 |             | 16.0 | ns    |
| $t_{CKLS}$                                        | IOCLK Pad to Pad H/L, Low Slew                 |            | 20.2 |             | 22.4 | ns    |
| $d_{TLHHS}$                                       | Delta Low to High, High Slew                   |            | 0.06 |             | 0.07 | ns/pF |
| $d_{TLHLS}$                                       | Delta Low to High, Low Slew                    |            | 0.11 |             | 0.13 | ns/pF |
| $d_{THLHS}$                                       | Delta High to Low, High Slew                   |            | 0.04 |             | 0.05 | ns/pF |
| $d_{THLLS}$                                       | Delta High to Low, Low Slew                    |            | 0.05 |             | 0.06 | ns/pF |
| <b>Dedicated (Hard-Wired) I/O Clock Network</b>   |                                                |            |      |             |      |       |
| $t_{IOCKH}$                                       | Input Low to High<br>(Pad to I/O Module Input) |            | 3.5  |             | 4.1  | ns    |
| $t_{IOPWH}$                                       | Minimum Pulse Width High                       | 4.8        |      | 5.7         |      | ns    |
| $t_{IOPWL}$                                       | Minimum Pulse Width Low                        | 4.8        |      | 5.7         |      | ns    |
| $t_{IOSAPW}$                                      | Minimum Asynchronous Pulse Width               | 3.9        |      | 4.4         |      | ns    |
| $t_{IOCKSW}$                                      | Maximum Skew                                   |            | 0.9  |             | 1.0  | ns    |
| $t_{IOP}$                                         | Minimum Period                                 | 9.9        |      | 11.6        |      | ns    |
| $f_{IOMAX}$                                       | Maximum Frequency                              |            | 100  |             | 85   | MHz   |
| <b>Dedicated (Hard-Wired) Array Clock Network</b> |                                                |            |      |             |      |       |
| $t_{HCKH}$                                        | Input Low to High<br>(Pad to S-Module Input)   |            | 5.5  |             | 6.4  | ns    |
| $t_{HCKL}$                                        | Input High to Low<br>(Pad to S-Module Input)   |            | 5.5  |             | 6.4  | ns    |
| $t_{HPWH}$                                        | Minimum Pulse Width High                       | 4.8        |      | 5.7         |      | ns    |
| $t_{HPWL}$                                        | Minimum Pulse Width Low                        | 4.8        |      | 5.7         |      | ns    |
| $t_{HCKSW}$                                       | Maximum Skew                                   |            | 0.9  |             | 1.0  | ns    |
| $t_{HP}$                                          | Minimum Period                                 | 9.9        |      | 11.6        |      | ns    |
| $f_{HMAX}$                                        | Maximum Frequency                              |            | 100  |             | 85   | MHz   |

**Notes:**

1. Delays based on 35 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

**A14100A Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                    |                                | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|------------------------------------|--------------------------------|------------|------|-------------|------|-------|
| Parameter                          | Description                    | Min.       | Max. | Min.        | Max. | Units |
| <b>Routed Array Clock Networks</b> |                                |            |      |             |      |       |
| $t_{RCKH}$                         | Input Low to High (FO=256)     |            | 9.0  |             | 10.5 | ns    |
| $t_{RCKL}$                         | Input High to Low (FO=256)     |            | 9.0  |             | 10.5 | ns    |
| $t_{RPWH}$                         | Min. Pulse Width High (FO=256) | 6.3        |      | 7.1         |      | ns    |
| $t_{RPWL}$                         | Min. Pulse Width Low (FO=256)  | 6.3        |      | 7.1         |      | ns    |
| $t_{RCKSW}$                        | Maximum Skew (FO=128)          |            | 1.9  |             | 2.1  | ns    |
| $t_{RP}$                           | Minimum Period (FO=256)        | 12.9       |      | 14.5        |      | ns    |
| $f_{RMAX}$                         | Maximum Frequency (FO=256)     |            | 75   |             | 65   | MHz   |
| <b>Clock-to-Clock Skews</b>        |                                |            |      |             |      |       |
| $t_{IOHCKSW}$                      | I/O Clock to H-Clock Skew      | 0.0        | 3.5  | 0.0         | 3.5  | ns    |
| $t_{IORCKSW}$                      | I/O Clock to R-Clock Skew      | 0.0        | 5.0  | 0.0         | 5.0  | ns    |
| $t_{HRCKSW}$                       | H-Clock to R-Clock Skew        |            |      |             |      |       |
|                                    | (FO = 64)                      | 0.0        | 1.0  | 0.0         | 1.0  | ns    |
|                                    | (FO = 50% max.)                | 0.0        | 3.0  | 0.0         | 3.0  |       |

## A32100DX Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                                            | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|--------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                | Description                                | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Combinatorial Functions</b>              |                                            |            |      |             |      |       |
| $t_{PD}$                                                 | Internal Array Module Delay                |            | 3.1  |             | 4.1  | ns    |
| $t_{PDD}$                                                | Internal Decode Module Delay               |            | 3.3  |             | 4.3  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b> |                                            |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay                         |            | 1.3  |             | 1.8  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay                         |            | 1.9  |             | 2.6  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay                         |            | 2.6  |             | 3.4  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay                         |            | 3.3  |             | 4.3  | ns    |
| $t_{RD5}$                                                | FO=8 Routing Delay                         |            | 0.6  |             | 0.8  | ns    |
| $t_{RDD}$                                                | Decode-to-Output Routing Delay             |            | 0.5  |             | 0.6  | ns    |
| <b>Logic Module Sequential Timing</b>                    |                                            |            |      |             |      |       |
| $t_{CO}$                                                 | Flip-Flop Clock-to-Output                  |            | 3.1  |             | 4.1  | ns    |
| $t_{GO}$                                                 | Latch Gate-to-Output                       |            | 3.1  |             | 4.1  | ns    |
| $t_{SU}$                                                 | Flip-Flop (Latch) Setup Time               | 0.5        |      | 0.6         |      | ns    |
| $t_H$                                                    | Flip-Flop (Latch) Hold Time                | 0.0        |      | 0.0         |      | ns    |
| $t_{RO}$                                                 | Flip-Flop (Latch) Reset to Output          |            | 3.1  |             | 4.1  | ns    |
| $t_{SUENA}$                                              | Flip-Flop (Latch) Enable Setup             | 0.9        |      | 1.2         |      | ns    |
| $t_{HENA}$                                               | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$                                              | Flip-Flop (Latch) Clock Active Pulse Width | 4.3        |      | 5.8         |      | ns    |
| $t_{WASYN}$                                              | Flip-Flop (Latch) Asynchronous Pulse Width | 5.6        |      | 7.5         |      | ns    |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**A32100DX Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                     |                                    | '-1' Speed |      | 'Std' Speed |      |       |
|-------------------------------------|------------------------------------|------------|------|-------------|------|-------|
| Parameter                           | Description                        | Min.       | Max. | Min.        | Max. | Units |
| <b>Synchronous SRAM Operations</b>  |                                    |            |      |             |      |       |
| $t_{RC}$                            | Read Cycle Time                    | 8.8        |      | 11.8        |      | ns    |
| $t_{WC}$                            | Write Cycle Time                   | 8.8        |      | 11.8        |      | ns    |
| $t_{RCKHL}$                         | Clock High/Low Time                | 4.4        |      | 5.9         |      | ns    |
| $t_{RCO}$                           | Data Valid After Clock High/Low    |            | 4.4  |             | 5.9  | ns    |
| $t_{ADSU}$                          | Address/Data Setup Time            | 2.1        |      | 2.8         |      | ns    |
| $t_{ADH}$                           | Address/Data Hold Time             | 0.0        |      | 0.0         |      | ns    |
| $t_{RENSU}$                         | Read Enable Setup                  | 0.8        |      | 1.1         |      | ns    |
| $t_{RENH}$                          | Read Enable Hold                   | 4.4        |      | 5.9         |      | ns    |
| $t_{WENSU}$                         | Write Enable Setup                 | 3.5        |      | 4.7         |      | ns    |
| $t_{WENH}$                          | Write Enable Hold                  | 0.0        |      | 0.0         |      | ns    |
| $t_{BENS}$                          | Block Enable Setup                 | 3.6        |      | 4.8         |      | ns    |
| $t_{BENH}$                          | Block Enable Hold                  | 0.0        |      | 0.0         |      | ns    |
| <b>Asynchronous SRAM Operations</b> |                                    |            |      |             |      |       |
| $t_{RPD}$                           | Asynchronous Access Time           |            | 10.6 |             | 14.1 | ns    |
| $t_{RDADV}$                         | Read Address Valid                 | 11.5       |      | 15.3        |      | ns    |
| $t_{ADSU}$                          | Address/Data Setup Time            | 2.1        |      | 2.8         |      | ns    |
| $t_{ADH}$                           | Address/Data Hold Time             | 0.0        |      | 0.0         |      | ns    |
| $t_{RENSUA}$                        | Read Enable Setup to Address Valid | 0.8        |      | 1.1         |      | ns    |
| $t_{RENHA}$                         | Read Enable Hold                   | 4.4        |      | 5.9         |      | ns    |
| $t_{WENSU}$                         | Write Enable Setup                 | 3.5        |      | 4.7         |      | ns    |
| $t_{WENH}$                          | Write Enable Hold                  | 0.0        |      | 0.0         |      | ns    |
| $t_{DOH}$                           | Data Out Hold Time                 |            | 1.6  |             | 2.1  | ns    |

## A32100DX Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                            |        | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|----------------------------|--------|------------|------|-------------|------|-------|
| Parameter                                                | Description                |        | Min.       | Max. | Min.        | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                            |        |            |      |             |      |       |
| $t_{INPY}$                                               | Input Data Pad to Y        |        |            | 1.9  |             | 2.6  | ns    |
| $t_{INGO}$                                               | Input Latch Gate-to-Output |        |            | 4.0  |             | 5.3  | ns    |
| $t_{INH}$                                                | Input Latch Hold           |        | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$                                               | Input Latch Setup          |        | 0.7        |      | 0.9         |      | ns    |
| $t_{ILA}$                                                | Latch Active Pulse Width   |        | 6.1        |      | 8.1         |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                            |        |            |      |             |      |       |
| $t_{IRD1}$                                               | FO=1 Routing Delay         |        |            | 2.2  |             | 2.9  | ns    |
| $t_{IRD2}$                                               | FO=2 Routing Delay         |        |            | 2.8  |             | 3.8  | ns    |
| $t_{IRD3}$                                               | FO=3 Routing Delay         |        |            | 3.5  |             | 4.7  | ns    |
| $t_{IRD4}$                                               | FO=4 Routing Delay         |        |            | 3.5  |             | 4.7  | ns    |
| $t_{IRD8}$                                               | FO=8 Routing Delay         |        |            | 5.6  |             | 7.5  | ns    |
| <b>Global Clock Network</b>                              |                            |        |            |      |             |      |       |
| $t_{CKH}$                                                | Input Low to High          | FO=32  |            | 6.5  |             | 8.7  | ns    |
|                                                          |                            | FO=635 |            | 7.9  |             | 10.6 | ns    |
| $t_{CKL}$                                                | Input High to Low          | FO=32  |            | 6.6  |             | 8.8  | ns    |
|                                                          |                            | FO=635 |            | 8.8  |             | 11.8 | ns    |
| $t_{PWH}$                                                | Minimum Pulse Width High   | FO=32  | 4.1        |      | 5.5         |      | ns    |
|                                                          |                            | FO=635 | 4.6        |      | 6.1         |      | ns    |
| $t_{PWL}$                                                | Minimum Pulse Width Low    | FO=32  | 4.1        |      | 5.5         |      | ns    |
|                                                          |                            | FO=635 | 4.6        |      | 6.1         |      | ns    |
| $t_{CKSW}$                                               | Maximum Skew               | FO=32  |            | 1.8  |             | 2.4  | ns    |
|                                                          |                            | FO=635 |            | 1.8  |             | 2.4  | ns    |
| $t_{SUEXT}$                                              | Input Latch External Setup | FO=32  | 0.0        |      | 0.0         |      | ns    |
|                                                          |                            | FO=635 | 0.0        |      | 0.0         |      | ns    |
| $t_{HEXT}$                                               | Input Latch External Hold  | FO=32  | 3.0        |      | 4.0         |      | ns    |
|                                                          |                            | FO=635 | 3.8        |      | 5.1         |      | ns    |
| $t_P$                                                    | Minimum Period (1/fmax)    | FO=32  | 7.1        |      | 9.5         |      | ns    |
|                                                          |                            | FO=635 | 7.9        |      | 10.5        |      | ns    |
| $f_{HMAX}$                                               | Maximum Datapath Frequency | FO=32  |            | 140  |             | 105  | MHz   |
|                                                          |                            | FO=635 |            | 126  |             | 95   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

**A32100DX Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                              |                                           | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------|-------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                    | Description                               | Min.       | Max. | Min.        | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                                           |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High                          |            | 5.1  |             | 6.8  | ns    |
| $t_{DHL}$                                    | Data to Pad Low                           |            | 6.3  |             | 8.3  | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High                      |            | 6.6  |             | 8.8  | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low                       |            | 7.1  |             | 9.4  | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z                      |            | 11.5 |             | 15.3 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z                       |            | 11.5 |             | 15.3 | ns    |
| $t_{GLH}$                                    | G to Pad High                             |            | 11.5 |             | 15.3 | ns    |
| $t_{GHL}$                                    | G to Pad Low                              |            | 12.4 |             | 16.6 | ns    |
| $t_{LSU}$                                    | I/O Latch Output Setup                    | 0.4        |      | 0.5         |      | ns    |
| $t_{LH}$                                     | I/O Latch Output Hold                     | 0.0        |      | 0.0         |      | ns    |
| $t_{LCO}$                                    | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O   |            | 11.5 |             | 15.4 | ns    |
| $t_{ACO}$                                    | Array Latch Clock-Out (Pad-to-Pad) 32 I/O |            | 16.3 |             | 21.7 | ns    |
| $d_{TLH}$                                    | Capacitive Loading, Low to High           |            | 0.04 |             | 0.06 | ns/pF |
| $d_{THL}$                                    | Capacitive Loading, High to Low           |            | 0.06 |             | 0.08 | ns/pF |
| $t_{WDO}$                                    | Hard-Wired Wide Decode Output             |            | 0.05 |             | 0.07 | ns    |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                                           |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High                          |            | 6.3  |             | 8.3  | ns    |
| $t_{DHL}$                                    | Data to Pad Low                           |            | 5.1  |             | 6.8  | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High                      |            | 6.6  |             | 8.8  | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low                       |            | 7.1  |             | 9.4  | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z                      |            | 11.5 |             | 15.3 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z                       |            | 11.5 |             | 15.3 | ns    |
| $t_{GLH}$                                    | G to Pad High                             |            | 11.5 |             | 15.3 | ns    |
| $t_{GHL}$                                    | G to Pad Low                              |            | 12.4 |             | 16.6 | ns    |
| $t_{LSU}$                                    | I/O Latch Setup                           | 0.4        |      | 0.5         |      | ns    |
| $t_{LH}$                                     | I/O Latch Hold                            | 0.0        |      | 0.0         |      | ns    |
| $t_{LCO}$                                    | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O   |            | 13.7 |             | 18.2 | ns    |
| $t_{ACO}$                                    | Array Latch Clock-Out (Pad-to-Pad) 32 I/O |            | 19.2 |             | 25.6 | ns    |
| $d_{TLH}$                                    | Capacitive Loading, Low to High           |            | 0.06 |             | 0.08 | ns/pF |
| $d_{THL}$                                    | Capacitive Loading, High to Low           |            | 0.05 |             | 0.07 | ns/pF |
| $t_{WDO}$                                    | Hard-Wired Wide Decode Output             |            | 0.05 |             | 0.07 | ns    |

**Notes:**

1. Delays based on 35 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

## A32200DX Timing Characteristics

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                                            | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|--------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                                | Description                                | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Combinatorial Functions</b>              |                                            |            |      |             |      |       |
| $t_{PD}$                                                 | Internal Array Module Delay                |            | 2.8  |             | 3.8  | ns    |
| $t_{PDD}$                                                | Internal Decode Module Delay               |            | 3.4  |             | 4.6  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b> |                                            |            |      |             |      |       |
| $t_{RD1}$                                                | FO=1 Routing Delay                         |            | 1.6  |             | 2.1  | ns    |
| $t_{RD2}$                                                | FO=2 Routing Delay                         |            | 2.3  |             | 3.1  | ns    |
| $t_{RD3}$                                                | FO=3 Routing Delay                         |            | 2.9  |             | 3.9  | ns    |
| $t_{RD4}$                                                | FO=4 Routing Delay                         |            | 3.5  |             | 4.7  | ns    |
| $t_{RD5}$                                                | FO=8 Routing Delay                         |            | 6.2  |             | 8.2  | ns    |
| $t_{RDD}$                                                | Decode-to-Output Routing Delay             |            | 0.8  |             | 1.1  | ns    |
| <b>Logic Module Sequential Timing Characteristics</b>    |                                            |            |      |             |      |       |
| $t_{CO}$                                                 | Flip-Flop Clock-to-Output                  |            | 3.2  |             | 4.2  | ns    |
| $t_{GO}$                                                 | Latch Gate-to-Output                       |            | 2.8  |             | 3.8  | ns    |
| $t_{SU}$                                                 | Flip-Flop (Latch) Setup Time               | 0.5        |      | 0.6         |      | ns    |
| $t_H$                                                    | Flip-Flop (Latch) Hold Time                | 0.0        |      | 0.0         |      | ns    |
| $t_{RO}$                                                 | Flip-Flop (Latch) Reset to Output          |            | 3.2  |             | 4.2  | ns    |
| $t_{SUENA}$                                              | Flip-Flop (Latch) Enable Setup             | 0.9        |      | 1.2         |      | ns    |
| $t_{HENA}$                                               | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$                                              | Flip-Flop (Latch) Clock Active Pulse Width | 4.3        |      | 5.8         |      | ns    |
| $t_{WASYN}$                                              | Flip-Flop (Latch) Asynchronous Pulse Width | 5.7        |      | 7.6         |      | ns    |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**A32200DX Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                     |                                    | ‘-1’ Speed |      | ‘Std’ Speed |      |       |
|-------------------------------------|------------------------------------|------------|------|-------------|------|-------|
| Parameter                           | Description                        | Min.       | Max. | Min.        | Max. | Units |
| <b>Synchronous SRAM Operations</b>  |                                    |            |      |             |      |       |
| $t_{RC}$                            | Read Cycle Time                    | 8.8        |      | 11.8        |      | ns    |
| $t_{WC}$                            | Write Cycle Time                   | 8.8        |      | 11.8        |      | ns    |
| $t_{RCKHL}$                         | Clock High/Low Time                | 4.4        |      | 5.9         |      | ns    |
| $t_{RCO}$                           | Data Valid After Clock High/Low    |            | 4.4  |             | 5.9  | ns    |
| $t_{ADSU}$                          | Address/Data Setup Time            | 2.1        |      | 2.8         |      | ns    |
| $t_{ADH}$                           | Address/Data Hold Time             | 0.0        |      | 0.0         |      | ns    |
| $t_{RENSU}$                         | Read Enable Setup                  | 0.8        |      | 1.1         |      | ns    |
| $t_{RENH}$                          | Read Enable Hold                   | 4.4        |      | 5.9         |      | ns    |
| $t_{WENSU}$                         | Write Enable Setup                 | 3.5        |      | 4.7         |      | ns    |
| $t_{WENH}$                          | Write Enable Hold                  | 0.0        |      | 0.0         |      | ns    |
| $t_{BENS}$                          | Block Enable Setup                 | 3.6        |      | 4.8         |      | ns    |
| $t_{BENH}$                          | Block Enable Hold                  | 0.0        |      | 0.0         |      | ns    |
| <b>Asynchronous SRAM Operations</b> |                                    |            |      |             |      |       |
| $t_{RPD}$                           | Asynchronous Access Time           |            | 10.6 |             | 14.1 | ns    |
| $t_{RDADV}$                         | Read Address Valid                 | 11.5       |      | 15.3        |      | ns    |
| $t_{ADSU}$                          | Address/Data Setup Time            | 2.1        |      | 2.8         |      | ns    |
| $t_{ADH}$                           | Address/Data Hold Time             | 0.0        |      | 0.0         |      | ns    |
| $t_{RENSUA}$                        | Read Enable Setup to Address Valid | 0.8        |      | 1.1         |      | ns    |
| $t_{RENHA}$                         | Read Enable Hold                   | 4.4        |      | 5.9         |      | ns    |
| $t_{WENSU}$                         | Write Enable Setup                 | 3.5        |      | 4.7         |      | ns    |
| $t_{WENH}$                          | Write Enable Hold                  | 0.0        |      | 0.0         |      | ns    |
| $t_{DOH}$                           | Data Out Hold Time                 |            | 1.6  |             | 2.1  | ns    |

## A32200DX Timing Characteristics (continued)

(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )

|                                                          |                            |        | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------------------|----------------------------|--------|------------|------|-------------|------|-------|
| Parameter                                                | Description                |        | Min.       | Max. | Min.        | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                            |        |            |      |             |      |       |
| $t_{INPY}$                                               | Input Data Pad to Y        |        |            | 1.9  |             | 2.6  | ns    |
| $t_{INGO}$                                               | Input Latch Gate-to-Output |        |            | 4.6  |             | 6.0  | ns    |
| $t_{INH}$                                                | Input Latch Hold           |        | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$                                               | Input Latch Setup          |        | 0.7        |      | 0.9         |      | ns    |
| $t_{ILA}$                                                | Latch Active Pulse Width   |        | 6.1        |      | 8.1         |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                            |        |            |      |             |      |       |
| $t_{IRD1}$                                               | FO=1 Routing Delay         |        |            | 2.6  |             | 3.5  | ns    |
| $t_{IRD2}$                                               | FO=2 Routing Delay         |        |            | 3.4  |             | 4.6  | ns    |
| $t_{IRD3}$                                               | FO=3 Routing Delay         |        |            | 4.6  |             | 6.1  | ns    |
| $t_{IRD4}$                                               | FO=4 Routing Delay         |        |            | 5.4  |             | 7.2  | ns    |
| $t_{IRD5}$                                               | FO=8 Routing Delay         |        |            | 7.0  |             | 9.3  | ns    |
| <b>Global Clock Network</b>                              |                            |        |            |      |             |      |       |
| $t_{CKH}$                                                | Input Low to High          | FO=32  |            | 7.3  |             | 9.8  | ns    |
|                                                          |                            | FO=635 |            | 8.5  |             | 11.3 | ns    |
| $t_{CKL}$                                                | Input High to Low          | FO=32  |            | 7.2  |             | 9.6  | ns    |
|                                                          |                            | FO=635 |            | 9.3  |             | 12.5 | ns    |
| $t_{PWH}$                                                | Minimum Pulse Width High   | FO=32  | 3.2        |      | 4.3         |      | ns    |
|                                                          |                            | FO=635 | 3.9        |      | 5.2         |      | ns    |
| $t_{PWL}$                                                | Minimum Pulse Width Low    | FO=32  | 3.2        |      | 4.3         |      | ns    |
|                                                          |                            | FO=635 | 3.9        |      | 5.2         |      | ns    |
| $t_{CKSW}$                                               | Maximum Skew               | FO=32  |            | 1.8  |             | 2.4  | ns    |
|                                                          |                            | FO=635 |            | 1.8  |             | 2.4  | ns    |
| $t_{SUEXT}$                                              | Input Latch External Setup | FO=32  | 0.0        |      | 0.0         |      | ns    |
|                                                          |                            | FO=635 | 0.0        |      | 0.0         |      | ns    |
| $t_{HEXT}$                                               | Input Latch External Hold  | FO=32  | 3.0        |      | 4.0         |      | ns    |
|                                                          |                            | FO=635 | 3.8        |      | 5.1         |      | ns    |
| $t_P$                                                    | Minimum Period (1/fmax)    | FO=32  | 5.8        |      | 7.7         |      | ns    |
|                                                          |                            | FO=635 | 6.8        |      | 9.1         |      | ns    |
| $f_{HMAX}$                                               | Maximum Datapath Frequency | FO=32  |            | 172  |             | 130  | MHz   |
|                                                          |                            | FO=635 |            | 147  |             | 110  | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.

**A32200DX Timing Characteristics (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

|                                              |                                           | '-1' Speed |      | 'Std' Speed |      |       |
|----------------------------------------------|-------------------------------------------|------------|------|-------------|------|-------|
| Parameter                                    | Description                               | Min.       | Max. | Min.        | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                                           |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High                          |            | 5.1  |             | 6.8  | ns    |
| $t_{DHL}$                                    | Data to Pad Low                           |            | 6.3  |             | 8.3  | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High                      |            | 6.6  |             | 8.8  | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low                       |            | 7.1  |             | 9.5  | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z                      |            | 11.5 |             | 15.3 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z                       |            | 11.5 |             | 15.3 | ns    |
| $t_{GLH}$                                    | G to Pad High                             |            | 11.5 |             | 15.3 | ns    |
| $t_{GHL}$                                    | G to Pad Low                              |            | 12.3 |             | 16.5 | ns    |
| $t_{LSU}$                                    | I/O Latch Output Setup                    | 0.4        |      | 0.5         |      | ns    |
| $t_{LH}$                                     | I/O Latch Output Hold                     | 0.0        |      | 0.0         |      | ns    |
| $t_{LCO}$                                    | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O   |            | 11.5 |             | 15.4 | ns    |
| $t_{ACO}$                                    | Array Latch Clock-Out (Pad-to-Pad) 32 I/O |            | 16.3 |             | 21.7 | ns    |
| $d_{TLH}$                                    | Capacitive Loading, Low to High           |            | 0.04 |             | 0.06 | ns/pF |
| $d_{THL}$                                    | Capacitive Loading, High to Low           |            | 0.06 |             | 0.08 | ns/pF |
| $t_{WDO}$                                    | Hard-Wired Wide Decode Output             |            | 0.05 |             | 0.07 | ns    |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                                           |            |      |             |      |       |
| $t_{DLH}$                                    | Data to Pad High                          |            | 5.1  |             | 6.8  | ns    |
| $t_{DHL}$                                    | Data to Pad Low                           |            | 6.3  |             | 8.3  | ns    |
| $t_{ENZH}$                                   | Enable Pad Z to High                      |            | 6.6  |             | 8.8  | ns    |
| $t_{ENZL}$                                   | Enable Pad Z to Low                       |            | 7.1  |             | 9.5  | ns    |
| $t_{ENHZ}$                                   | Enable Pad High to Z                      |            | 11.5 |             | 15.3 | ns    |
| $t_{ENLZ}$                                   | Enable Pad Low to Z                       |            | 11.5 |             | 15.3 | ns    |
| $t_{GLH}$                                    | G to Pad High                             |            | 11.5 |             | 15.3 | ns    |
| $t_{GHL}$                                    | G to Pad Low                              |            | 12.3 |             | 16.5 | ns    |
| $t_{LSU}$                                    | I/O Latch Setup                           | 0.4        |      | 0.5         |      | ns    |
| $t_{LH}$                                     | I/O Latch Hold                            | 0.0        |      | 0.0         |      | ns    |
| $t_{LCO}$                                    | I/O Latch Clock-Out (Pad-to-Pad) 32 I/O   |            | 13.7 |             | 18.2 | ns    |
| $t_{ACO}$                                    | Array Latch Clock-Out (Pad-to-Pad) 32 I/O |            | 19.2 |             | 25.6 | ns    |
| $d_{TLH}$                                    | Capacitive Loading, Low to High           |            | 0.06 |             | 0.08 | ns/pF |
| $d_{THL}$                                    | Capacitive Loading, High to Low           |            | 0.05 |             | 0.07 | ns/pF |
| $t_{WDO}$                                    | Hard-Wired Wide Decode Output             |            | 0.05 |             | 0.07 | ns    |

**Notes:**

1. Delays based on 35 pF loading.
2. SSO information can be found in the Simultaneously Switching Output Limits for Actel FPGAs application note at <http://www.actel.com/appnotes>.

## Pin Description

### **CLK**                      **Clock (Input)**

ACT 1 only. TTL Clock input for global clock distribution network. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **CLKA**                      **Clock A (Input)**

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **CLKB**                      **Clock B (Input)**

ACT 2, 1200XL, 3200DX, and ACT 3 only. TTL Clock input for global clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **DCLK**                      **Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **GND**                      **Ground**

LOW supply voltage.

### **HCLK**                      **Dedicated (Hard-wired) Array Clock (Input)**

ACT 3 only. TTL Clock input for sequential modules. This input is directly wired to each S-module and offers clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

### **I/O**                      **Input/Output (Input, Output)**

I/O pin functions as an input, output, tristate, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. In the ACT 3 and 3200DX families, unused I/Os are automatically tri-stated. With this configuration, the input buffer internal to the I/O module is disabled. In the ACT 1, ACT 2 and 1200XL families, unused I/Os are automatically configured as bi-directional buffers where each buffer is configured as a LOW driver.

### **IOCLK**                      **Dedicated (Hard-wired) I/O Clock (Input)**

ACT 3 only. TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

### **IOPCL**                      **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

ACT 3 only. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

### **MODE**                      **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide debugging capability, the MODE pin should be terminated to GND through a 10 k $\Omega$  resistor so that the MODE pin can be pulled high when required.

### **NC**                      **No Connection**

This pin is not connected to circuitry within the device.

### **PRA, I/O**                      **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **PRB, I/O**                      **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **SDI**                      **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **V<sub>cc</sub>**                      **5.0V Supply Voltage**

HIGH supply voltage.

### **QCLKA/B,C,D** **Quadrant Clock (Input/Output)**

3200DX only. These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

### **TCK**                      **Test Clock**

Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

**TDI                      Test Data In**

Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

**TDO                      Test Data Out**

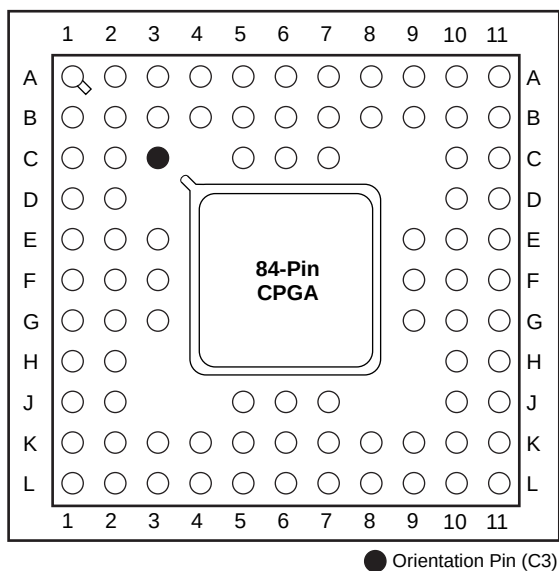
Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

**TMS                      Test Mode Select**

Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed. JTAG pins are only available in the 3200DX device.

## Package Pin Assignments

### 84-Pin CPGA (Top View)



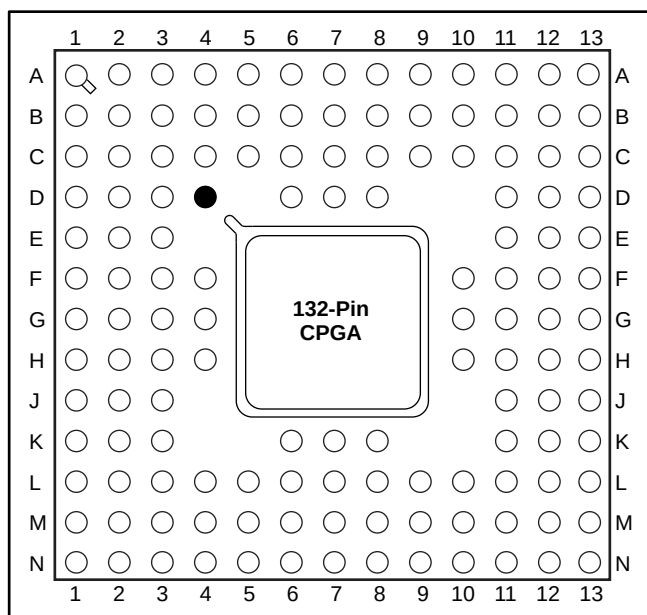
**84-Pin CPGA**

| Pin Number | A1010B<br>Function | A1020B<br>Function |
|------------|--------------------|--------------------|
| A1         | I/O                | I/O                |
| A2         | I/O                | I/O                |
| A3         | I/O                | I/O                |
| A4         | I/O                | I/O                |
| A5         | I/O                | I/O                |
| A6         | I/O                | I/O                |
| A7         | I/O                | I/O                |
| A8         | I/O                | I/O                |
| A9         | I/O                | I/O                |
| A10        | I/O                | I/O                |
| A11        | PRA, I/O           | PRA, I/O           |
| B1         | NC                 | I/O                |
| B2         | NC                 | NC                 |
| B3         | I/O                | I/O                |
| B4         | I/O                | I/O                |
| B5         | V <sub>CC</sub>    | V <sub>CC</sub>    |
| B6         | I/O                | I/O                |
| B7         | GND                | GND                |
| B8         | I/O                | I/O                |
| B9         | I/O                | I/O                |
| B10        | PRB, I/O           | PRB, I/O           |
| B11        | SDI, I/O           | SDI, I/O           |
| C1         | NC                 | I/O                |
| C2         | NC                 | I/O                |
| C5         | I/O                | I/O                |
| C6         | I/O                | I/O                |
| C7         | I/O                | I/O                |
| C10        | DCLK, I/O          | DCLK, I/O          |
| C11        | NC                 | I/O                |
| D1         | I/O                | I/O                |
| D2         | I/O                | I/O                |
| D10        | NC                 | I/O                |
| D11        | NC                 | I/O                |
| E1         | I/O                | I/O                |
| E2         | GND                | GND                |
| E3         | GND                | GND                |
| E9         | V <sub>CC</sub>    | V <sub>CC</sub>    |
| E10        | V <sub>CC</sub>    | V <sub>CC</sub>    |
| E11        | MODE               | MODE               |
| F1         | V <sub>CC</sub>    | V <sub>CC</sub>    |
| F2         | I/O                | I/O                |
| F3         | I/O                | I/O                |

| Pin Number | A1010B<br>Function | A1020B<br>Function |
|------------|--------------------|--------------------|
| F9         | CLK, I/O           | CLK, I/O           |
| F10        | GND                | GND                |
| F11        | I/O                | I/O                |
| G1         | I/O                | I/O                |
| G2         | V <sub>CC</sub>    | V <sub>CC</sub>    |
| G3         | I/O                | I/O                |
| G9         | I/O                | I/O                |
| G10        | GND                | GND                |
| G11        | I/O                | I/O                |
| H1         | I/O                | I/O                |
| H2         | I/O                | I/O                |
| H10        | I/O                | I/O                |
| H11        | I/O                | I/O                |
| J1         | I/O                | I/O                |
| J2         | NC                 | I/O                |
| J5         | I/O                | I/O                |
| J6         | I/O                | I/O                |
| J7         | I/O                | I/O                |
| J10        | NC                 | I/O                |
| J11        | I/O                | I/O                |
| K1         | NC                 | I/O                |
| K2         | V <sub>CC</sub>    | V <sub>CC</sub>    |
| K3         | I/O                | I/O                |
| K4         | I/O                | I/O                |
| K5         | GND                | GND                |
| K6         | I/O                | I/O                |
| K7         | V <sub>CC</sub>    | V <sub>CC</sub>    |
| K8         | I/O                | I/O                |
| K9         | I/O                | I/O                |
| K10        | NC                 | I/O                |
| K11        | NC                 | I/O                |
| L1         | NC                 | I/O                |
| L2         | I/O                | I/O                |
| L3         | I/O                | I/O                |
| L4         | I/O                | I/O                |
| L5         | I/O                | I/O                |
| L6         | I/O                | I/O                |
| L7         | I/O                | I/O                |
| L8         | I/O                | I/O                |
| L9         | I/O                | I/O                |
| L10        | I/O                | I/O                |
| L11        | I/O                | I/O                |

## Package Pin Assignments (continued)

### 132-Pin CPGA (Top View)



● Orientation Pin

**132-Pin CPGA**

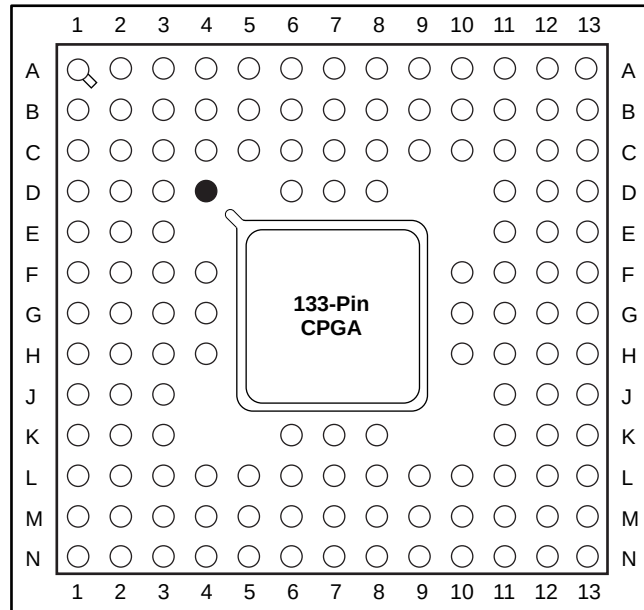
| Pin Number | A1240A Function |
|------------|-----------------|
| A1         | MODE            |
| A2         | I/O             |
| A3         | I/O             |
| A4         | I/O             |
| A5         | I/O             |
| A6         | I/O             |
| A7         | I/O             |
| A8         | I/O             |
| A9         | I/O             |
| A10        | I/O             |
| A11        | I/O             |
| A12        | I/O             |
| A13        | I/O             |
| B1         | I/O             |
| B2         | I/O             |
| B3         | I/O             |
| B4         | I/O             |
| B5         | GND             |
| B6         | CLKB, I/O       |
| B7         | CLKA, I/O       |
| B8         | PRA, I/O        |
| B9         | GND             |
| B10        | I/O             |
| B11        | I/O             |
| B12        | SDI, I/O        |
| B13        | I/O             |
| C1         | I/O             |
| C2         | I/O             |
| C3         | DCLK, I/O       |
| C4         | I/O             |
| C5         | GND             |
| C6         | PRB, I/O        |
| C7         | V <sub>CC</sub> |
| C8         | I/O             |
| C9         | GND             |
| C10        | I/O             |
| C11        | I/O             |
| C12        | I/O             |
| C13        | I/O             |
| D1         | I/O             |
| D2         | I/O             |
| D3         | I/O             |
| D6         | I/O             |
| D7         | V <sub>CC</sub> |

| Pin Number | A1240A Function |
|------------|-----------------|
| D8         | I/O             |
| D11        | I/O             |
| D12        | I/O             |
| D13        | I/O             |
| E1         | I/O             |
| E2         | I/O             |
| E3         | GND             |
| E11        | GND             |
| E12        | GND             |
| E13        | I/O             |
| F1         | I/O             |
| F2         | I/O             |
| F3         | I/O             |
| F4         | GND             |
| F10        | I/O             |
| F11        | I/O             |
| F12        | I/O             |
| F13        | I/O             |
| G1         | I/O             |
| G2         | V <sub>CC</sub> |
| G3         | V <sub>CC</sub> |
| G4         | V <sub>CC</sub> |
| G10        | V <sub>CC</sub> |
| G11        | V <sub>CC</sub> |
| G12        | V <sub>CC</sub> |
| G13        | V <sub>CC</sub> |
| H1         | I/O             |
| H2         | I/O             |
| H3         | I/O             |
| H4         | I/O             |
| H10        | I/O             |
| H11        | I/O             |
| H12        | I/O             |
| H13        | GND             |
| J1         | I/O             |
| J2         | GND             |
| J3         | GND             |
| J11        | GND             |
| J12        | I/O             |
| J13        | I/O             |
| K1         | I/O             |
| K2         | I/O             |
| K3         | I/O             |
| K6         | I/O             |

| Pin Number | A1240A Function |
|------------|-----------------|
| K7         | V <sub>CC</sub> |
| K8         | I/O             |
| K11        | I/O             |
| K12        | GND             |
| K13        | I/O             |
| L1         | I/O             |
| L2         | I/O             |
| L3         | I/O             |
| L4         | I/O             |
| L5         | GND             |
| L6         | I/O             |
| L7         | V <sub>CC</sub> |
| L8         | I/O             |
| L9         | GND             |
| L10        | I/O             |
| L11        | I/O             |
| L12        | I/O             |
| L13        | I/O             |
| M1         | I/O             |
| M2         | I/O             |
| M3         | I/O             |
| M4         | I/O             |
| M5         | I/O             |
| M6         | I/O             |
| M7         | I/O             |
| M8         | I/O             |
| M9         | GND             |
| M10        | I/O             |
| M11        | I/O             |
| M12        | I/O             |
| M13        | I/O             |
| N1         | I/O             |
| N2         | I/O             |
| N3         | I/O             |
| N4         | I/O             |
| N5         | I/O             |
| N6         | I/O             |
| N7         | I/O             |
| N8         | I/O             |
| N9         | I/O             |
| N10        | I/O             |
| N11        | I/O             |
| N12        | I/O             |
| N13        | I/O             |

## Package Pin Assignments (continued)

### 133-Pin CPGA (Top View)



● Orientation Pin

## 133-Pin CPGA

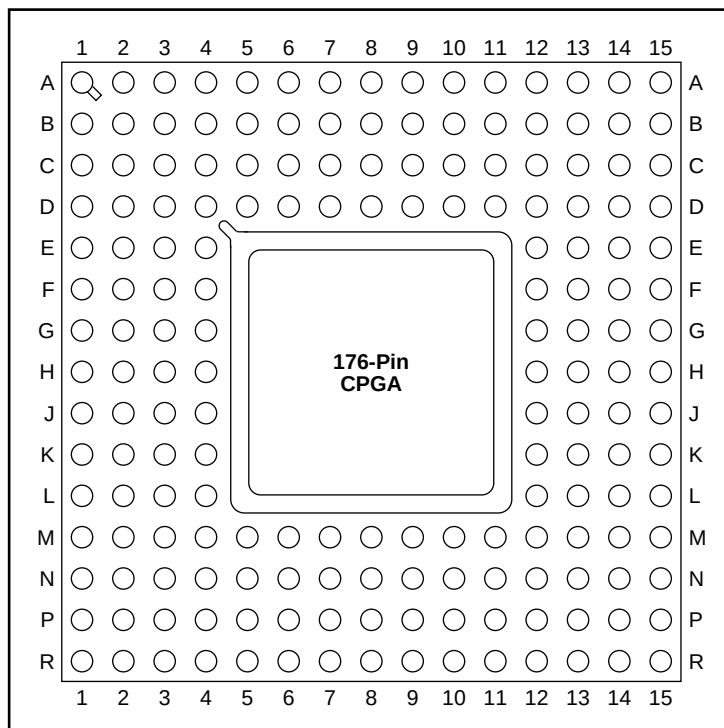
| Pin Number | A1425A Function |
|------------|-----------------|
| A1         | NC              |
| A2         | GND             |
| A3         | I/O             |
| A4         | I/O             |
| A5         | I/O             |
| A6         | PRA, I/O        |
| A7         | NC              |
| A8         | I/O             |
| A9         | I/O             |
| A10        | I/O             |
| A11        | I/O             |
| A12        | I/O             |
| A13        | NC              |
| B1         | I/O             |
| B2         | V <sub>CC</sub> |
| B3         | I/O             |
| B4         | I/O             |
| B5         | I/O             |
| B6         | CLKB, I/O       |
| B7         | V <sub>CC</sub> |
| B8         | I/O             |
| B9         | I/O             |
| B10        | I/O             |
| B11        | I/O             |
| B12        | V <sub>CC</sub> |
| B13        | I/O             |
| C1         | I/O             |
| C2         | SDI, I/O        |
| C3         | GND             |
| C4         | I/O             |
| C5         | I/O             |
| C6         | I/O             |
| C7         | GND             |
| C8         | I/O             |
| C9         | I/O             |
| C10        | IOCLK, I/O      |
| C11        | GND             |
| C12        | GND             |
| C13        | I/O             |
| D1         | I/O             |
| D2         | I/O             |
| D3         | I/O             |
| D4         | DCLK, I/O       |
| D6         | CLKA, I/O       |
| D7         | I/O             |

| Pin Number | A1425A Function |
|------------|-----------------|
| D8         | I/O             |
| D11        | I/O             |
| D12        | I/O             |
| D13        | I/O             |
| E1         | I/O             |
| E2         | I/O             |
| E3         | MODE            |
| E11        | V <sub>CC</sub> |
| E12        | I/O             |
| E13        | I/O             |
| F1         | I/O             |
| F2         | I/O             |
| F3         | I/O             |
| F4         | I/O             |
| F10        | GND             |
| F11        | I/O             |
| F12        | I/O             |
| F13        | I/O             |
| G1         | NC              |
| G2         | V <sub>CC</sub> |
| G3         | GND             |
| G4         | I/O             |
| G10        | I/O             |
| G11        | GND             |
| G12        | V <sub>CC</sub> |
| G13        | NC              |
| H1         | I/O             |
| H2         | I/O             |
| H3         | I/O             |
| H4         | I/O             |
| H10        | I/O             |
| H11        | I/O             |
| H12        | I/O             |
| H13        | I/O             |
| J1         | I/O             |
| J2         | V <sub>CC</sub> |
| J3         | I/O             |
| J11        | I/O             |
| J12        | V <sub>CC</sub> |
| J13        | I/O             |
| K1         | I/O             |
| K2         | I/O             |
| K3         | I/O             |
| K6         | I/O             |
| K7         | HCLKA, I/O      |

| Pin Number | A1425A Function |
|------------|-----------------|
| K8         | I/O             |
| K11        | I/O             |
| K12        | I/O             |
| K13        | I/O             |
| L1         | I/O             |
| L2         | I/O             |
| L3         | GND             |
| L4         | I/O             |
| L5         | I/O             |
| L6         | PRB, I/O        |
| L7         | GND             |
| L8         | I/O             |
| L9         | I/O             |
| L10        | IOPCL, I/O      |
| L11        | GND             |
| L12        | I/O             |
| L13        | I/O             |
| M1         | I/O             |
| M2         | V <sub>CC</sub> |
| M3         | GND             |
| M4         | I/O             |
| M5         | I/O             |
| M6         | I/O             |
| M7         | V <sub>CC</sub> |
| M8         | I/O             |
| M9         | I/O             |
| M10        | I/O             |
| M11        | I/O             |
| M12        | V <sub>CC</sub> |
| M13        | I/O             |
| N1         | NC              |
| N2         | I/O             |
| N3         | I/O             |
| N4         | I/O             |
| N5         | I/O             |
| N6         | I/O             |
| N7         | NC              |
| N8         | I/O             |
| N9         | I/O             |
| N10        | I/O             |
| N11        | I/O             |
| N12        | GND             |
| N13        | NC              |

## Package Pin Assignments (continued)

### 176-Pin CPGA (Top View)



## 176-Pin CPGA

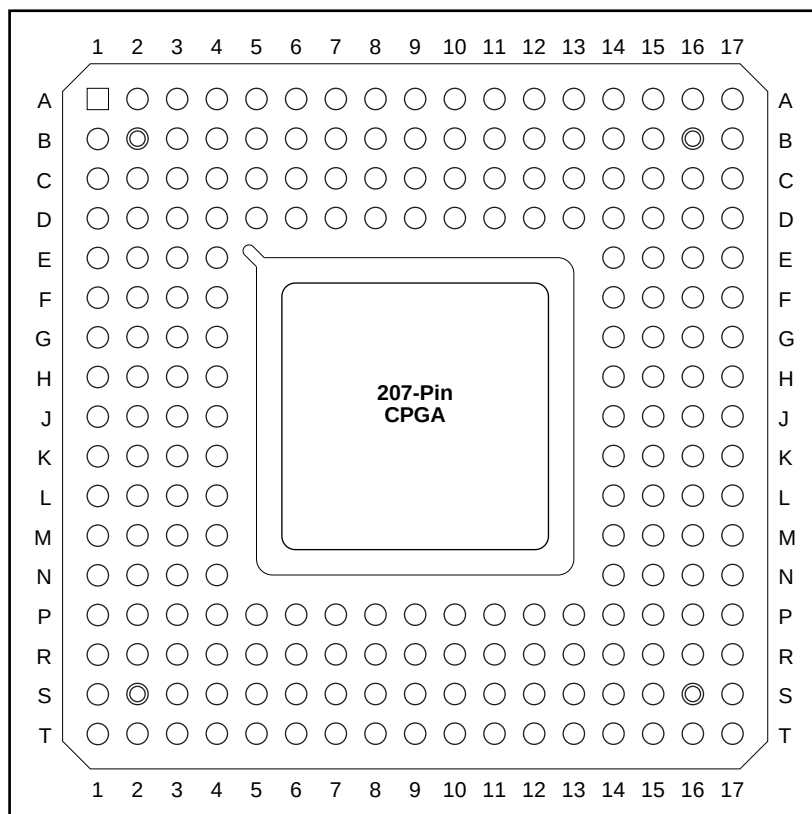
| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| A1         | I/O                | I/O                 |
| A2         | I/O                | I/O                 |
| A3         | I/O                | I/O                 |
| A4         | I/O                | I/O                 |
| A5         | I/O                | I/O                 |
| A6         | I/O                | I/O                 |
| A7         | I/O                | I/O                 |
| A8         | I/O                | I/O                 |
| A9         | CLKA, I/O          | CLKA, I/O           |
| A10        | I/O                | I/O                 |
| A11        | I/O                | I/O                 |
| A12        | I/O                | I/O                 |
| A13        | I/O                | I/O                 |
| A14        | I/O                | I/O                 |
| A15        | I/O                | I/O                 |
| B1         | I/O                | I/O                 |
| B2         | I/O                | I/O                 |
| B3         | DCLK, I/O          | DCLK, I/O           |
| B4         | I/O                | I/O                 |
| B5         | I/O                | I/O                 |
| B6         | I/O                | I/O                 |
| B7         | I/O                | I/O                 |
| B8         | CLKB, I/O          | CLKB, I/O           |
| B9         | I/O                | I/O                 |
| B10        | I/O                | I/O                 |
| B11        | I/O                | I/O                 |
| B12        | I/O                | I/O                 |
| B13        | I/O                | I/O                 |
| B14        | SDI, I/O           | SDI, I/O            |
| B15        | I/O                | I/O                 |
| C1         | I/O                | I/O                 |
| C2         | I/O                | I/O                 |
| C3         | MODE               | MODE                |
| C4         | I/O                | I/O                 |
| C5         | I/O                | I/O                 |
| C6         | I/O                | I/O                 |
| C7         | I/O                | I/O                 |
| C8         | GND                | GND                 |
| C9         | PRA, I/O           | PRA, I/O            |
| C10        | I/O                | I/O                 |
| C11        | I/O                | I/O                 |
| C12        | I/O                | I/O                 |
| C13        | I/O                | I/O                 |
| C14        | I/O                | I/O                 |

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| C15        | I/O                | I/O                 |
| D1         | I/O                | I/O                 |
| D2         | I/O                | I/O                 |
| D3         | I/O                | I/O                 |
| D4         | GND                | GND                 |
| D5         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| D6         | GND                | GND                 |
| D7         | PRB, I/O           | PRB, I/O            |
| D8         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| D9         | I/O                | I/O                 |
| D10        | GND                | GND                 |
| D11        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| D12        | GND                | GND                 |
| D13        | I/O                | I/O                 |
| D14        | I/O                | I/O                 |
| D15        | I/O                | I/O                 |
| E1         | I/O                | I/O                 |
| E2         | I/O                | I/O                 |
| E3         | I/O                | I/O                 |
| E4         | GND                | GND                 |
| E12        | GND                | GND                 |
| E13        | I/O                | I/O                 |
| E14        | I/O                | I/O                 |
| E15        | I/O                | I/O                 |
| F1         | I/O                | I/O                 |
| F2         | I/O                | I/O                 |
| F3         | I/O                | I/O                 |
| F4         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| F12        | GND                | GND                 |
| F13        | I/O                | I/O                 |
| F14        | I/O                | I/O                 |
| F15        | I/O                | I/O                 |
| G1         | I/O                | I/O                 |
| G2         | I/O                | I/O                 |
| G3         | I/O                | I/O                 |
| G4         | GND                | GND                 |
| G12        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| G13        | I/O                | I/O                 |
| G14        | I/O                | I/O                 |
| G15        | I/O                | I/O                 |
| H1         | I/O                | I/O                 |
| H2         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| H3         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| H4         | GND                | GND                 |

**176-Pin CPGA (Continued)**

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| H12        | GND                | GND                 |
| H13        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| H14        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| H15        | I/O                | I/O                 |
| J1         | I/O                | I/O                 |
| J2         | I/O                | I/O                 |
| J3         | I/O                | I/O                 |
| J4         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| J12        | GND                | GND                 |
| J13        | GND                | GND                 |
| J14        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| J15        | I/O                | I/O                 |
| K1         | I/O                | I/O                 |
| K2         | I/O                | I/O                 |
| K3         | I/O                | I/O                 |
| K4         | GND                | GND                 |
| K12        | GND                | GND                 |
| K13        | I/O                | I/O                 |
| K14        | I/O                | I/O                 |
| K15        | I/O                | I/O                 |
| L1         | I/O                | I/O                 |
| L2         | I/O                | I/O                 |
| L3         | I/O                | I/O                 |
| L4         | GND                | GND                 |
| L12        | I/O                | I/O                 |
| L13        | I/O                | I/O                 |
| L14        | I/O                | I/O                 |
| L15        | I/O                | I/O                 |
| M1         | I/O                | I/O                 |
| M2         | I/O                | I/O                 |
| M3         | I/O                | I/O                 |
| M4         | GND                | GND                 |
| M5         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| M6         | GND                | GND                 |
| M7         | I/O                | I/O                 |
| M8         | GND                | GND                 |
| M9         | I/O                | I/O                 |
| M10        | GND                | GND                 |
| M11        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| M12        | GND                | GND                 |
| M13        | I/O                | I/O                 |
| M14        | I/O                | I/O                 |
| M15        | I/O                | I/O                 |
| N1         | I/O                | I/O                 |

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| N2         | I/O                | I/O                 |
| N3         | I/O                | I/O                 |
| N4         | I/O                | I/O                 |
| N5         | I/O                | I/O                 |
| N6         | I/O                | I/O                 |
| N7         | I/O                | I/O                 |
| N8         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| N9         | I/O                | I/O                 |
| N10        | I/O                | I/O                 |
| N11        | I/O                | I/O                 |
| N12        | I/O                | I/O                 |
| N13        | I/O                | I/O                 |
| N14        | I/O                | I/O                 |
| N15        | I/O                | I/O                 |
| P1         | I/O                | I/O                 |
| P2         | I/O                | I/O                 |
| P3         | I/O                | I/O                 |
| P4         | I/O                | I/O                 |
| P5         | I/O                | I/O                 |
| P6         | I/O                | I/O                 |
| P7         | I/O                | I/O                 |
| P8         | I/O                | I/O                 |
| P9         | I/O                | I/O                 |
| P10        | I/O                | I/O                 |
| P11        | I/O                | I/O                 |
| P12        | I/O                | I/O                 |
| P13        | I/O                | I/O                 |
| P14        | I/O                | I/O                 |
| P15        | I/O                | I/O                 |
| R1         | I/O                | I/O                 |
| R2         | I/O                | I/O                 |
| R3         | I/O                | I/O                 |
| R4         | I/O                | I/O                 |
| R5         | I/O                | I/O                 |
| R6         | I/O                | I/O                 |
| R7         | I/O                | I/O                 |
| R8         | I/O                | I/O                 |
| R9         | I/O                | I/O                 |
| R10        | I/O                | I/O                 |
| R11        | I/O                | I/O                 |
| R12        | I/O                | I/O                 |
| R13        | I/O                | I/O                 |
| R14        | I/O                | I/O                 |
| R15        | I/O                | I/O                 |

**Package Pin Assignments (continued)****207-Pin CPGA (Top View)**

## 207-Pin CPGA

| Pin Number | A1460A Function |
|------------|-----------------|
| A1         | NC              |
| A2         | NC              |
| A3         | I/O             |
| A4         | I/O             |
| A5         | I/O             |
| A6         | I/O             |
| A7         | I/O             |
| A8         | I/O             |
| A9         | I/O             |
| A10        | I/O             |
| A11        | I/O             |
| A12        | I/O             |
| A13        | I/O             |
| A14        | I/O             |
| A15        | I/O             |
| A16        | NC              |
| A17        | NC              |
| B1         | NC              |
| B2         | V <sub>CC</sub> |
| B3         | I/O             |
| B4         | I/O             |
| B5         | I/O             |
| B6         | I/O             |
| B7         | I/O             |
| B8         | I/O             |
| B9         | V <sub>CC</sub> |
| B10        | I/O             |
| B11        | I/O             |
| B12        | I/O             |
| B13        | I/O             |
| B14        | I/O             |
| B15        | I/O             |
| B16        | V <sub>CC</sub> |
| B17        | NC              |
| C1         | NC              |
| C2         | NC              |
| C3         | SDI, I/O        |
| C4         | I/O             |
| C5         | I/O             |
| C6         | I/O             |
| C7         | I/O             |
| C8         | I/O             |
| C9         | I/O             |

| Pin Number | A1460A Function |
|------------|-----------------|
| C10        | I/O             |
| C11        | I/O             |
| C12        | I/O             |
| C13        | I/O             |
| C14        | I/O             |
| C15        | GND             |
| C16        | I/O             |
| C17        | I/O             |
| D1         | I/O             |
| D2         | I/O             |
| D3         | I/O             |
| D4         | GND             |
| D5         | GND             |
| D6         | I/O             |
| D7         | MODE            |
| D8         | I/O             |
| D9         | GND             |
| D10        | I/O             |
| D11        | V <sub>CC</sub> |
| D12        | I/O             |
| D13        | I/O             |
| D14        | GND             |
| D15        | I/O             |
| D16        | I/O             |
| D17        | I/O             |
| E1         | I/O             |
| E2         | I/O             |
| E3         | I/O             |
| E4         | DCLK, I/O       |
| E14        | I/O             |
| E15        | I/O             |
| E16        | I/O             |
| E17        | I/O             |
| F1         | I/O             |
| F2         | I/O             |
| F3         | I/O             |
| F4         | I/O             |
| F14        | I/O             |
| F15        | I/O             |
| F16        | I/O             |
| F17        | I/O             |
| G1         | I/O             |
| G2         | I/O             |

| Pin Number | A1460A Function |
|------------|-----------------|
| G3         | I/O             |
| G4         | I/O             |
| G14        | I/O             |
| G15        | I/O             |
| G16        | I/O             |
| G17        | I/O             |
| H1         | PRA, I/O        |
| H2         | I/O             |
| H3         | I/O             |
| H4         | I/O             |
| H14        | I/O             |
| H15        | I/O             |
| H16        | I/O             |
| H17        | I/O             |
| J1         | I/O             |
| J2         | V <sub>CC</sub> |
| J3         | CLKB, I/O       |
| J4         | GND             |
| J14        | GND             |
| J15        | HCLK, I/O       |
| J16        | V <sub>CC</sub> |
| J17        | I/O             |
| K1         | CLKA, I/O       |
| K2         | I/O             |
| K3         | I/O             |
| K4         | I/O             |
| K14        | I/O             |
| K15        | I/O             |
| K16        | PRB, I/O        |
| K17        | I/O             |
| L1         | I/O             |
| L2         | I/O             |
| L3         | I/O             |
| L4         | I/O             |
| L14        | I/O             |
| L15        | I/O             |
| L16        | I/O             |
| L17        | I/O             |
| M1         | I/O             |
| M2         | I/O             |
| M3         | I/O             |
| M4         | I/O             |
| M14        | I/O             |

**207-Pin CPGA (Continued)**

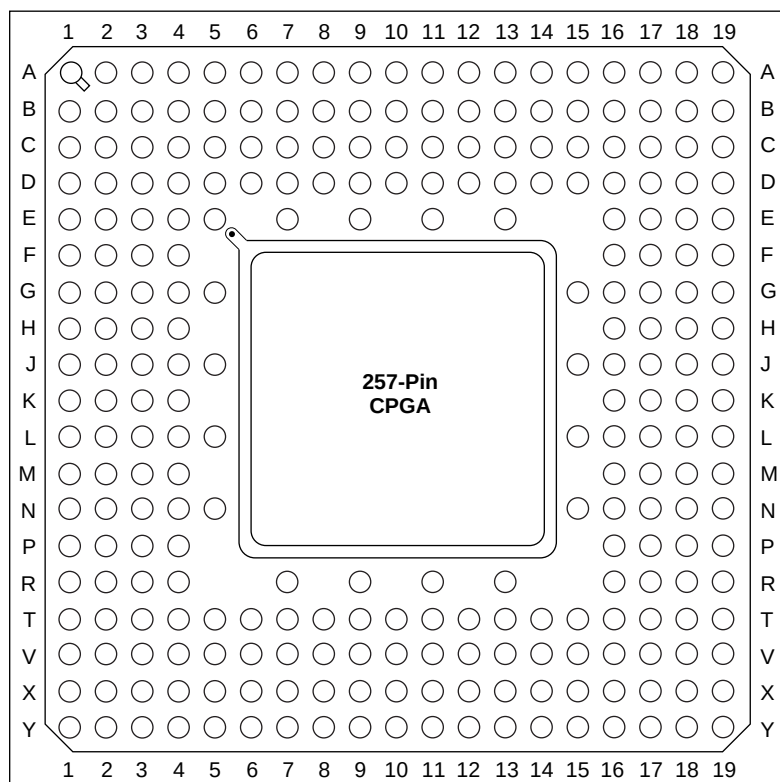
| Pin Number | A1460A Function |
|------------|-----------------|
| M15        | I/O             |
| M16        | I/O             |
| M17        | I/O             |
| N1         | I/O             |
| N2         | I/O             |
| N3         | I/O             |
| N4         | I/O             |
| N14        | IOPCL, I/O      |
| N15        | I/O             |
| N16        | I/O             |
| N17        | I/O             |
| P1         | I/O             |
| P2         | I/O             |
| P3         | GND             |
| P4         | GND             |
| P5         | IOCLK, I/O      |
| P6         | I/O             |
| P7         | GND             |
| P8         | I/O             |
| P9         | GND             |
| P10        | I/O             |
| P11        | I/O             |
| P12        | V <sub>CC</sub> |
| P13        | I/O             |
| P14        | GND             |
| P15        | I/O             |
| P16        | I/O             |

| Pin Number | A1460A Function |
|------------|-----------------|
| P17        | I/O             |
| R1         | I/O             |
| R2         | I/O             |
| R3         | I/O             |
| R4         | I/O             |
| R5         | I/O             |
| R6         | I/O             |
| R7         | I/O             |
| R8         | I/O             |
| R9         | I/O             |
| R10        | I/O             |
| R11        | I/O             |
| R12        | I/O             |
| R13        | I/O             |
| R14        | I/O             |
| R15        | GND             |
| R16        | I/O             |
| R17        | I/O             |
| S1         | NC              |
| S2         | V <sub>CC</sub> |
| S3         | NC              |
| S4         | I/O             |
| S5         | I/O             |
| S6         | I/O             |
| S7         | I/O             |
| S8         | I/O             |
| S9         | V <sub>CC</sub> |

| Pin Number | A1460A Function |
|------------|-----------------|
| S10        | I/O             |
| S11        | I/O             |
| S12        | I/O             |
| S13        | I/O             |
| S14        | I/O             |
| S15        | I/O             |
| S16        | V <sub>CC</sub> |
| S17        | NC              |
| T1         | NC              |
| T2         | NC              |
| T3         | I/O             |
| T4         | I/O             |
| T5         | V <sub>CC</sub> |
| T6         | I/O             |
| T7         | I/O             |
| T8         | I/O             |
| T9         | I/O             |
| T10        | I/O             |
| T11        | I/O             |
| T12        | I/O             |
| T13        | I/O             |
| T14        | I/O             |
| T15        | I/O             |
| T16        | NC              |
| T17        | NC              |

## Package Pin Assignments (continued)

### 257-Pin CPGA (Top View)



## 257-Pin CPGA

| Pin Number | A14100A Function |
|------------|------------------|
| A1         | I/O              |
| A2         | I/O              |
| A3         | I/O              |
| A4         | I/O              |
| A5         | MODE             |
| A6         | I/O              |
| A7         | I/O              |
| A8         | I/O              |
| A9         | I/O              |
| A10        | I/O              |
| A11        | I/O              |
| A12        | I/O              |
| A13        | I/O              |
| A14        | I/O              |
| A15        | I/O              |
| A16        | I/O              |
| A17        | I/O              |
| A18        | I/O              |
| A19        | I/O              |
| B1         | I/O              |
| B2         | I/O              |
| B3         | I/O              |
| B4         | SDI, I/O         |
| B5         | I/O              |
| B6         | I/O              |
| B7         | I/O              |
| B8         | I/O              |
| B9         | I/O              |
| B10        | I/O              |
| B11        | I/O              |
| B12        | I/O              |
| B13        | I/O              |
| B14        | I/O              |
| B15        | I/O              |
| B16        | GND              |
| B17        | I/O              |
| B18        | I/O              |
| B19        | I/O              |
| C1         | I/O              |
| C2         | I/O              |
| C3         | V <sub>CC</sub>  |
| C4         | GND              |
| C5         | I/O              |
| C6         | I/O              |

| Pin Number | A14100A Function |
|------------|------------------|
| C7         | I/O              |
| C8         | I/O              |
| C9         | I/O              |
| C10        | V <sub>CC</sub>  |
| C11        | I/O              |
| C12        | I/O              |
| C13        | V <sub>CC</sub>  |
| C14        | I/O              |
| C15        | I/O              |
| C16        | I/O              |
| C17        | V <sub>CC</sub>  |
| C18        | I/O              |
| C19        | I/O              |
| D1         | I/O              |
| D2         | I/O              |
| D3         | I/O              |
| D4         | GND              |
| D5         | I/O              |
| D6         | I/O              |
| D7         | I/O              |
| D8         | I/O              |
| D9         | I/O              |
| D10        | GND              |
| D11        | I/O              |
| D12        | I/O              |
| D13        | I/O              |
| D14        | I/O              |
| D15        | I/O              |
| D16        | GND              |
| D17        | I/O              |
| D18        | I/O              |
| D19        | I/O              |
| E1         | I/O              |
| E2         | I/O              |
| E3         | I/O              |
| E4         | DCLK, I/O        |
| E5         | NC               |
| E7         | I/O              |
| E9         | I/O              |
| E11        | GND              |
| E13        | I/O              |
| E16        | I/O              |
| E17        | I/O              |
| E18        | I/O              |

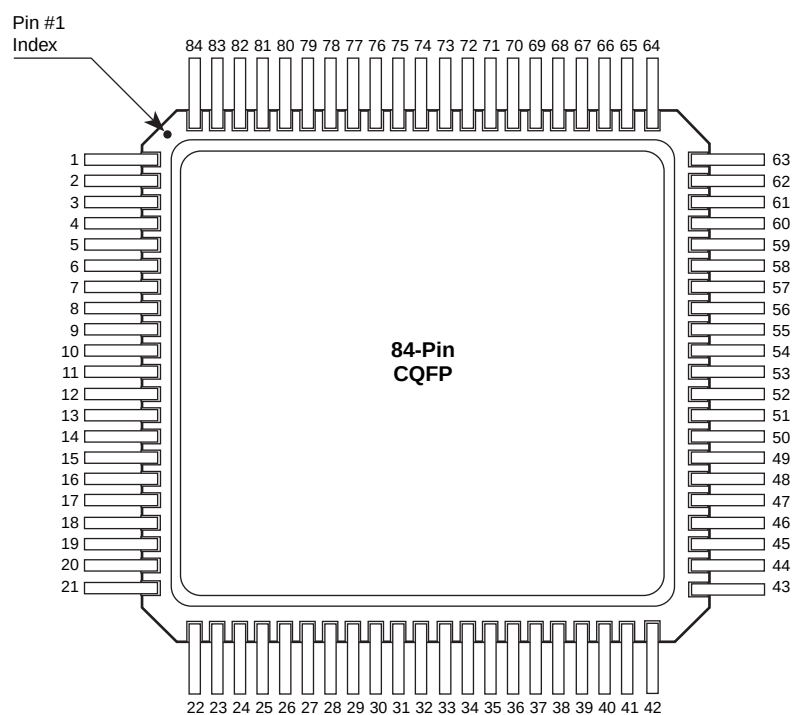
| Pin Number | A14100A Function |
|------------|------------------|
| E19        | I/O              |
| F1         | I/O              |
| F2         | I/O              |
| F3         | I/O              |
| F4         | I/O              |
| F16        | I/O              |
| F17        | I/O              |
| F18        | I/O              |
| F19        | I/O              |
| G1         | I/O              |
| G2         | I/O              |
| G3         | I/O              |
| G4         | I/O              |
| G5         | I/O              |
| G15        | I/O              |
| G16        | I/O              |
| G17        | I/O              |
| G18        | I/O              |
| G19        | I/O              |
| H1         | I/O              |
| H2         | I/O              |
| H3         | I/O              |
| H4         | I/O              |
| H16        | I/O              |
| H17        | I/O              |
| H18        | I/O              |
| H19        | I/O              |
| J1         | PRA, I/O         |
| J2         | I/O              |
| J3         | I/O              |
| J4         | I/O              |
| J5         | GND              |
| J15        | I/O              |
| J16        | HCLK, I/O        |
| J17        | PRB, I/O         |
| J18        | I/O              |
| J19        | I/O              |
| K1         | I/O              |
| K2         | I/O              |
| K3         | V <sub>CC</sub>  |
| K4         | GND              |
| K16        | GND              |
| K17        | V <sub>CC</sub>  |
| K18        | I/O              |

## 257-Pin CPGA (Continued)

| Pin Number | A14100A Function |
|------------|------------------|
| K19        | I/O              |
| L1         | I/O              |
| L2         | I/O              |
| L3         | I/O              |
| L4         | CLKA, I/O        |
| L5         | CLKB, I/O        |
| L15        | GND              |
| L16        | I/O              |
| L17        | I/O              |
| L18        | I/O              |
| L19        | I/O              |
| M1         | I/O              |
| M2         | I/O              |
| M3         | I/O              |
| M4         | I/O              |
| M16        | I/O              |
| M17        | I/O              |
| M18        | I/O              |
| M19        | I/O              |
| N1         | I/O              |
| N2         | I/O              |
| N3         | I/O              |
| N4         | I/O              |
| N5         | I/O              |
| N15        | I/O              |
| N16        | I/O              |
| N17        | I/O              |
| N18        | I/O              |
| N19        | I/O              |
| P1         | I/O              |
| P2         | I/O              |
| P3         | I/O              |
| P4         | I/O              |
| P16        | I/O              |
| P17        | I/O              |
| P18        | I/O              |
| P19        | I/O              |
| R1         | I/O              |
| R2         | I/O              |
| R3         | I/O              |
| R4         | GND              |
| R7         | I/O              |

| Pin Number | A14100A Function |
|------------|------------------|
| R9         | I/O              |
| R11        | I/O              |
| R13        | I/O              |
| R16        | IOPCL, I/O       |
| R17        | I/O              |
| R18        | I/O              |
| R19        | I/O              |
| T1         | I/O              |
| T2         | I/O              |
| T3         | I/O              |
| T4         | GND              |
| T5         | IOCLK, I/O       |
| T6         | I/O              |
| T7         | I/O              |
| T8         | I/O              |
| T9         | I/O              |
| T10        | GND              |
| T11        | I/O              |
| T12        | I/O              |
| T13        | I/O              |
| T14        | I/O              |
| T15        | I/O              |
| T16        | GND              |
| T17        | GND              |
| T18        | I/O              |
| T19        | I/O              |
| V1         | I/O              |
| V2         | I/O              |
| V3         | V <sub>CC</sub>  |
| V4         | I/O              |
| V5         | I/O              |
| V6         | I/O              |
| V7         | V <sub>CC</sub>  |
| V8         | I/O              |
| V9         | I/O              |
| V10        | V <sub>CC</sub>  |
| V11        | I/O              |
| V12        | I/O              |
| V13        | I/O              |
| V14        | I/O              |
| V15        | I/O              |
| V16        | I/O              |

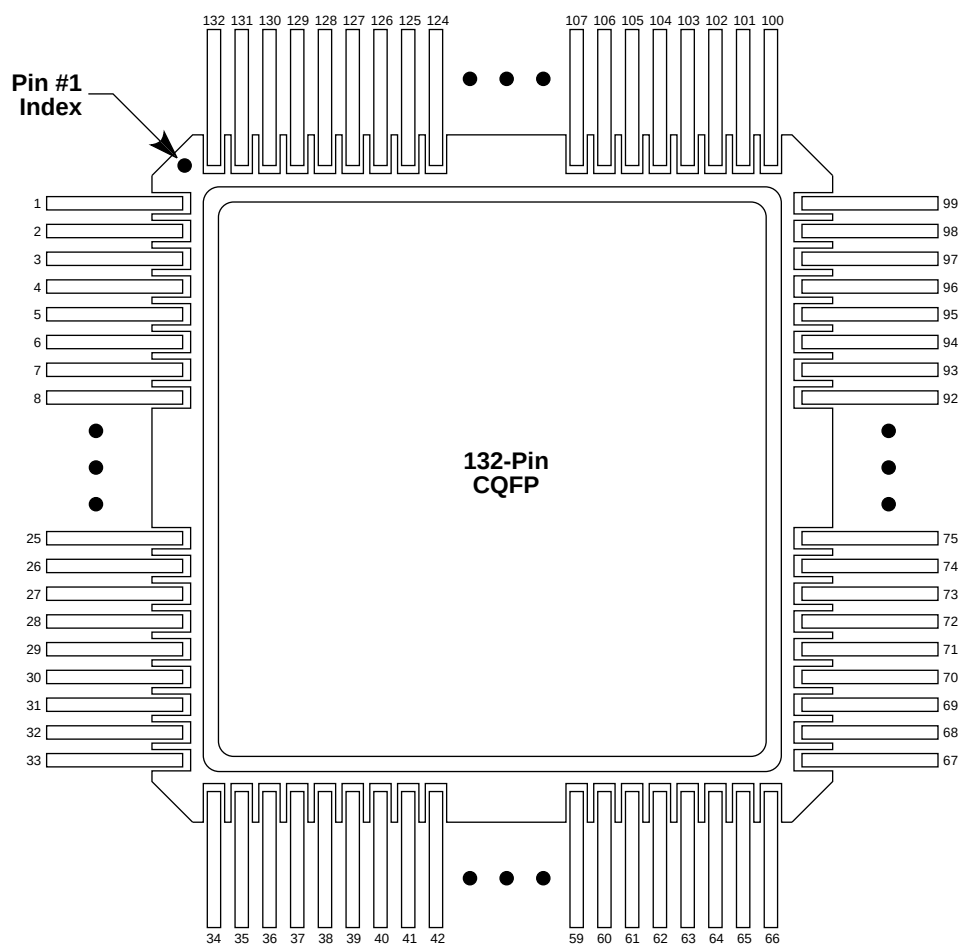
| Pin Number | A14100A Function |
|------------|------------------|
| V17        | V <sub>CC</sub>  |
| V18        | I/O              |
| V19        | I/O              |
| X1         | I/O              |
| X2         | I/O              |
| X3         | I/O              |
| X4         | I/O              |
| X5         | I/O              |
| X6         | I/O              |
| X7         | GND              |
| X8         | I/O              |
| X9         | I/O              |
| X10        | I/O              |
| X11        | I/O              |
| X12        | I/O              |
| X13        | I/O              |
| X14        | V <sub>CC</sub>  |
| X15        | I/O              |
| X16        | I/O              |
| X17        | I/O              |
| X18        | I/O              |
| X19        | I/O              |
| Y1         | I/O              |
| Y2         | I/O              |
| Y3         | I/O              |
| Y4         | I/O              |
| Y5         | I/O              |
| Y6         | I/O              |
| Y7         | I/O              |
| Y8         | I/O              |
| Y9         | I/O              |
| Y10        | I/O              |
| Y11        | I/O              |
| Y12        | I/O              |
| Y13        | I/O              |
| Y14        | I/O              |
| Y15        | I/O              |
| Y16        | I/O              |
| Y17        | I/O              |
| Y18        | I/O              |
| Y19        | I/O              |

**Package Pin Assignments (continued)****84-Pin CQFP (Top View)**

## 84-Pin CQFP

| Pin Number | A1020B Function | A32100DX Function |
|------------|-----------------|-------------------|
| 1          | NC              | GND               |
| 2          | I/O             | MODE              |
| 3          | I/O             | I/O               |
| 4          | I/O             | I/O               |
| 5          | I/O             | I/O               |
| 6          | I/O             | I/O               |
| 7          | GND             | V <sub>CC</sub>   |
| 8          | GND             | I/O               |
| 9          | I/O             | I/O               |
| 10         | I/O             | GND               |
| 11         | I/O             | V <sub>CC</sub>   |
| 12         | I/O             | V <sub>CC</sub>   |
| 13         | I/O             | I/O               |
| 14         | V <sub>CC</sub> | I/O               |
| 15         | V <sub>CC</sub> | I/O               |
| 16         | I/O             | I/O               |
| 17         | I/O             | GND               |
| 18         | I/O             | I/O               |
| 19         | I/O             | I/O               |
| 20         | I/O             | I/O               |
| 21         | I/O             | I/O               |
| 22         | V <sub>CC</sub> | GND               |
| 23         | I/O             | I/O               |
| 24         | I/O             | I/O               |
| 25         | I/O             | I/O (WD)          |
| 26         | I/O             | I/O (WD)          |
| 27         | I/O             | I/O               |
| 28         | I/O             | QCLKA, I/O        |
| 29         | GND             | GND               |
| 30         | I/O             | I/O (WD)          |
| 31         | I/O             | I/O               |
| 32         | I/O             | GND               |
| 33         | I/O             | V <sub>CC</sub>   |
| 34         | I/O             | I/O (WD)          |
| 35         | V <sub>CC</sub> | I/O (WD)          |
| 36         | I/O             | QCLKB, I/O        |
| 37         | I/O             | I/O (WD)          |
| 38         | I/O             | GND               |
| 39         | I/O             | I/O (WD)          |
| 40         | I/O             | I/O (WD)          |
| 41         | I/O             | I/O (WD)          |
| 42         | I/O             | SDO, I/O          |

| Pin Number | A1020B Function | A32100DX Function |
|------------|-----------------|-------------------|
| 43         | I/O             | GND               |
| 44         | I/O             | I/O               |
| 45         | I/O             | I/O               |
| 46         | I/O             | I/O               |
| 47         | I/O             | I/O               |
| 48         | I/O             | I/O               |
| 49         | GND             | I/O               |
| 50         | GND             | GND               |
| 51         | I/O             | TCK, I/O          |
| 52         | I/O             | GND               |
| 53         | CLKA, I/O       | V <sub>CC</sub>   |
| 54         | I/O             | V <sub>CC</sub>   |
| 55         | MODE            | V <sub>CC</sub>   |
| 56         | V <sub>CC</sub> | V <sub>CC</sub>   |
| 57         | V <sub>CC</sub> | I/O               |
| 58         | I/O             | I/O               |
| 59         | I/O             | GND               |
| 60         | I/O             | I/O               |
| 61         | SDI, I/O        | I/O               |
| 62         | DCLK, I/O       | I/O               |
| 63         | PRA, I/O        | GND               |
| 64         | PRB, I/O        | SDI, I/O          |
| 65         | I/O             | I/O (WD)          |
| 66         | I/O             | I/O (WD)          |
| 67         | I/O             | I/O (WD)          |
| 68         | I/O             | I/O (WD)          |
| 69         | I/O             | QCLKD, I/O        |
| 70         | I/O             | I/O (WD)          |
| 71         | GND             | I/O (WD)          |
| 72         | I/O             | PRA, I/O          |
| 73         | I/O             | CLKA, I/O         |
| 74         | I/O             | V <sub>CC</sub>   |
| 75         | I/O             | GND               |
| 76         | I/O             | CLKB, I/O         |
| 77         | V <sub>CC</sub> | PRB, I/O          |
| 78         | I/O             | I/O (WD)          |
| 79         | I/O             | I/O (WD)          |
| 80         | I/O             | QCLKC, I/O        |
| 81         | I/O             | GND               |
| 82         | I/O             | I/O (WD)          |
| 83         | I/O             | I/O (WD)          |
| 84         | I/O             | DCLK, I/O         |

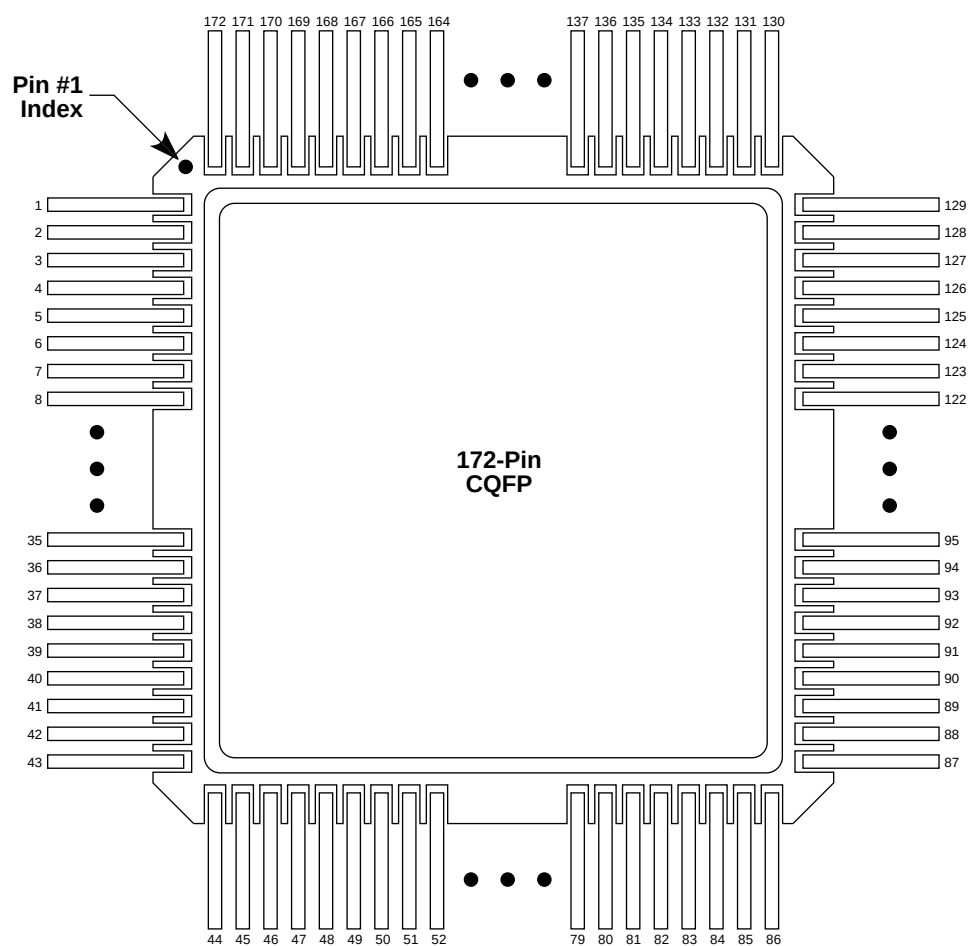
**Package Pin Assignments (continued)****132-Pin CQFP (Top View)**

# 132-Pin CQFP

| Pin Number | A1425A Function |
|------------|-----------------|
| 1          | NC              |
| 2          | GND             |
| 3          | SDI, I/O        |
| 4          | I/O             |
| 5          | I/O             |
| 6          | I/O             |
| 7          | I/O             |
| 8          | I/O             |
| 9          | MODE            |
| 10         | GND             |
| 11         | V <sub>CC</sub> |
| 12         | I/O             |
| 13         | I/O             |
| 14         | I/O             |
| 15         | I/O             |
| 16         | I/O             |
| 17         | I/O             |
| 18         | I/O             |
| 19         | I/O             |
| 20         | I/O             |
| 21         | I/O             |
| 22         | V <sub>CC</sub> |
| 23         | I/O             |
| 24         | I/O             |
| 25         | I/O             |
| 26         | GND             |
| 27         | V <sub>CC</sub> |
| 28         | I/O             |
| 29         | I/O             |
| 30         | I/O             |
| 31         | I/O             |
| 32         | I/O             |
| 33         | I/O             |
| 34         | NC              |
| 35         | I/O             |
| 36         | GND             |
| 37         | I/O             |
| 38         | I/O             |
| 39         | I/O             |
| 40         | I/O             |
| 41         | I/O             |
| 42         | GND             |
| 43         | V <sub>CC</sub> |
| 44         | I/O             |

| Pin Number | A1425A Function |
|------------|-----------------|
| 45         | I/O             |
| 46         | I/O             |
| 47         | I/O             |
| 48         | PRB, I/O        |
| 49         | I/O             |
| 50         | HCLK, I/O       |
| 51         | I/O             |
| 52         | I/O             |
| 53         | I/O             |
| 54         | I/O             |
| 55         | I/O             |
| 56         | I/O             |
| 57         | I/O             |
| 58         | GND             |
| 59         | V <sub>CC</sub> |
| 60         | I/O             |
| 61         | I/O             |
| 62         | I/O             |
| 63         | I/O             |
| 64         | IOPCL, I/O      |
| 65         | GND             |
| 66         | NC              |
| 67         | NC              |
| 68         | I/O             |
| 69         | I/O             |
| 70         | I/O             |
| 71         | I/O             |
| 72         | I/O             |
| 73         | I/O             |
| 74         | GND             |
| 75         | V <sub>CC</sub> |
| 76         | I/O             |
| 77         | I/O             |
| 78         | V <sub>CC</sub> |
| 79         | I/O             |
| 80         | I/O             |
| 81         | I/O             |
| 82         | I/O             |
| 83         | I/O             |
| 84         | I/O             |
| 85         | I/O             |
| 86         | I/O             |
| 87         | I/O             |
| 88         | I/O             |

| Pin Number | A1425A Function |
|------------|-----------------|
| 89         | V <sub>CC</sub> |
| 90         | GND             |
| 91         | V <sub>CC</sub> |
| 92         | GND             |
| 93         | I/O             |
| 94         | I/O             |
| 95         | I/O             |
| 96         | I/O             |
| 97         | I/O             |
| 98         | IOCLK, I/O      |
| 99         | NC              |
| 100        | NC              |
| 101        | GND             |
| 102        | I/O             |
| 103        | I/O             |
| 104        | I/O             |
| 105        | I/O             |
| 106        | GND             |
| 107        | V <sub>CC</sub> |
| 108        | I/O             |
| 109        | I/O             |
| 110        | I/O             |
| 111        | I/O             |
| 112        | I/O             |
| 113        | I/O             |
| 114        | I/O             |
| 115        | I/O             |
| 116        | CLKA, I/O       |
| 117        | CLKB, I/O       |
| 118        | PRA, I/O        |
| 119        | I/O             |
| 120        | I/O             |
| 121        | I/O             |
| 122        | GND             |
| 123        | V <sub>CC</sub> |
| 124        | I/O             |
| 125        | I/O             |
| 126        | I/O             |
| 127        | I/O             |
| 128        | I/O             |
| 129        | I/O             |
| 130        | I/O             |
| 131        | DCLK, I/O       |
| 132        | NC              |

**Package Pin Assignments (continued)****172-Pin CQFP (Top View)**

## 172-Pin CQFP

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| 1          | MODE               | MODE                |
| 2          | I/O                | I/O                 |
| 3          | I/O                | I/O                 |
| 4          | I/O                | I/O                 |
| 5          | I/O                | I/O                 |
| 6          | I/O                | I/O                 |
| 7          | GND                | GND                 |
| 8          | I/O                | I/O                 |
| 9          | I/O                | I/O                 |
| 10         | I/O                | I/O                 |
| 11         | I/O                | I/O                 |
| 12         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 13         | I/O                | I/O                 |
| 14         | I/O                | I/O                 |
| 15         | I/O                | I/O                 |
| 16         | I/O                | I/O                 |
| 17         | GND                | GND                 |
| 18         | I/O                | I/O                 |
| 19         | I/O                | I/O                 |
| 20         | I/O                | I/O                 |
| 21         | I/O                | I/O                 |
| 22         | GND                | GND                 |
| 23         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 24         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 25         | I/O                | I/O                 |
| 26         | I/O                | I/O                 |
| 27         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 28         | I/O                | I/O                 |
| 29         | I/O                | I/O                 |
| 30         | I/O                | I/O                 |
| 31         | I/O                | I/O                 |
| 32         | GND                | GND                 |
| 33         | I/O                | I/O                 |
| 34         | I/O                | I/O                 |
| 35         | I/O                | I/O                 |
| 36         | I/O                | I/O                 |
| 37         | GND                | GND                 |
| 38         | I/O                | I/O                 |
| 39         | I/O                | I/O                 |
| 40         | I/O                | I/O                 |
| 41         | I/O                | I/O                 |
| 42         | I/O                | I/O                 |
| 43         | I/O                | I/O                 |
| 44         | I/O                | I/O                 |

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| 45         | I/O                | I/O                 |
| 46         | I/O                | I/O                 |
| 47         | I/O                | I/O                 |
| 48         | I/O                | I/O                 |
| 49         | I/O                | I/O                 |
| 50         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 51         | I/O                | I/O                 |
| 52         | I/O                | I/O                 |
| 53         | I/O                | I/O                 |
| 54         | I/O                | I/O                 |
| 55         | GND                | GND                 |
| 56         | I/O                | I/O                 |
| 57         | I/O                | I/O                 |
| 58         | I/O                | I/O                 |
| 59         | I/O                | I/O                 |
| 60         | I/O                | I/O                 |
| 61         | I/O                | I/O                 |
| 62         | I/O                | I/O                 |
| 63         | I/O                | I/O                 |
| 64         | I/O                | I/O                 |
| 65         | GND                | GND                 |
| 66         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 67         | I/O                | I/O                 |
| 68         | I/O                | I/O                 |
| 69         | I/O                | I/O                 |
| 70         | I/O                | I/O                 |
| 71         | I/O                | I/O                 |
| 72         | I/O                | I/O                 |
| 73         | I/O                | I/O                 |
| 74         | I/O                | I/O                 |
| 75         | GND                | GND                 |
| 76         | I/O                | I/O                 |
| 77         | I/O                | I/O                 |
| 78         | I/O                | I/O                 |
| 79         | I/O                | I/O                 |
| 80         | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 81         | I/O                | I/O                 |
| 82         | I/O                | I/O                 |
| 83         | I/O                | I/O                 |
| 84         | I/O                | I/O                 |
| 85         | I/O                | I/O                 |
| 86         | I/O                | I/O                 |
| 87         | I/O                | I/O                 |
| 88         | I/O                | I/O                 |

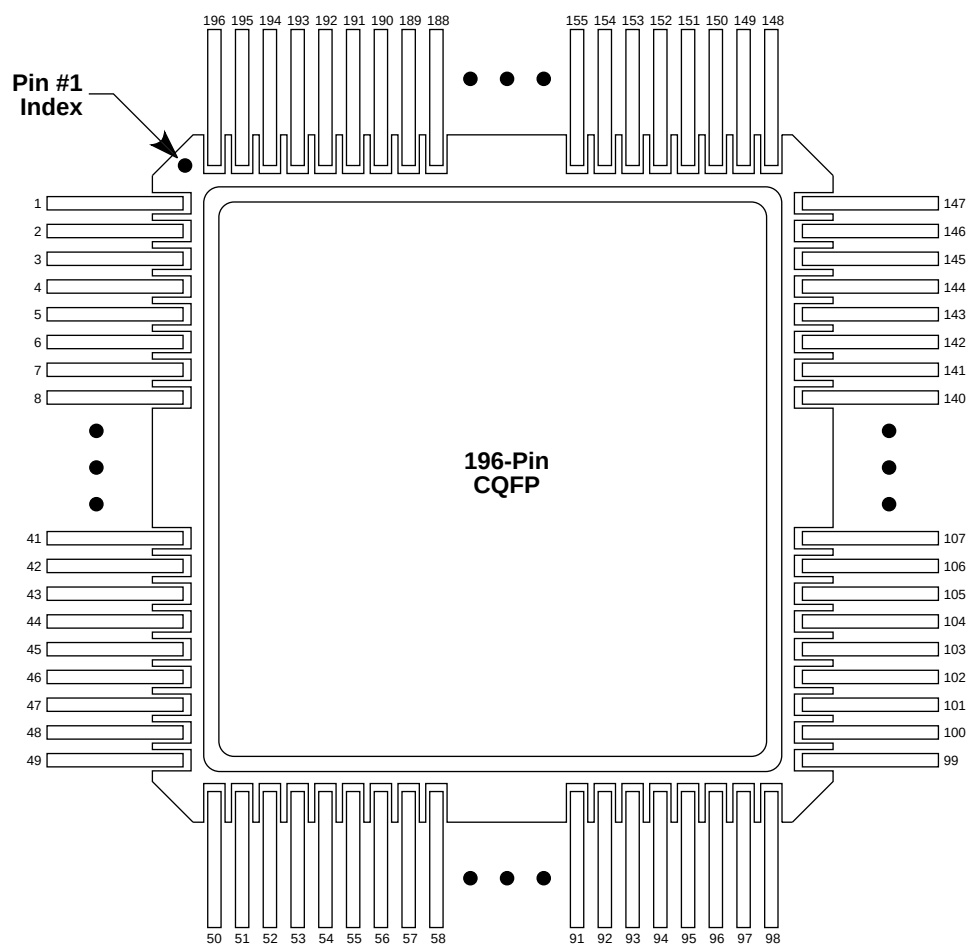
**172-Pin CQFP (Continued)**

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| 89         | I/O                | I/O                 |
| 90         | I/O                | I/O                 |
| 91         | I/O                | I/O                 |
| 92         | I/O                | I/O                 |
| 93         | I/O                | I/O                 |
| 94         | I/O                | I/O                 |
| 95         | I/O                | I/O                 |
| 96         | I/O                | I/O                 |
| 97         | I/O                | I/O                 |
| 98         | GND                | GND                 |
| 99         | I/O                | I/O                 |
| 100        | I/O                | I/O                 |
| 101        | I/O                | I/O                 |
| 102        | I/O                | I/O                 |
| 103        | GND                | GND                 |
| 104        | I/O                | I/O                 |
| 105        | I/O                | I/O                 |
| 106        | GND                | GND                 |
| 107        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 108        | GND                | GND                 |
| 109        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 110        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 111        | I/O                | I/O                 |
| 112        | I/O                | I/O                 |
| 113        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 114        | I/O                | I/O                 |
| 115        | I/O                | I/O                 |
| 116        | I/O                | I/O                 |
| 117        | I/O                | I/O                 |
| 118        | GND                | GND                 |
| 119        | I/O                | I/O                 |
| 120        | I/O                | I/O                 |
| 121        | I/O                | I/O                 |
| 122        | I/O                | I/O                 |
| 123        | GND                | GND                 |
| 124        | I/O                | I/O                 |
| 125        | I/O                | I/O                 |
| 126        | I/O                | I/O                 |
| 127        | I/O                | I/O                 |
| 128        | I/O                | I/O                 |
| 129        | I/O                | I/O                 |
| 130        | I/O                | I/O                 |

| Pin Number | A1280A<br>Function | A1280XL<br>Function |
|------------|--------------------|---------------------|
| 131        | SDI, I/O           | SDI, I/O            |
| 132        | I/O                | I/O                 |
| 133        | I/O                | I/O                 |
| 134        | I/O                | I/O                 |
| 135        | I/O                | I/O                 |
| 136        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 137        | I/O                | I/O                 |
| 138        | I/O                | I/O                 |
| 139        | I/O                | I/O                 |
| 140        | I/O                | I/O                 |
| 141        | GND                | GND                 |
| 142        | I/O                | I/O                 |
| 143        | I/O                | I/O                 |
| 144        | I/O                | I/O                 |
| 145        | I/O                | I/O                 |
| 146        | I/O                | I/O                 |
| 147        | I/O                | I/O                 |
| 148        | PRA, I/O           | PRA, I/O            |
| 149        | I/O                | I/O                 |
| 150        | CLKA, I/O          | CLKA, I/O           |
| 151        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 152        | GND                | GND                 |
| 153        | I/O                | I/O                 |
| 154        | CLKB, I/O          | CLKB, I/O           |
| 155        | I/O                | I/O                 |
| 156        | PRB, I/O           | PRB, I/O            |
| 157        | I/O                | I/O                 |
| 158        | I/O                | I/O                 |
| 159        | I/O                | I/O                 |
| 160        | I/O                | I/O                 |
| 161        | GND                | GND                 |
| 162        | I/O                | I/O                 |
| 163        | I/O                | I/O                 |
| 164        | I/O                | I/O                 |
| 165        | I/O                | I/O                 |
| 166        | V <sub>CC</sub>    | V <sub>CC</sub>     |
| 167        | I/O                | I/O                 |
| 168        | I/O                | I/O                 |
| 169        | I/O                | I/O                 |
| 170        | I/O                | I/O                 |
| 171        | DCLK, I/O          | DCLK, I/O           |
| 172        | I/O                | I/O                 |

## Package Pin Assignments (continued)

### 196-Pin CQFP (Top View)



**196-Pin CQFP**

| Pin Number | A1460A Function |
|------------|-----------------|
| 1          | GND             |
| 2          | SDI, I/O        |
| 3          | I/O             |
| 4          | I/O             |
| 5          | I/O             |
| 6          | I/O             |
| 7          | I/O             |
| 8          | I/O             |
| 9          | I/O             |
| 10         | I/O             |
| 11         | MODE            |
| 12         | V <sub>CC</sub> |
| 13         | GND             |
| 14         | I/O             |
| 15         | I/O             |
| 16         | I/O             |
| 17         | I/O             |
| 18         | I/O             |
| 19         | I/O             |
| 20         | I/O             |
| 21         | I/O             |
| 22         | I/O             |
| 23         | I/O             |
| 24         | I/O             |
| 25         | I/O             |
| 26         | I/O             |
| 27         | I/O             |
| 28         | I/O             |
| 29         | I/O             |
| 30         | I/O             |
| 31         | I/O             |
| 32         | I/O             |
| 33         | I/O             |
| 34         | I/O             |
| 35         | I/O             |
| 36         | I/O             |
| 37         | GND             |
| 38         | V <sub>CC</sub> |
| 39         | V <sub>CC</sub> |
| 40         | I/O             |
| 41         | I/O             |
| 42         | I/O             |
| 43         | I/O             |

| Pin Number | A1460A Function |
|------------|-----------------|
| 44         | I/O             |
| 45         | I/O             |
| 46         | I/O             |
| 47         | I/O             |
| 48         | I/O             |
| 49         | I/O             |
| 50         | I/O             |
| 51         | GND             |
| 52         | GND             |
| 53         | I/O             |
| 54         | I/O             |
| 55         | I/O             |
| 56         | I/O             |
| 57         | I/O             |
| 58         | I/O             |
| 59         | V <sub>CC</sub> |
| 60         | I/O             |
| 61         | I/O             |
| 62         | I/O             |
| 63         | I/O             |
| 64         | GND             |
| 65         | I/O             |
| 66         | I/O             |
| 67         | I/O             |
| 68         | I/O             |
| 69         | I/O             |
| 70         | I/O             |
| 71         | I/O             |
| 72         | I/O             |
| 73         | I/O             |
| 74         | I/O             |
| 75         | PRB, I/O        |
| 76         | I/O             |
| 77         | HCLK, I/O       |
| 78         | I/O             |
| 79         | I/O             |
| 80         | I/O             |
| 81         | I/O             |
| 82         | I/O             |
| 83         | I/O             |
| 84         | I/O             |
| 85         | I/O             |
| 86         | GND             |

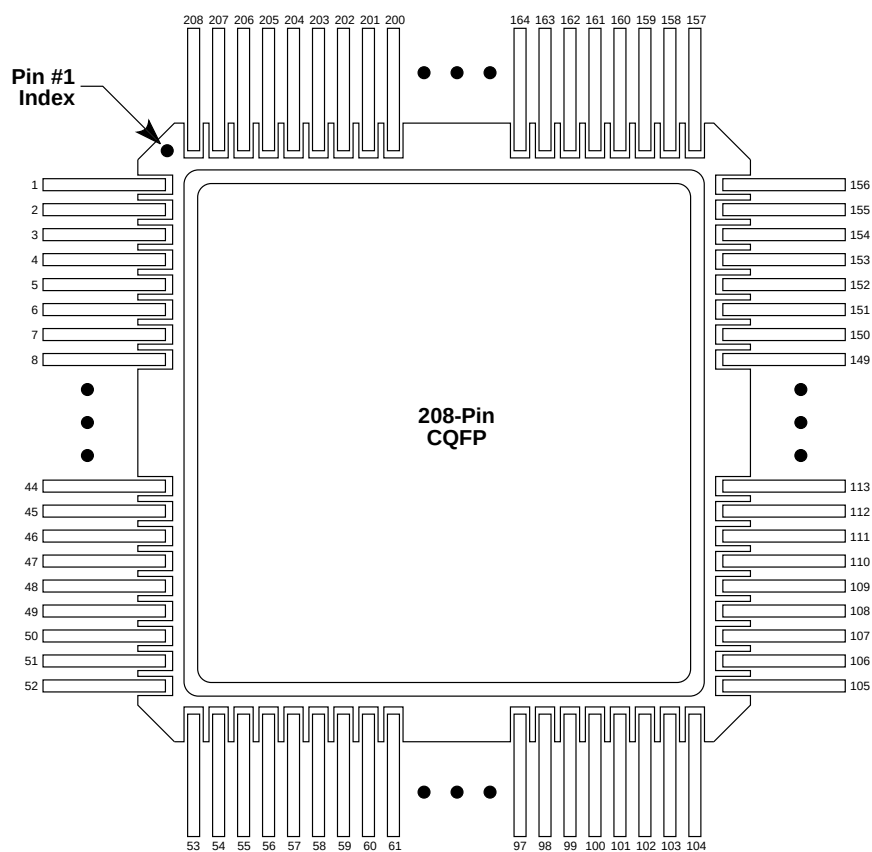
| Pin Number | A1460A Function |
|------------|-----------------|
| 87         | I/O             |
| 88         | I/O             |
| 89         | I/O             |
| 90         | I/O             |
| 91         | I/O             |
| 92         | I/O             |
| 93         | I/O             |
| 94         | V <sub>CC</sub> |
| 95         | I/O             |
| 96         | I/O             |
| 97         | I/O             |
| 98         | GND             |
| 99         | I/O             |
| 100        | IOPCL, I/O      |
| 101        | GND             |
| 102        | I/O             |
| 103        | I/O             |
| 104        | I/O             |
| 105        | I/O             |
| 106        | I/O             |
| 107        | I/O             |
| 108        | I/O             |
| 109        | I/O             |
| 110        | V <sub>CC</sub> |
| 111        | V <sub>CC</sub> |
| 112        | GND             |
| 113        | I/O             |
| 114        | I/O             |
| 115        | I/O             |
| 116        | I/O             |
| 117        | I/O             |
| 118        | I/O             |
| 119        | I/O             |
| 120        | I/O             |
| 121        | I/O             |
| 122        | I/O             |
| 123        | I/O             |
| 124        | I/O             |
| 125        | I/O             |
| 126        | I/O             |
| 127        | I/O             |
| 128        | I/O             |
| 129        | I/O             |

**196-Pin CQFP (Continued)**

| Pin Number | A1460A Function |
|------------|-----------------|
| 130        | I/O             |
| 131        | I/O             |
| 132        | I/O             |
| 133        | I/O             |
| 134        | I/O             |
| 135        | I/O             |
| 136        | I/O             |
| 137        | V <sub>CC</sub> |
| 138        | GND             |
| 139        | GND             |
| 140        | V <sub>CC</sub> |
| 141        | I/O             |
| 142        | I/O             |
| 143        | I/O             |
| 144        | I/O             |
| 145        | I/O             |
| 146        | I/O             |
| 147        | I/O             |
| 148        | IOCLK, I/O      |
| 149        | GND             |
| 150        | I/O             |
| 151        | I/O             |
| 152        | I/O             |

| Pin Number | A1460A Function |
|------------|-----------------|
| 153        | I/O             |
| 154        | I/O             |
| 155        | V <sub>CC</sub> |
| 156        | I/O             |
| 157        | I/O             |
| 158        | I/O             |
| 159        | I/O             |
| 160        | I/O             |
| 161        | I/O             |
| 162        | GND             |
| 163        | I/O             |
| 164        | I/O             |
| 165        | I/O             |
| 166        | I/O             |
| 167        | I/O             |
| 168        | I/O             |
| 169        | I/O             |
| 170        | I/O             |
| 171        | I/O             |
| 172        | CLKA, I/O       |
| 173        | CLKB, I/O       |
| 174        | PRA, I/O        |
| 175        | I/O             |

| Pin Number | A1460A Function |
|------------|-----------------|
| 176        | I/O             |
| 177        | I/O             |
| 178        | I/O             |
| 179        | I/O             |
| 180        | I/O             |
| 181        | I/O             |
| 182        | I/O             |
| 183        | GND             |
| 184        | I/O             |
| 185        | I/O             |
| 186        | I/O             |
| 187        | I/O             |
| 188        | I/O             |
| 189        | V <sub>CC</sub> |
| 190        | I/O             |
| 191        | I/O             |
| 192        | I/O             |
| 193        | GND             |
| 194        | I/O             |
| 195        | I/O             |
| 196        | DCLK, I/O       |

**Package Pin Assignments (continued)****208-Pin CQFP (Top View)**

## 208-Pin CQFP

| Pin Number | A32100DX Function |
|------------|-------------------|
| 1          | GND               |
| 2          | V <sub>CC</sub>   |
| 3          | MODE              |
| 4          | I/O               |
| 5          | I/O               |
| 6          | I/O               |
| 7          | I/O               |
| 8          | I/O               |
| 9          | I/O               |
| 10         | I/O               |
| 11         | I/O               |
| 12         | I/O               |
| 13         | I/O               |
| 14         | I/O               |
| 15         | I/O               |
| 16         | I/O               |
| 17         | V <sub>CC</sub>   |
| 18         | I/O               |
| 19         | I/O               |
| 20         | I/O               |
| 21         | I/O               |
| 22         | GND               |
| 23         | I/O               |
| 24         | I/O               |
| 25         | I/O               |
| 26         | I/O               |
| 27         | GND               |
| 28         | V <sub>CC</sub>   |
| 29         | V <sub>CC</sub>   |
| 30         | I/O               |
| 31         | I/O               |
| 32         | V <sub>CC</sub>   |
| 33         | I/O               |
| 34         | I/O               |
| 35         | I/O               |
| 36         | I/O               |
| 37         | I/O               |
| 38         | I/O               |
| 39         | I/O               |
| 40         | I/O               |
| 41         | I/O               |
| 42         | I/O               |
| 43         | I/O               |

| Pin Number | A32100DX Function |
|------------|-------------------|
| 44         | I/O               |
| 45         | I/O               |
| 46         | I/O               |
| 47         | I/O               |
| 48         | I/O               |
| 49         | I/O               |
| 50         | I/O               |
| 51         | I/O               |
| 52         | GND               |
| 53         | GND               |
| 54         | TMS, I/O          |
| 55         | TDI, I/O          |
| 56         | I/O               |
| 57         | I/O (WD)          |
| 58         | I/O (WD)          |
| 59         | I/O               |
| 60         | V <sub>CC</sub>   |
| 61         | I/O               |
| 62         | I/O               |
| 63         | I/O               |
| 64         | I/O               |
| 65         | QCLKA, I/O        |
| 66         | I/O (WD)          |
| 67         | I/O (WD)          |
| 68         | I/O               |
| 69         | I/O               |
| 70         | I/O (WD)          |
| 71         | I/O (WD)          |
| 72         | I/O               |
| 73         | I/O               |
| 74         | I/O               |
| 75         | I/O               |
| 76         | I/O               |
| 77         | I/O               |
| 78         | GND               |
| 79         | V <sub>CC</sub>   |
| 80         | V <sub>CC</sub>   |
| 81         | I/O               |
| 82         | I/O               |
| 83         | I/O               |
| 84         | I/O               |
| 85         | I/O (WD)          |
| 86         | I/O (WD)          |

| Pin Number | A32100DX Function |
|------------|-------------------|
| 87         | I/O               |
| 88         | I/O               |
| 89         | I/O               |
| 90         | I/O               |
| 91         | QCLKB, I/O        |
| 92         | I/O               |
| 93         | I/O (WD)          |
| 94         | I/O (WD)          |
| 95         | I/O               |
| 96         | I/O               |
| 97         | I/O               |
| 98         | V <sub>CC</sub>   |
| 99         | I/O               |
| 100        | I/O (WD)          |
| 101        | I/O (WD)          |
| 102        | I/O               |
| 103        | SDO, I/O          |
| 104        | I/O               |
| 105        | GND               |
| 106        | V <sub>CC</sub>   |
| 107        | I/O               |
| 108        | I/O               |
| 109        | I/O               |
| 110        | I/O               |
| 111        | I/O               |
| 112        | I/O               |
| 113        | I/O               |
| 114        | I/O               |
| 115        | I/O               |
| 116        | I/O               |
| 117        | I/O               |
| 118        | I/O               |
| 119        | I/O               |
| 120        | I/O               |
| 121        | I/O               |
| 122        | I/O               |
| 123        | I/O               |
| 124        | I/O               |
| 125        | I/O               |
| 126        | GND               |
| 127        | I/O               |
| 128        | TCK, I/O          |
| 129        | GND               |

**208-Pin CQFP (Continued)**

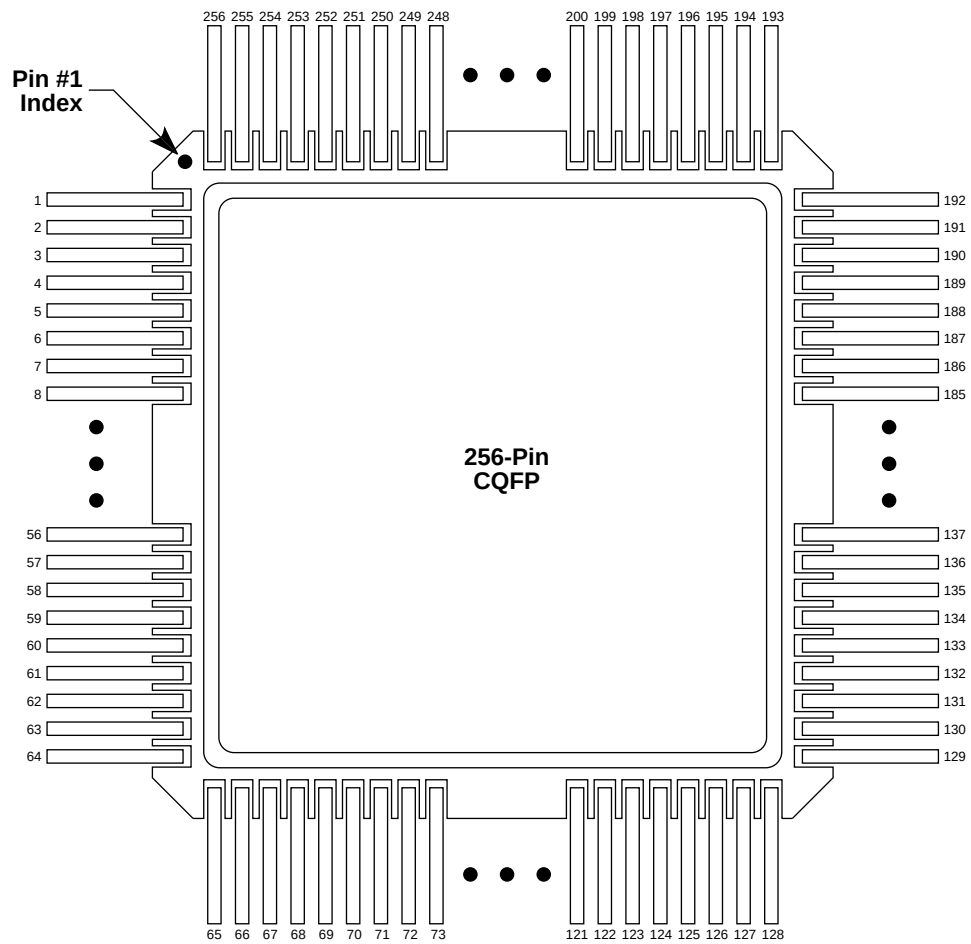
| Pin Number | A32100DX Function |
|------------|-------------------|
| 130        | V <sub>CC</sub>   |
| 131        | GND               |
| 132        | V <sub>CC</sub>   |
| 133        | V <sub>CC</sub>   |
| 134        | I/O               |
| 135        | I/O               |
| 136        | V <sub>CC</sub>   |
| 137        | I/O               |
| 138        | I/O               |
| 139        | I/O               |
| 140        | I/O               |
| 141        | I/O               |
| 142        | I/O               |
| 143        | I/O               |
| 144        | I/O               |
| 145        | I/O               |
| 146        | I/O               |
| 147        | I/O               |
| 148        | I/O               |
| 149        | I/O               |
| 150        | GND               |
| 151        | I/O               |
| 152        | I/O               |
| 153        | I/O               |
| 154        | I/O               |
| 155        | I/O               |
| 156        | I/O               |

| Pin Number | A32100DX Function |
|------------|-------------------|
| 157        | GND               |
| 158        | I/O               |
| 159        | SDI, I/O          |
| 160        | I/O               |
| 161        | I/O (WD)          |
| 162        | I/O (WD)          |
| 163        | I/O               |
| 164        | V <sub>CC</sub>   |
| 165        | I/O               |
| 166        | I/O               |
| 167        | I/O               |
| 168        | I/O (WD)          |
| 169        | I/O (WD)          |
| 170        | I/O               |
| 171        | QCLKD, I/O        |
| 172        | I/O               |
| 173        | I/O               |
| 174        | I/O               |
| 175        | I/O               |
| 176        | I/O (WD)          |
| 177        | I/O (WD)          |
| 178        | PRA, I/O          |
| 179        | I/O               |
| 180        | CLKA, I/O         |
| 181        | I/O               |
| 182        | V <sub>CC</sub>   |
| 183        | V <sub>CC</sub>   |

| Pin Number | A32100DX Function |
|------------|-------------------|
| 184        | GND               |
| 185        | I/O               |
| 186        | CLKB, I/O         |
| 187        | I/O               |
| 188        | PRB, I/O          |
| 189        | I/O               |
| 190        | I/O (WD)          |
| 191        | I/O (WD)          |
| 192        | I/O               |
| 193        | I/O               |
| 194        | I/O (WD)          |
| 195        | I/O (WD)          |
| 196        | QCLKC, I/O        |
| 197        | I/O               |
| 198        | I/O               |
| 199        | I/O               |
| 200        | I/O               |
| 201        | I/O               |
| 202        | V <sub>CC</sub>   |
| 203        | I/O (WD)          |
| 204        | I/O (WD)          |
| 205        | I/O               |
| 206        | I/O               |
| 207        | DCLK, I/O         |
| 208        | I/O               |

## Package Pin Assignments (continued)

### 256-Pin CQFP (Top View)



## 256-Pin CQFP

| Pin Number | A14100A Function | A32200DX Function |
|------------|------------------|-------------------|
| 1          | GND              | NC                |
| 2          | SDI, I/O         | GND               |
| 3          | I/O              | I/O               |
| 4          | I/O              | I/O               |
| 5          | I/O              | I/O               |
| 6          | I/O              | I/O               |
| 7          | I/O              | I/O               |
| 8          | I/O              | I/O               |
| 9          | I/O              | I/O               |
| 10         | I/O              | GND               |
| 11         | MODE             | I/O               |
| 12         | I/O              | I/O               |
| 13         | I/O              | I/O               |
| 14         | I/O              | I/O               |
| 15         | I/O              | I/O               |
| 16         | I/O              | I/O               |
| 17         | I/O              | I/O               |
| 18         | I/O              | I/O               |
| 19         | I/O              | I/O               |
| 20         | I/O              | I/O               |
| 21         | I/O              | I/O               |
| 22         | I/O              | I/O               |
| 23         | I/O              | I/O               |
| 24         | I/O              | I/O               |
| 25         | I/O              | I/O               |
| 26         | I/O              | V <sub>CC</sub>   |
| 27         | I/O              | I/O               |
| 28         | V <sub>CC</sub>  | I/O               |
| 29         | GND              | V <sub>CC</sub>   |
| 30         | V <sub>CC</sub>  | V <sub>CC</sub>   |
| 31         | GND              | GND               |
| 32         | I/O              | V <sub>CC</sub>   |
| 33         | I/O              | GND               |
| 34         | I/O              | TCK, I/O          |
| 35         | I/O              | I/O               |
| 36         | I/O              | GND               |
| 37         | I/O              | I/O               |
| 38         | I/O              | I/O               |
| 39         | I/O              | I/O               |
| 40         | I/O              | I/O               |
| 41         | I/O              | I/O               |
| 42         | I/O              | I/O               |
| 43         | I/O              | I/O               |
| 44         | I/O              | I/O               |

| Pin Number | A14100A Function | A32200DX Function |
|------------|------------------|-------------------|
| 45         | I/O              | I/O               |
| 46         | V <sub>CC</sub>  | I/O               |
| 47         | I/O              | I/O               |
| 48         | I/O              | GND               |
| 49         | I/O              | I/O               |
| 50         | I/O              | I/O               |
| 51         | I/O              | I/O               |
| 52         | I/O              | I/O               |
| 53         | I/O              | I/O               |
| 54         | I/O              | I/O               |
| 55         | I/O              | I/O               |
| 56         | I/O              | I/O               |
| 57         | I/O              | I/O               |
| 58         | I/O              | I/O               |
| 59         | GND              | I/O               |
| 60         | I/O              | V <sub>CC</sub>   |
| 61         | I/O              | GND               |
| 62         | I/O              | GND               |
| 63         | I/O              | NC                |
| 64         | I/O              | NC                |
| 65         | I/O              | NC                |
| 66         | I/O              | I/O               |
| 67         | I/O              | SDO, I/O          |
| 68         | I/O              | I/O               |
| 69         | I/O              | I/O (WD)          |
| 70         | I/O              | I/O (WD)          |
| 71         | I/O              | I/O               |
| 72         | I/O              | V <sub>CC</sub>   |
| 73         | I/O              | I/O               |
| 74         | I/O              | I/O               |
| 75         | I/O              | I/O               |
| 76         | I/O              | I/O (WD)          |
| 77         | I/O              | GND               |
| 78         | I/O              | I/O (WD)          |
| 79         | I/O              | I/O               |
| 80         | I/O              | QCLKB, I/O        |
| 81         | I/O              | I/O               |
| 82         | I/O              | I/O               |
| 83         | I/O              | I/O               |
| 84         | I/O              | I/O               |
| 85         | I/O              | I/O               |
| 86         | I/O              | I/O               |
| 87         | I/O              | I/O (WD)          |
| 88         | I/O              | I/O (WD)          |

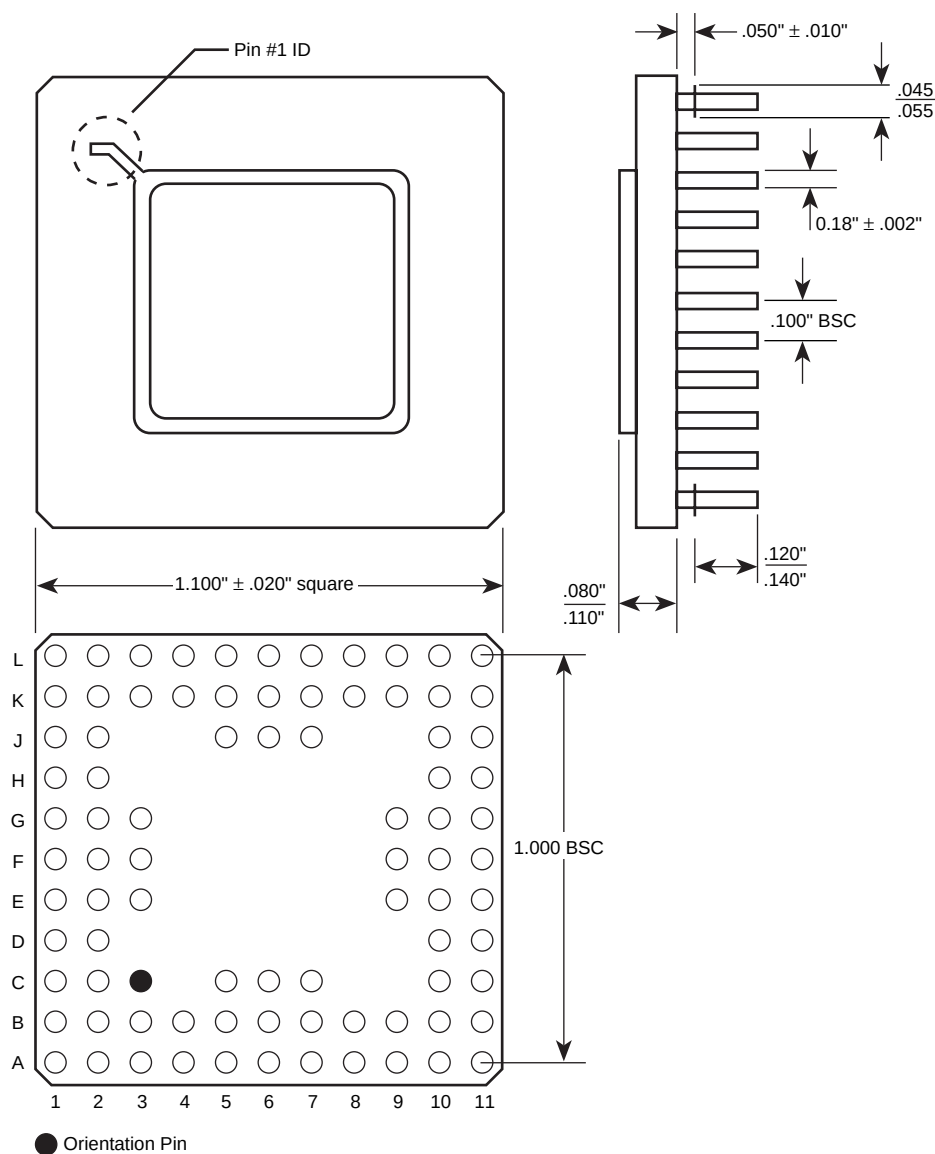
| Pin Number | A14100A Function | A32200DX Function |
|------------|------------------|-------------------|
| 89         | I/O              | I/O               |
| 90         | PRB, I/O         | I/O               |
| 91         | GND              | I/O               |
| 92         | V <sub>CC</sub>  | I/O               |
| 93         | GND              | I/O               |
| 94         | V <sub>CC</sub>  | I/O               |
| 95         | I/O              | V <sub>CC</sub>   |
| 96         | HCLK, I/O        | V <sub>CC</sub>   |
| 97         | I/O              | GND               |
| 98         | I/O              | GND               |
| 99         | I/O              | I/O               |
| 100        | I/O              | I/O               |
| 101        | I/O              | I/O               |
| 102        | I/O              | I/O               |
| 103        | I/O              | I/O               |
| 104        | I/O              | I/O               |
| 105        | I/O              | I/O (WD)          |
| 106        | I/O              | I/O (WD)          |
| 107        | I/O              | I/O               |
| 108        | I/O              | I/O               |
| 109        | I/O              | I/O (WD)          |
| 110        | GND              | I/O (WD)          |
| 111        | I/O              | I/O               |
| 112        | I/O              | QCLKA, I/O        |
| 113        | I/O              | I/O               |
| 114        | I/O              | GND               |
| 115        | I/O              | I/O               |
| 116        | I/O              | I/O               |
| 117        | I/O              | I/O               |
| 118        | I/O              | I/O               |
| 119        | I/O              | V <sub>CC</sub>   |
| 120        | I/O              | I/O               |
| 121        | I/O              | I/O (WD)          |
| 122        | I/O              | I/O (WD)          |
| 123        | I/O              | I/O               |
| 124        | I/O              | I/O               |
| 125        | I/O              | TDI, I/O          |
| 126        | I/O              | TMS, I/O          |
| 127        | IOPCL, I/O       | GND               |
| 128        | GND              | NC                |
| 129        | I/O              | NC                |
| 130        | I/O              | NC                |
| 131        | I/O              | GND               |
| 132        | I/O              | I/O               |

## 256-Pin CQFP (Continued)

| Pin Number | A14100A Function | A32200DX Function | Pin Number | A14100A Function | A32200DX Function | Pin Number | A14100A Function | A32200DX Function |
|------------|------------------|-------------------|------------|------------------|-------------------|------------|------------------|-------------------|
| 133        | I/O              | I/O               | 175        | GND              | I/O               | 217        | I/O              | I/O               |
| 134        | I/O              | I/O               | 176        | GND              | I/O               | 218        | I/O              | PRB, I/O          |
| 135        | I/O              | I/O               | 177        | I/O              | I/O               | 219        | CLKA, I/O        | I/O               |
| 136        | I/O              | I/O               | 178        | I/O              | I/O               | 220        | CLKB, I/O        | CLKB, I/O         |
| 137        | I/O              | I/O               | 179        | I/O              | I/O               | 221        | V <sub>CC</sub>  | I/O               |
| 138        | I/O              | I/O               | 180        | I/O              | GND               | 222        | GND              | GND               |
| 139        | I/O              | GND               | 181        | I/O              | I/O               | 223        | V <sub>CC</sub>  | GND               |
| 140        | I/O              | I/O               | 182        | I/O              | I/O               | 224        | GND              | V <sub>CC</sub>   |
| 141        | V <sub>CC</sub>  | I/O               | 183        | I/O              | I/O               | 225        | PRA, I/O         | V <sub>CC</sub>   |
| 142        | I/O              | I/O               | 184        | I/O              | I/O               | 226        | I/O              | I/O               |
| 143        | I/O              | I/O               | 185        | I/O              | I/O               | 227        | I/O              | CLKA, I/O         |
| 144        | I/O              | I/O               | 186        | I/O              | I/O               | 228        | I/O              | I/O               |
| 145        | I/O              | I/O               | 187        | I/O              | I/O               | 229        | I/O              | PRA, I/O          |
| 146        | I/O              | I/O               | 188        | IOCLK, I/O       | MODE              | 230        | I/O              | I/O               |
| 147        | I/O              | I/O               | 189        | GND              | V <sub>CC</sub>   | 231        | I/O              | I/O               |
| 148        | I/O              | I/O               | 190        | I/O              | GND               | 232        | I/O              | I/O (WD)          |
| 149        | I/O              | I/O               | 191        | I/O              | NC                | 233        | I/O              | I/O (WD)          |
| 150        | I/O              | I/O               | 192        | I/O              | NC                | 234        | I/O              | I/O               |
| 151        | I/O              | I/O               | 193        | I/O              | NC                | 235        | I/O              | I/O               |
| 152        | I/O              | I/O               | 194        | I/O              | I/O               | 236        | I/O              | I/O               |
| 153        | I/O              | I/O               | 195        | I/O              | DCLK, I/O         | 237        | I/O              | I/O               |
| 154        | I/O              | I/O               | 196        | I/O              | I/O               | 238        | I/O              | I/O               |
| 155        | I/O              | V <sub>CC</sub>   | 197        | I/O              | I/O               | 239        | I/O              | I/O               |
| 156        | I/O              | I/O               | 198        | I/O              | I/O               | 240        | GND              | QCLKD, I/O        |
| 157        | I/O              | I/O               | 199        | I/O              | I/O (WD)          | 241        | I/O              | I/O               |
| 158        | GND              | V <sub>CC</sub>   | 200        | I/O              | I/O (WD)          | 242        | I/O              | I/O (WD)          |
| 159        | V <sub>CC</sub>  | V <sub>CC</sub>   | 201        | I/O              | V <sub>CC</sub>   | 243        | I/O              | GND               |
| 160        | GND              | GND               | 202        | I/O              | I/O               | 244        | I/O              | I/O (WD)          |
| 161        | V <sub>CC</sub>  | I/O               | 203        | I/O              | I/O               | 245        | I/O              | I/O               |
| 162        | I/O              | I/O               | 204        | I/O              | I/O               | 246        | I/O              | I/O               |
| 163        | I/O              | I/O               | 205        | I/O              | I/O               | 247        | I/O              | I/O               |
| 164        | I/O              | I/O               | 206        | I/O              | GND               | 248        | I/O              | V <sub>CC</sub>   |
| 165        | I/O              | GND               | 207        | I/O              | I/O               | 249        | I/O              | I/O               |
| 166        | I/O              | I/O               | 208        | I/O              | I/O               | 250        | I/O              | I/O (WD)          |
| 167        | I/O              | I/O               | 209        | I/O              | QCLKC, I/O        | 251        | I/O              | I/O (WD)          |
| 168        | I/O              | I/O               | 210        | I/O              | I/O               | 252        | I/O              | I/O               |
| 169        | I/O              | I/O               | 211        | I/O              | I/O (WD)          | 253        | I/O              | SDI, I/O          |
| 170        | I/O              | V <sub>CC</sub>   | 212        | I/O              | I/O (WD)          | 254        | I/O              | I/O               |
| 171        | I/O              | I/O               | 213        | I/O              | I/O               | 255        | I/O              | GND               |
| 172        | I/O              | I/O               | 214        | I/O              | I/O               | 256        | DCLK, I/O        | NC                |
| 173        | I/O              | I/O               | 215        | I/O              | I/O (WD)          |            |                  |                   |
| 174        | V <sub>CC</sub>  | I/O               | 216        | I/O              | I/O (WD)          |            |                  |                   |

## Package Mechanical Drawings

### 84-Pin CPGA

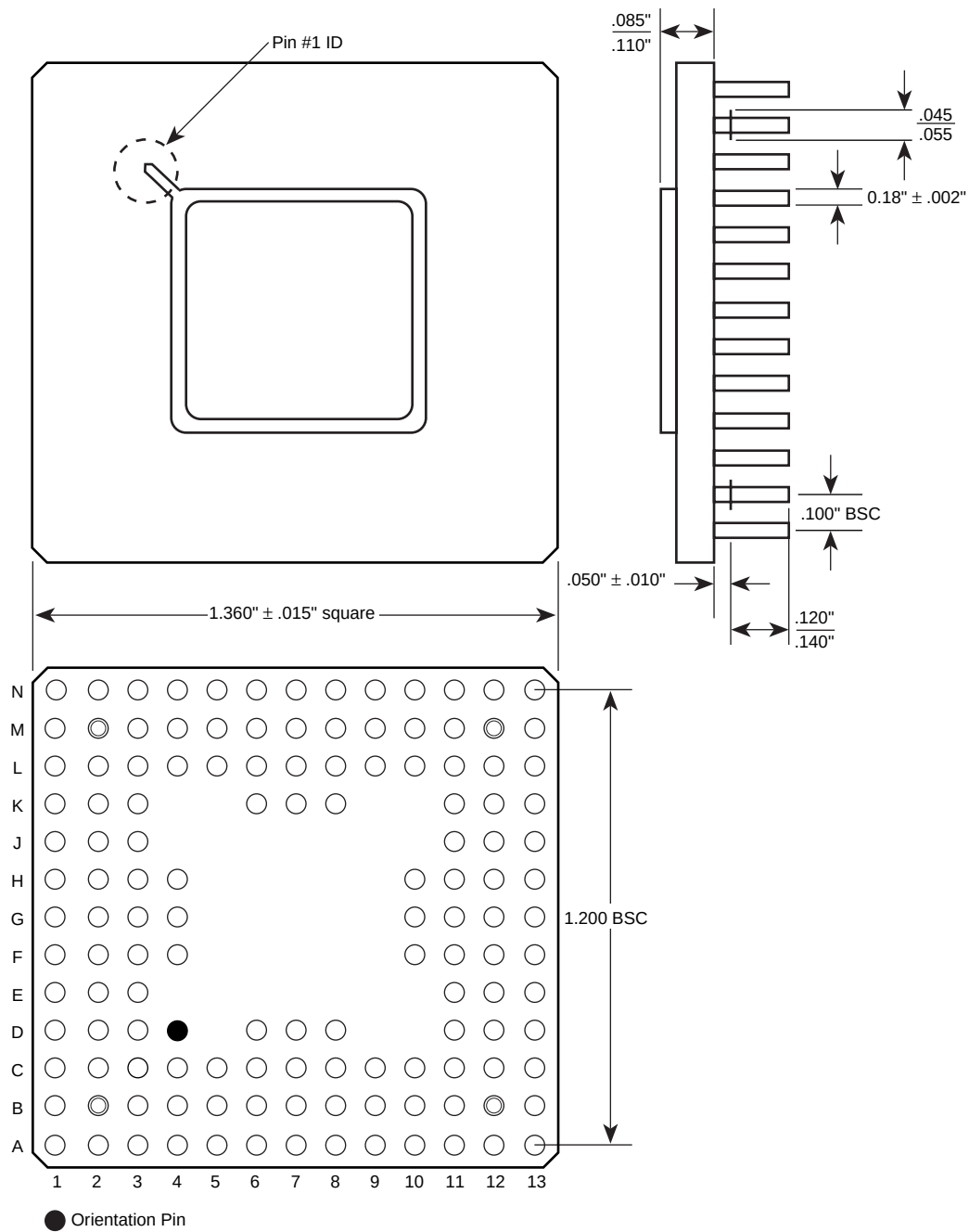


#### Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

## Package Mechanical Drawings (continued)

### 132-Pin CPGA

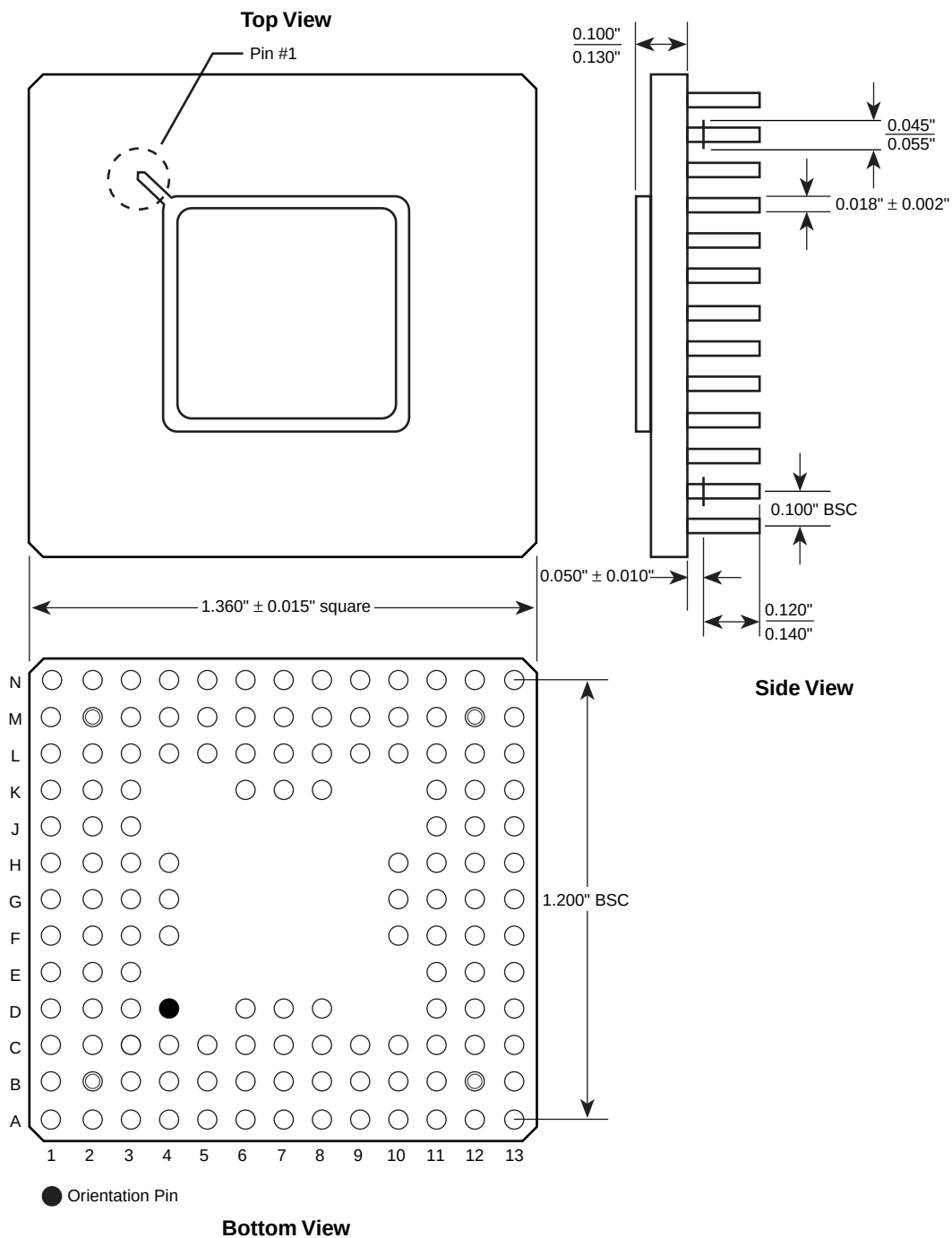


#### Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

## Package Mechanical Drawings (continued)

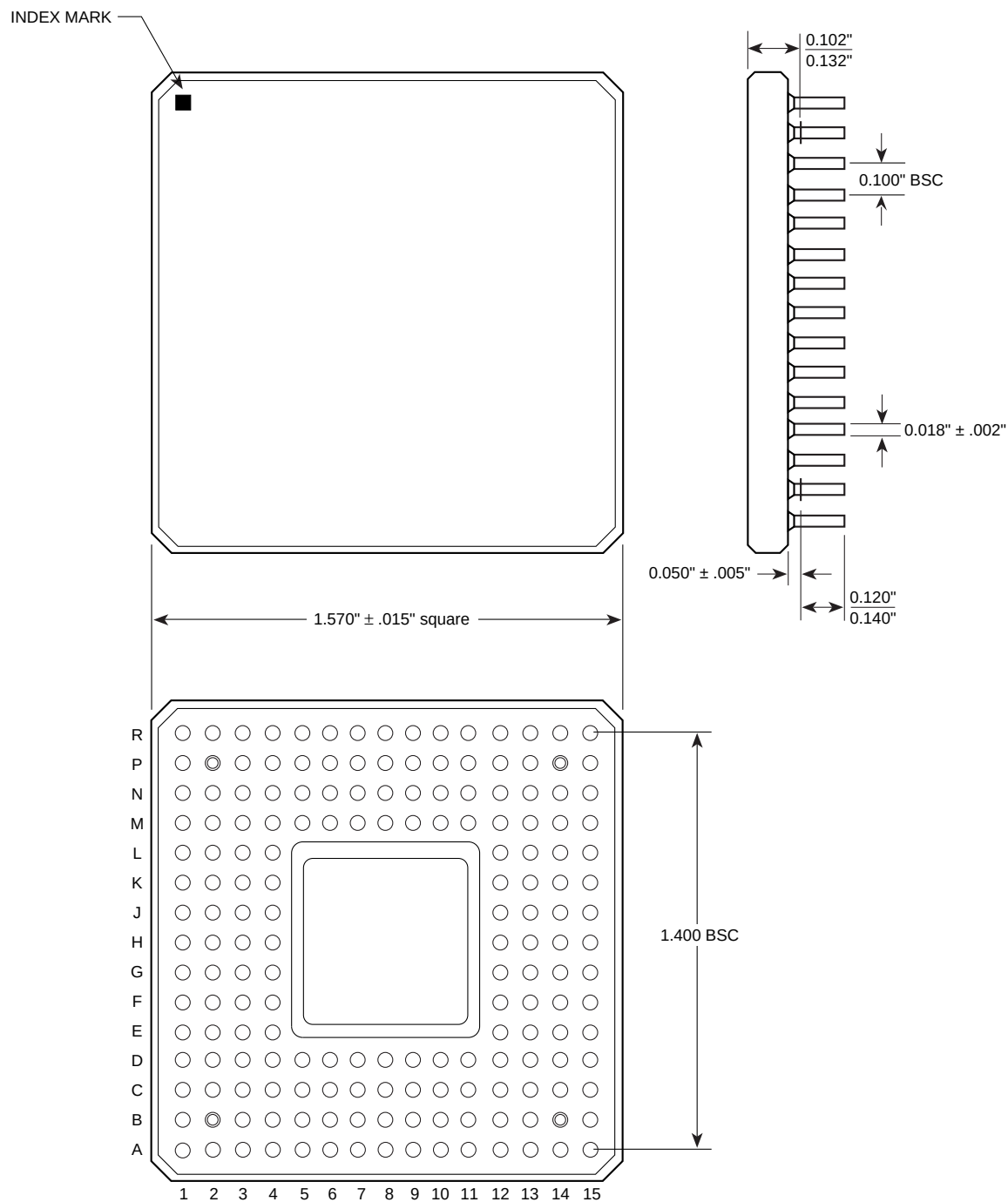
## 133-Pin CPGA

**Notes:**

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

## Package Mechanical Drawings (continued)

### 176-Pin CPGA

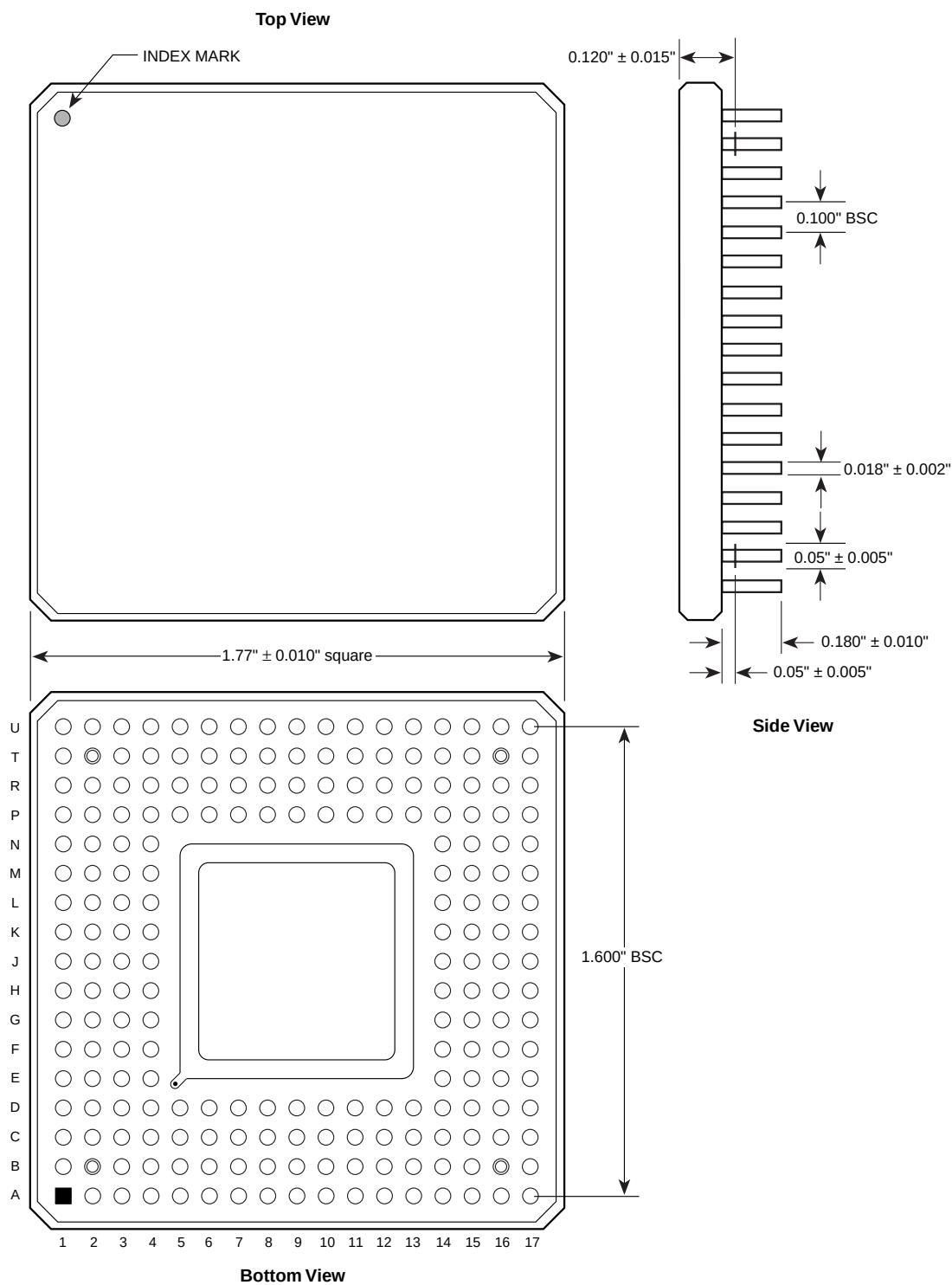


#### Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

## Package Mechanical Drawings (continued)

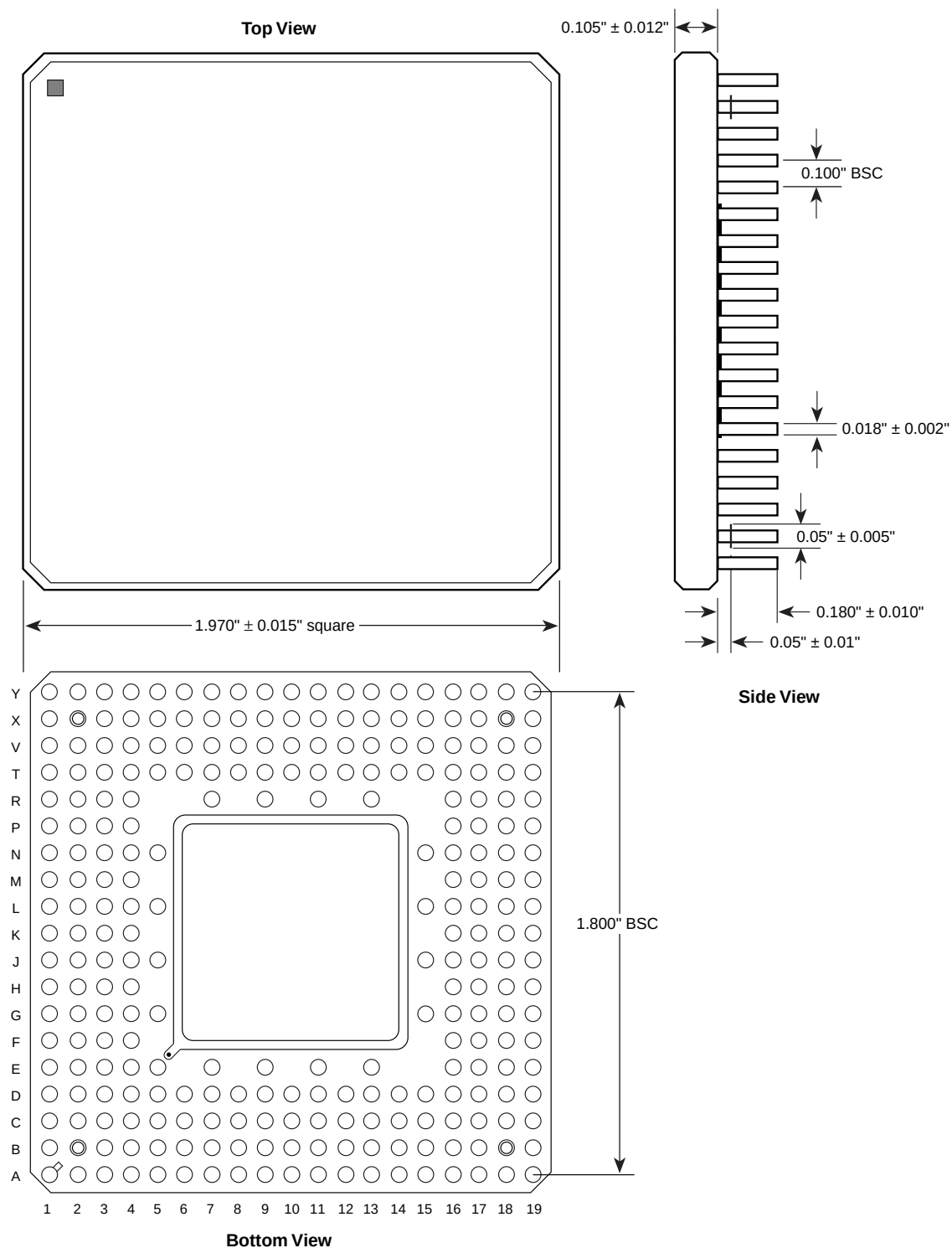
## 207-Pin CPGA

**Notes:**

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

## Package Mechanical Drawings (continued)

### 257-Pin CPGA

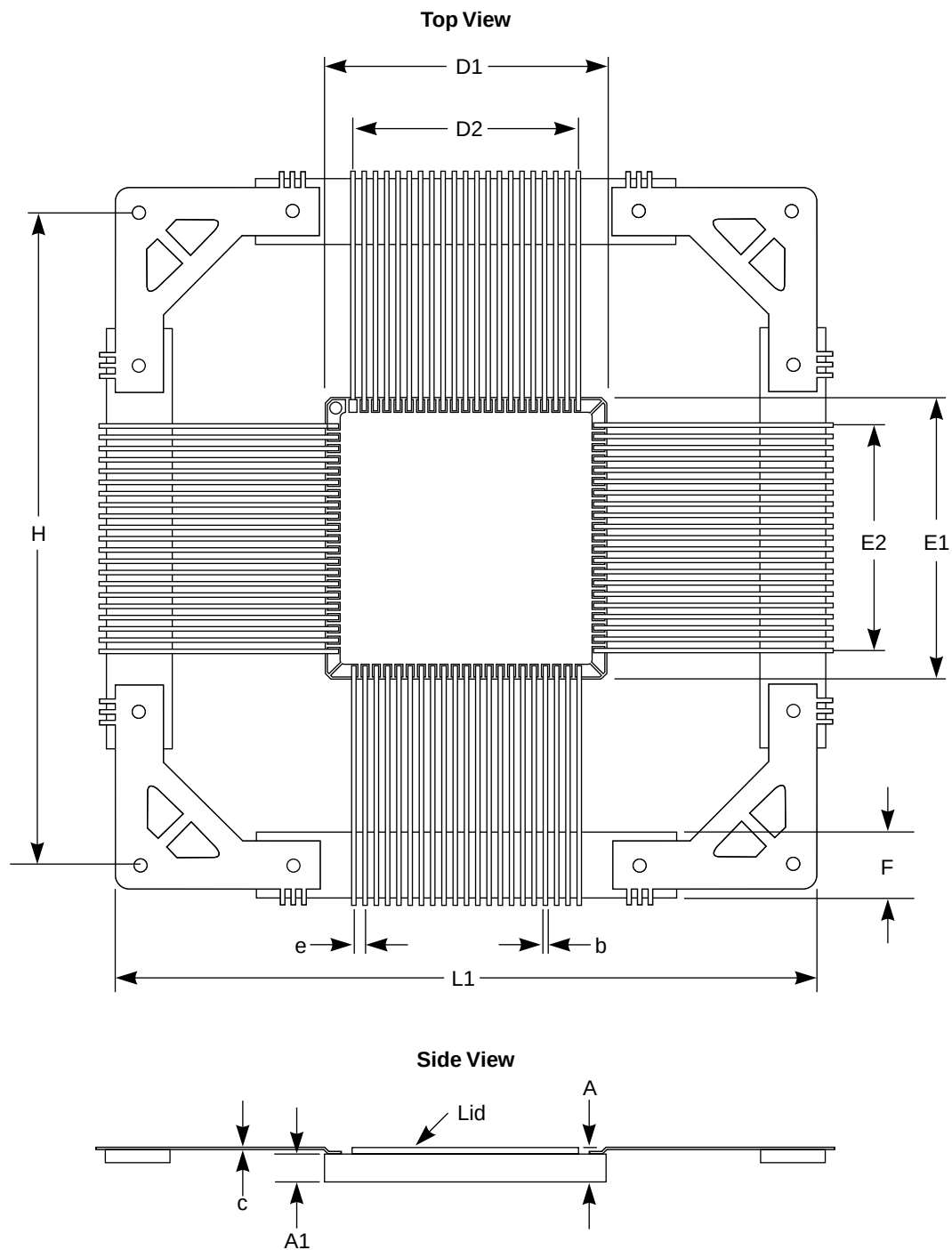


#### Notes:

1. All dimensions are in inches unless otherwise stated.
2. BSC—Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

## Package Mechanical Drawings (continued)

### 84-Pin CQFP

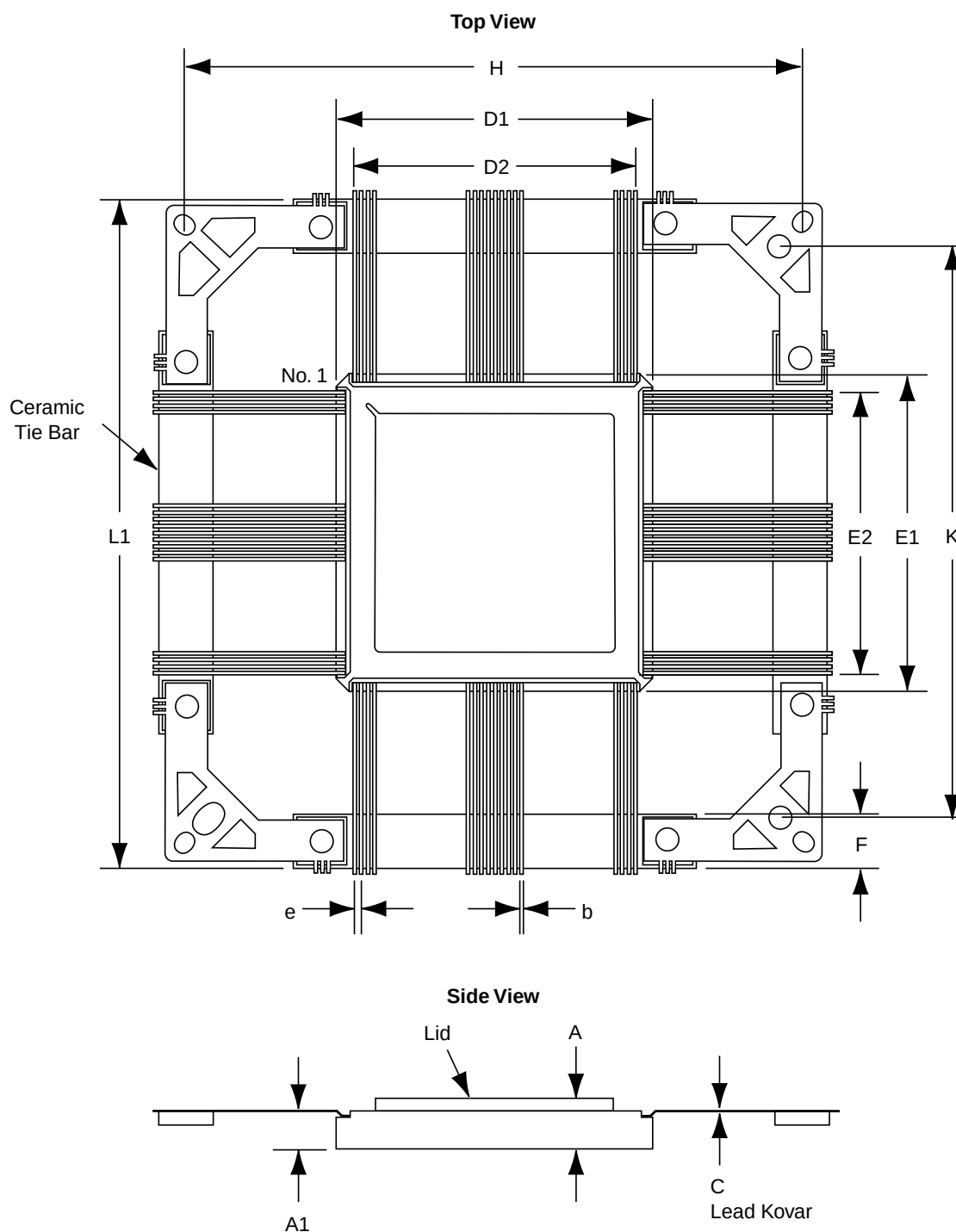


#### Notes:

1. Seal ring and lid are connected to Ground.
2. Lead material is Kovar with minimum 50 microinches gold plate over nickel.
3. Packages are shipped unformed with the ceramic tie bar in a test carrier.

## Package Mechanical Drawings (continued)

### 132-Pin, 172-Pin, 196-Pin, 208-Pin, and 256-Pin CQFP (Cavity Up)



#### Notes:

1. Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.
2. Seal ring and lid are connected to Ground.
3. Lead material is Kovar with minimum 50 microinches gold plate over nickel.
4. Packages are shipped unformed with the ceramic tie bar.
5. 32200DX – CQ208 has a heat sink on the back.

**CQFP (Ceramic Quad Flat Pack)**

|        | CQFP 84   |       |       | CQFP 132  |       |       | CQFP 172  |       |       | CQFP 196  |       |       |
|--------|-----------|-------|-------|-----------|-------|-------|-----------|-------|-------|-----------|-------|-------|
| Symbol | Min.      | Nom.  | Max.  | Min.      | Nom.  | Max.  | Min.      | Nom.  | Max.  | Min.      | Nom.  | Max.  |
| A      | 0.070     | 0.090 | 0.100 | 0.094     | 0.105 | 0.116 | 0.094     | 0.105 | 0.116 | 0.094     | 0.105 | 0.116 |
| A1     | 0.060     | 0.075 | 0.080 | 0.080     | 0.090 | 0.100 | 0.080     | 0.090 | 0.100 | 0.080     | 0.090 | 0.100 |
| b      | 0.008     | 0.010 | 0.012 | 0.007     | 0.008 | 0.010 | 0.007     | 0.008 | 0.010 | 0.007     | 0.008 | 0.010 |
| c      | 0.004     | 0.006 | 0.008 | 0.004     | 0.006 | 0.008 | 0.004     | 0.006 | 0.008 | 0.004     | 0.006 | 0.008 |
| D1/E1  | 0.640     | 0.650 | 0.660 | 0.940     | 0.950 | 0.960 | 1.168     | 1.180 | 1.192 | 1.336     | 1.350 | 1.364 |
| D2/E2  | 0.500 BSC |       |       | 0.800 BSC |       |       | 1.050 BSC |       |       | 1.200 BSC |       |       |
| e      | 0.025 BSC |       |       | 0.025 BSC |       |       | 0.025 BSC |       |       | 0.025 BSC |       |       |
| F      | 0.130     | 0.140 | 0.150 | 0.325     | 0.350 | 0.375 | 0.175     | 0.200 | 0.225 | 0.175     | 0.200 | 0.225 |
| H      | 1.460 BSC |       |       | 2.320 BSC |       |       | 2.320 BSC |       |       | 2.320 BSC |       |       |
| K      | —         |       |       | 2.140 BSC |       |       | 2.140 BSC |       |       | 2.140 BSC |       |       |
| L1     | 1.595     | 1.600 | 1.615 | 2.485     | 2.500 | 2.505 | 2.485     | 2.495 | 2.505 | 2.485     | 2.495 | 2.505 |

**Note:**

1. All dimensions are in inches except CQ208 and CQ256, which are in millimeters.
2. BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

**CQFP (Ceramic Quad Flat Pack)**

|        | CQFP 208  |       |       | CQFP 256  |       |       |
|--------|-----------|-------|-------|-----------|-------|-------|
| Symbol | Min.      | Nom.  | Max.  | Min.      | Nom.  | Max.  |
| A      | 2.78      | 3.17  | 3.56  | 2.28      | 2.67  | 3.06  |
| A1     | 2.43      | 2.79  | 3.15  | 1.93      | 2.29  | 2.65  |
| b      | 0.18      | 0.20  | 0.22  | 0.18      | 0.20  | 0.22  |
| c      | 0.11      | 0.15  | 0.17  | 0.11      | 0.15  | 0.18  |
| D1/E1  | 28.96     | 29.21 | 29.46 | 35.64     | 36.00 | 36.36 |
| D2/E2  | 25.5 BSC  |       |       | 31.5 BSC  |       |       |
| e      | 0.50 BSC  |       |       | 0.50 BSC  |       |       |
| F      | 7.05      | 7.75  | 8.45  | 7.05      | 7.75  | 8.45  |
| H      | 70.00 BSC |       |       | 70.00 BSC |       |       |
| K      | 65.90 BSC |       |       | 65.90 BSC |       |       |
| L1     | 74.60     | 75.00 | 75.40 | 74.60     | 75.00 | 75.40 |

**Note:**

1. All dimensions are in inches except CQ208 and CQ256, which are in millimeters.
2. BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.

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<http://www.actel.com>

**Actel Europe Ltd.**

Daneshill House, Lutyens Close  
Basingstoke, Hampshire RG24 8AG  
United Kingdom

**Tel:** +44-(0)125-630-5600

**Fax:** +44-(0)125-635-5420

**Actel Corporation**

955 East Arques Avenue  
Sunnyvale, California 94086  
USA

**Tel:** (408) 739-1010

**Fax:** (408) 739-1540

**Actel Asia-Pacific**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150 Japan

**Tel:** +81-(0)3-3445-7671

**Fax:** +81-(0)3-3445-7668