

DS30EA101 0.15 to 3.125 Gbps Adaptive Cable Equalizer

Check for Samples: [DS30EA101](#)

FEATURES

- Automatic Equalization of Coaxial and Twisted Pair Cables
- Data Rates from 150 Mbps to 3.125 Gbps
- Supports SD and HD Video Resolutions
- Power Consumption: 115 mW Typical
- Industrial Temperature Range: -40°C to +85°C

APPLICATIONS

- Cable Extension
- Data Recovery Equalization
- Security and Surveillance

DESCRIPTION

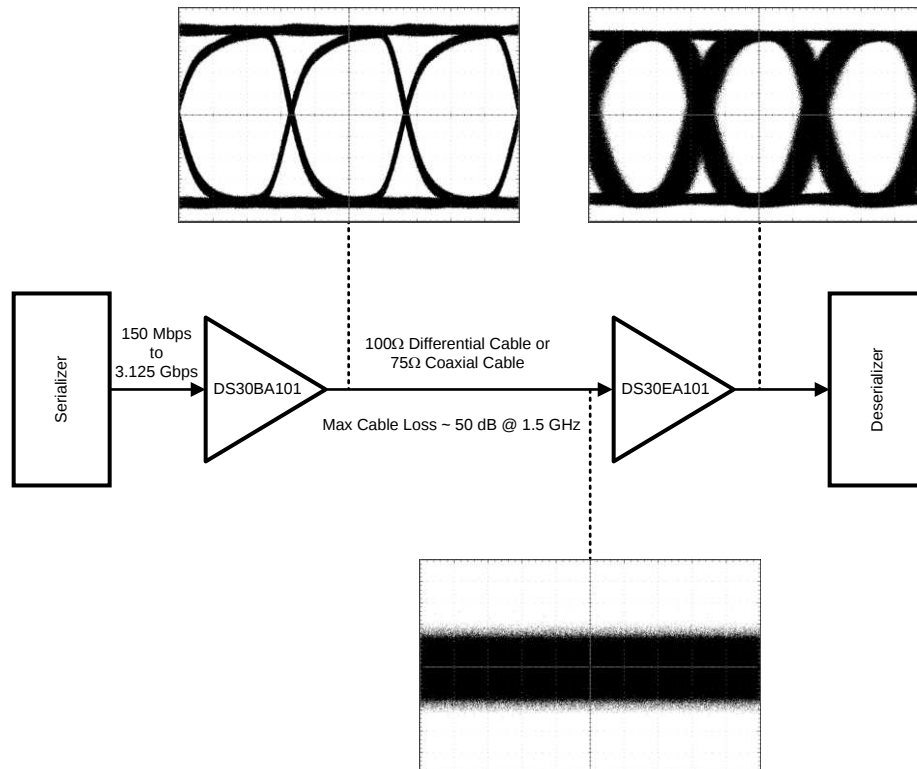
The DS30EA101 is an adaptive cable equalizer optimized for equalizing data transmitted over copper cables. The equalizer operates over a range of data rates from 150 Mbps to 3.125 Gbps and automatically adapts to equalize signals sent over any cable length from zero meters to lengths that attenuate the signal by 50 dB at 1.5 GHz.

The DS30EA101 allows either single-ended or differential input. This enables equalization of signals over coaxial cables as well as twisted pair cables.

Additional features include an LOS detect and output enable which, when tied together, disable the output when no input signal is present.

The DS30EA101 is powered from a single 2.5V supply and consumes 115 mW (typical). It operates over the full industrial temperature range of -40°C to +85°C and is available in a 4 x 4 mm 16-pin WQFN package.

Typical Application



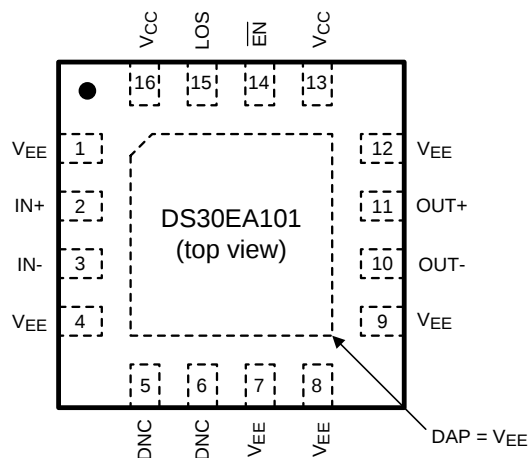
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Connection Diagram



The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

Figure 1. 16-Pin WQFN Package
See Package Number RUM0016A

PIN DESCRIPTIONS

Pin	Name	I/O, Type	Description
1	V _{EE}	Ground	Negative power supply (ground).
2	IN+	I, Data	Non-inverting input.
3	IN-	I, Data	Inverting input.
4	V _{EE}	Ground	Negative power supply (ground).
5	DNC	N/A	Do not connect – leave open.
6	DNC	N/A	Do not connect – leave open.
7	V _{EE}	Ground	Negative power supply (ground).
8	V _{EE}	Ground	Negative power supply (ground).
9	V _{EE}	Ground	Negative power supply (ground).
10	OUT-	O, LVDS	Inverting output.
11	OUT+	O, LVDS	Non-inverting output.
12	V _{EE}	Ground	Negative power supply (ground).
13	V _{CC}	Power	Positive power supply (+2.5V).
14	$\overline{\text{EN}}$	I, LVCMOS	Output enable. LOS may be tied to this pin to inhibit the output when no input signal is present. This pin has an internal pulldown. H = Outputs disabled. L = Outputs enabled.
15	LOS	O, LVCMOS	Loss of signal. H = No input signal detected. L = Input signal detected.
16	V _{CC}	Power	Positive power supply (+2.5V).
DAP	V _{EE}	Ground	Connect exposed DAP to negative power supply (ground).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage	3.1V
Input Voltage (all inputs)	-0.3V to $V_{CC}+0.3V$
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+125°C
Package Thermal Resistance θ_{JA} 16-pin WQFN θ_{JC} 16-pin WQFN	+40°C/W +6°C/W
ESD Rating (HBM)	$\geq \pm 6$ kV
ESD Rating (MM)	$\geq \pm 300V$
ESD Rating (CDM)	$\geq \pm 2$ kV

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.5V $\pm 5\%$
Input Coupling Capacitance	1.0 μF
Operating Free Air Temperature (T_A)	-40°C to +85°C

DC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.⁽¹⁾⁽²⁾

Parameter		Test Conditions	Reference	Min	Typ	Max	Units
V_{IN}	Input Voltage	0m cable length	IN+, IN-	720	800	880	mV _{P-P}
V_{SS}	Steady State Differential Output Voltage	100 Ω load, Figure 2	OUT+, OUT-	500	700	900	mV _{P-P}
V_{OD}	Differential Output Voltage			250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States					50	mV
V_{OS}	Offset Voltage			1.1	1.2	1.35	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States					50	mV
I_{OS}	Output Short Circuit Current					30	mA
V_{IH}	Input Voltage High Level		$\overline{EN}$	1.7		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.7	V
V_{OH}	Output Voltage High Level	$I_{OH} = -2$ mA	LOS	2.0			V
V_{OL}	Output Voltage Low Level	$I_{OL} = +2$ mA				0.2	V
I_{CC}	Supply Current				45	65	mA

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms at $V_{CC} = +2.5V$, $T_A = +25^\circ C$, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.

AC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.⁽¹⁾⁽²⁾

Parameter		Test Conditions	Reference	Min	Typ	Max	Units
DR _{IN}	Input Data Rate		IN+, IN-	150		3125	Mbps
t _{JIT}	Total Jitter at BER 10 ⁻¹² ⁽³⁾	3.125 Gbps, 0-10 meters CAT6			0.35		UI
		2.5 Gbps, 0-25 meters CAT6			0.35		UI
		1.5 Gbps, 0-50 meters CAT6			0.35		UI
		3.125 Gbps, 0-100 meters RG59			0.3		UI
		2.5 Gbps, 0-110 meters RG59			0.35		UI
		1.5 Gbps, 0-120 meters RG59			0.2		UI
t _{TLH}	Transition Time Low to High	20% - 80%, 100Ω load, ⁽⁴⁾ , Figure 2	OUT+, OUT-		90	130	ps
t _{THL}	Transition Time High to Low				90	130	ps

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms at V_{CC} = +2.5V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.
- (3) The total jitter at BER 10⁻¹² is calculated as DJ + (14 × RJ), where DJ is deterministic jitter and RJ is random jitter. The jitter is expressed as a portion of the unit interval (UI). The UI is the reciprocal of the data rate.
- (4) Specification is ensured by characterization and is not tested in production.

TIMING DIAGRAMS

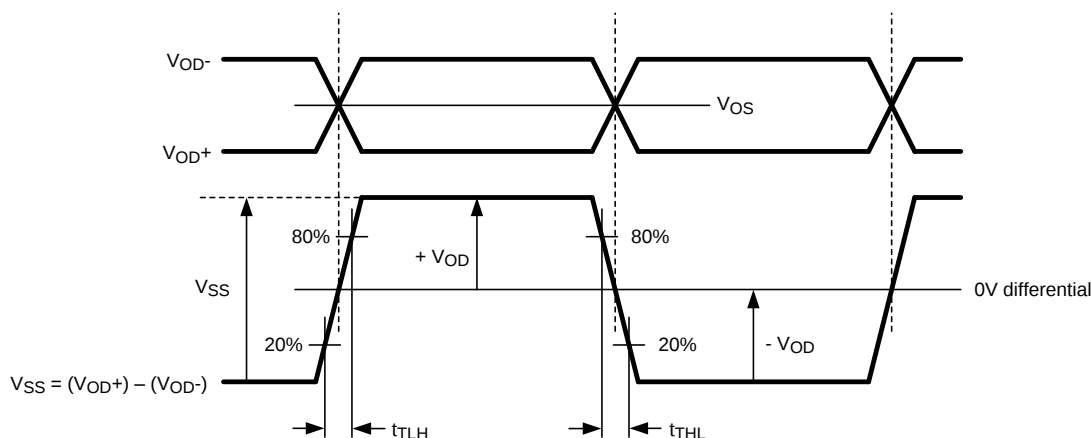


Figure 2. LVDS Output Voltage, Offset, and Timing Parameters

DEVICE OPERATION

The DS30EA101 equalizes data transmitted over copper cables. It automatically adjusts its gain to reverse the effects of the cable loss and restore the original signal. For proper operation, the launch amplitude of the signal going into the cable (the signal amplitude prior to the cable attenuation) must be set appropriately. If the signal is single-ended, its single-ended amplitude must be 800 mV_{P-P} ±10%. If the signal is differential, its differential amplitude must be 800 mV_{P-P} ±10% (400 mV_{P-P} single-ended).

INPUT INTERFACING

The DS30EA101 accepts either differential or single-ended input. The input must be AC coupled. Figure 3 and Figure 4 show the typical configurations for differential input and single-ended input, respectively. For single-ended input, the unused input must be properly terminated as shown.

OUTPUT INTERFACING

The DS30EA101 output signals (OUT+ and OUT-) are internally terminated 100Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

LOS AND $\overline{\text{EN}}$

LOS indicates the loss of signal at the DS30EA101 input. LOS is high when no input signal is present and low when a valid input signal is detected.

$\overline{\text{EN}}$ can be used to manually disable or enable the OUT+ and OUT- output signals. Applying a high input to $\overline{\text{EN}}$ will disable the DS30EA101 outputs by forcing the output to a logic 1, and applying a low input to $\overline{\text{EN}}$ will force the outputs to be active. $\overline{\text{EN}}$ has an internal pulldown to enable the outputs by default.

LOS and $\overline{\text{EN}}$ may be tied together to automatically disable the DS30EA101 outputs when no input signal is present.

APPLICATION INFORMATION

CABLE EXTENDER APPLICATION

The DS30EA101 together with the DS30BA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and FPGAs over 100Ω differential cables and 75Ω coaxial cables. Setting the correct DS30BA101 output amplitude and proper cable termination are essential for optimal operation. Figure 3 shows the recommended chipset configuration for 100Ω differential cable and Figure 4 shows the recommended chipset configuration for 75Ω coaxial cable.

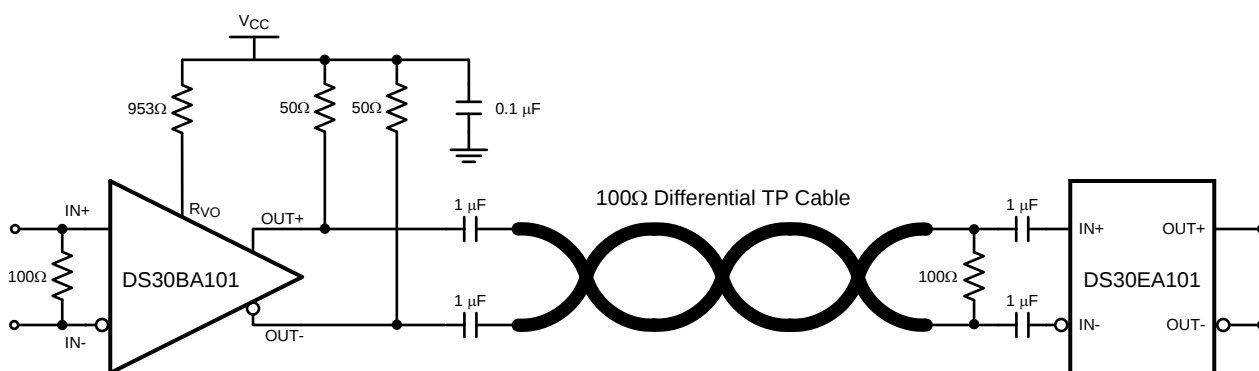


Figure 3. Cable Extender Chipset Application Circuit for 100Ω Differential Cable

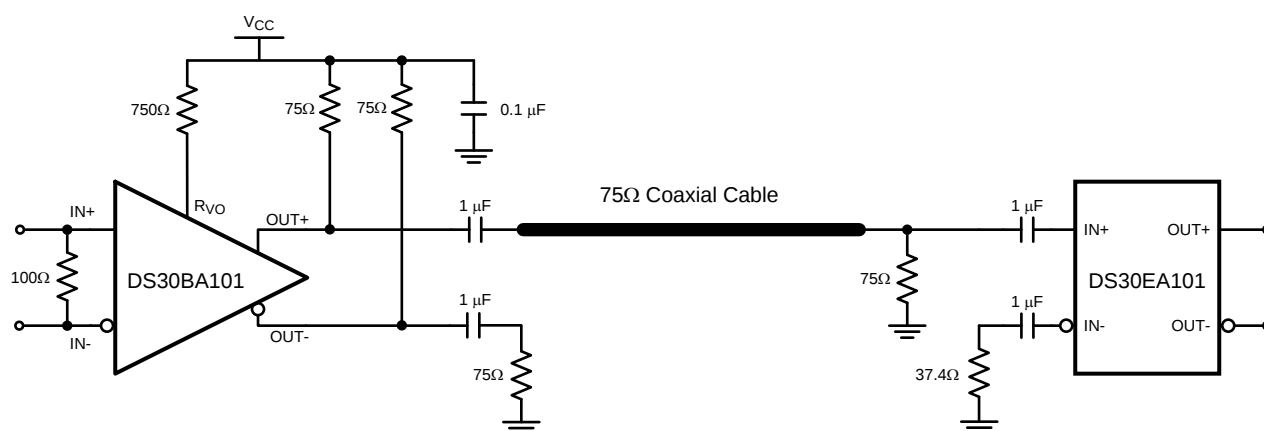


Figure 4. Cable Extender Chipset Application Circuit for 75Ω Coaxial Cable

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS30EA101SQ/NOPB	Active	Production	WQFN (RUM) 16	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQ/NOPB.A	Active	Production	WQFN (RUM) 16	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQ/NOPB.B	Active	Production	WQFN (RUM) 16	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQE/NOPB	Active	Production	WQFN (RUM) 16	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQE/NOPB.A	Active	Production	WQFN (RUM) 16	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQX/NOPB	Active	Production	WQFN (RUM) 16	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQX/NOPB.A	Active	Production	WQFN (RUM) 16	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101
DS30EA101SQX/NOPB.B	Active	Production	WQFN (RUM) 16	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	30EA101

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

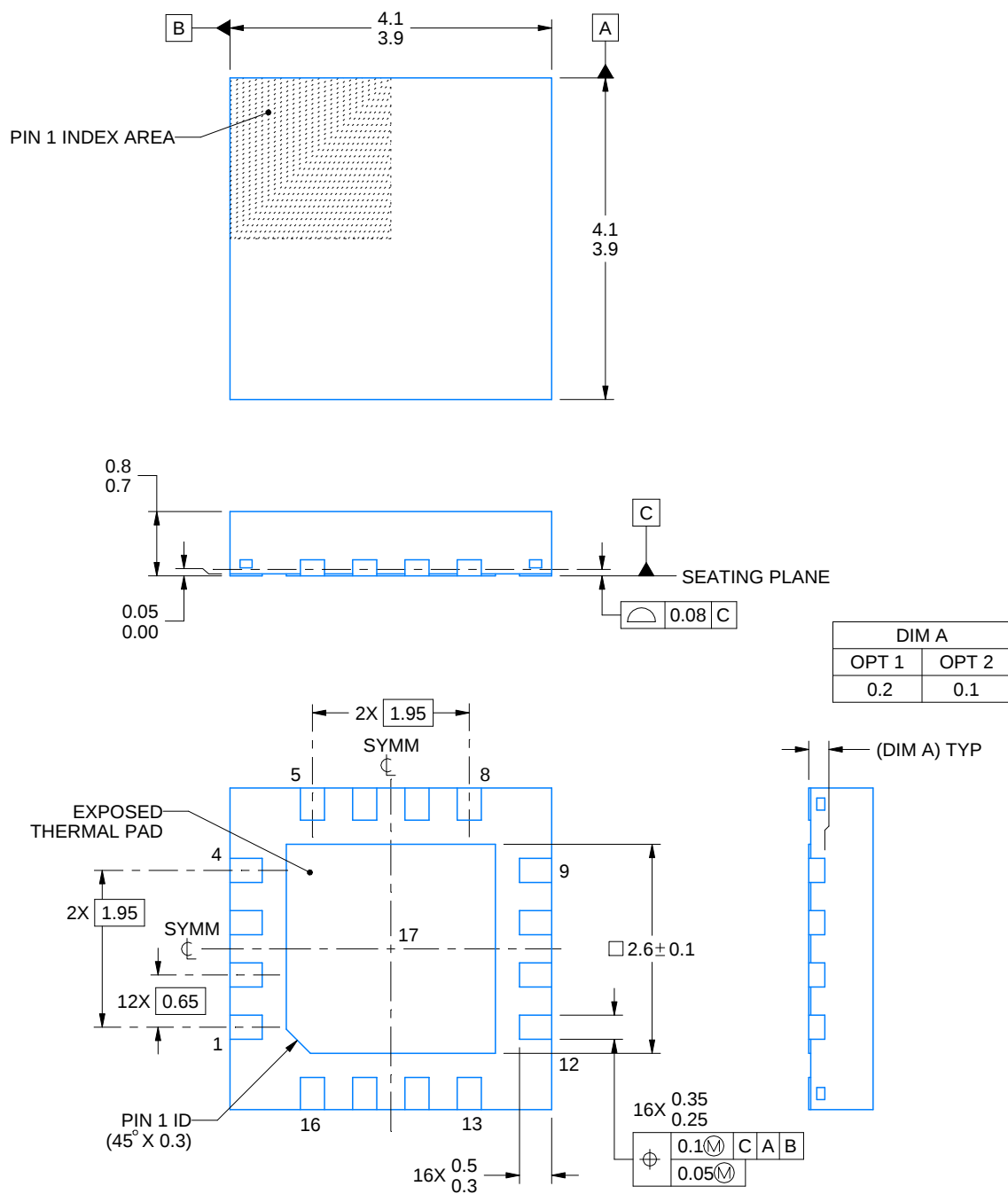
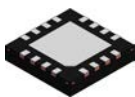
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS30EA101SQ/NOPB	WQFN	RUM	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS30EA101SQE/NOPB	WQFN	RUM	16	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS30EA101SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS30EA101SQ/NOPB	WQFN	RUM	16	1000	208.0	191.0	35.0
DS30EA101SQE/NOPB	WQFN	RUM	16	250	208.0	191.0	35.0
DS30EA101SQX/NOPB	WQFN	RUM	16	4500	356.0	356.0	36.0



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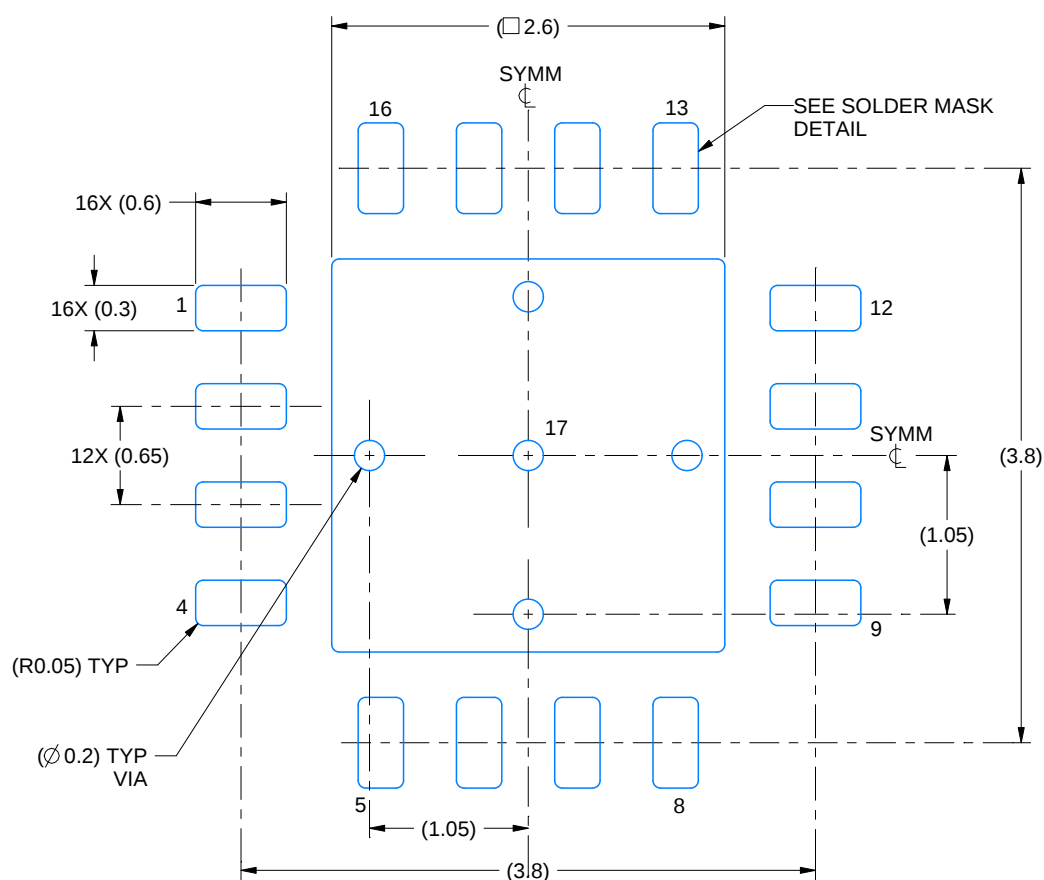
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

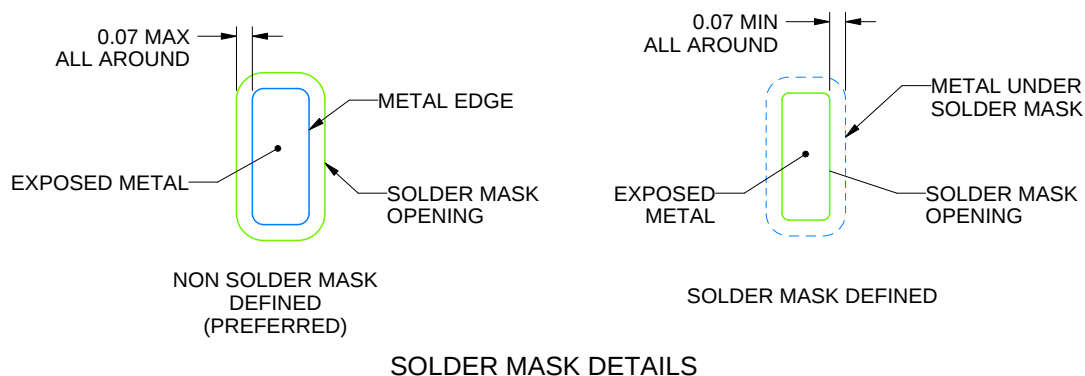
RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



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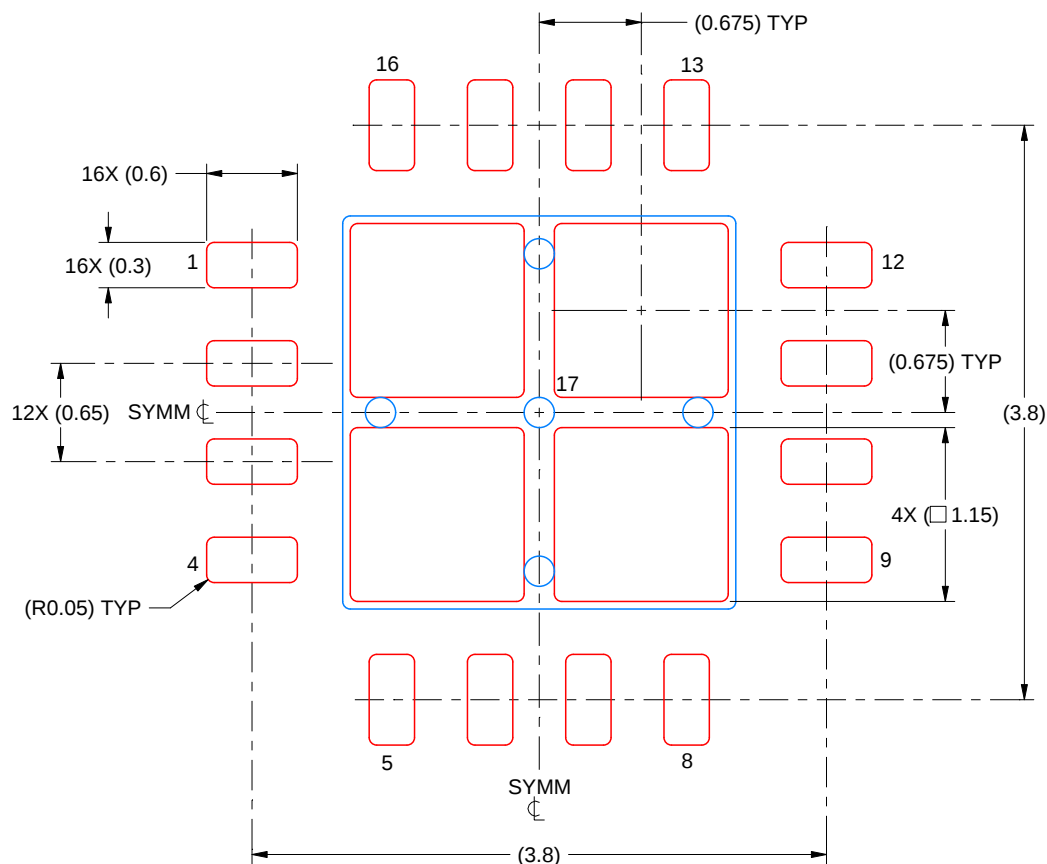
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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