

SN74CBT16209 18-BIT BUS EXCHANGE SWITCH

NOVEMBER 1992 – REVISED APRIL 1993

- 5-Ω Switch Connection Between Two Ports
- Near-Zero Propagation Delay
- TTL-Compatible Input and Output Levels
- Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages

description

The SN74CBT16209 provides 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay.

The device operates as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports using the data-select inputs (S0–S2).

The SN74CBT16209 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)

S0	1	48	S1
1A1	2	47	S2
1A2	3	46	1B1
GND	4	45	1B2
2A1	5	44	2B1
2A2	6	43	2B2
V _{CC}	7	42	GND
3A1	8	41	3B1
3A2	9	40	3B2
GND	10	39	GND
4A1	11	38	4B1
4A2	12	37	4B2
5A1	13	36	5B1
5A2	14	35	5B2
GND	15	34	GND
6A1	16	33	6B1
6A2	17	32	6B2
7A1	18	31	7B1
7A2	19	30	7B2
GND	20	29	GND
8A1	21	28	8B1
8A2	22	27	8B2
9A1	23	26	9B1
9A2	24	25	9B2

FUNCTION TABLE

FLOW CONTROL			OUTPUTS		FUNCTION
S0	S1	S2	A1	A2	
L	L	L	Z	Z	Disconnect
H	L	L	Z	B2	A2 to B2
L	H	L	B2	Z	A1 to B2
H	H	L	B1	B2	A1 to B1, A2 to B2
L	L	H	B1	Z	A1 to B1
H	L	H	Z	Z	Disconnect
L	H	H	Z	B1	A2 to B1
H	H	H	B2	B1	A1 to B2, A2 to B1

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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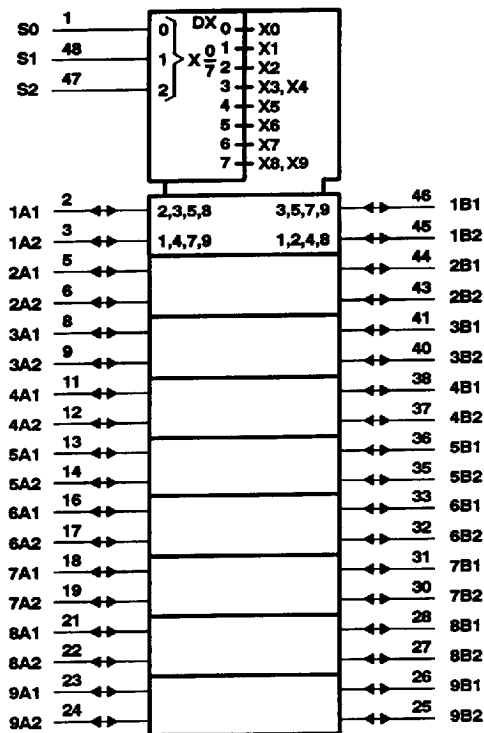
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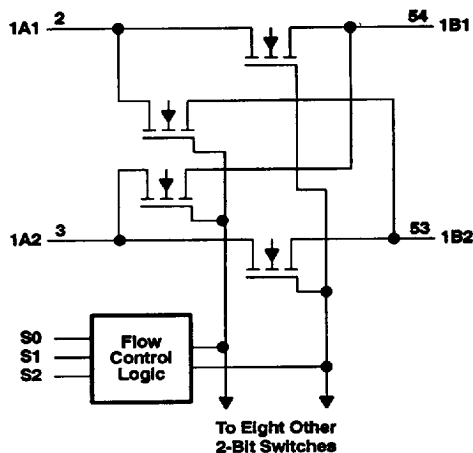
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logic symbol†



logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Current into any pin, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DGG package	0.6 W
DL package	0.85 W
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
T_A Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
I_I	$V_{CC} = 0$, $V_I = 5.5\text{ V}$			10	μA
	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$ or GND			± 1	
I_{OS}	$V_{CC} = 4.5\text{ V}$, $V_{I(A)} = 0$, $V_{I(B)} = 4.5\text{ V}$	100			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND			1	mA
$\Delta I_{CC}^\ddagger$	$V_{CC} = 3.6\text{ V}$, One input at 2.7 V, Other inputs at V_{CC} or GND			0.2	mA
C_i Control pins	$V_I = 3\text{ V}$ or 0		4		pF
$C_o(\text{ON})$	$V_O = 3\text{ V}$ or 0, Switch on		8		pF
$C_o(\text{OFF})$	$V_O = 3\text{ V}$ or 0, Switch off		6		pF
$r_{on}^\S$	$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 64\text{ mA}$			6	Ω
	$V_{CC} = 4.5\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			12	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = -40^\circ\text{C}$ TO 85°C		$T_A = 0^\circ\text{C}$ TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}^\ddagger$	A or B	B or A				0.25	ns
$t_{PHL}^\ddagger$						0.25	
t_{PLH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PHL}					1.5	7.5	
t_{PZH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	S0, S1, S2	A or B			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

‡ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.

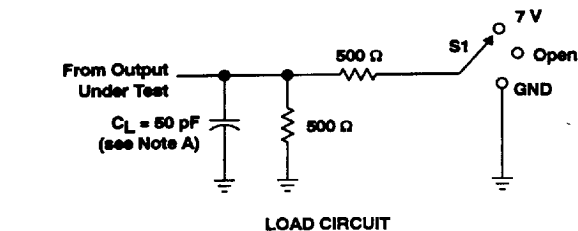
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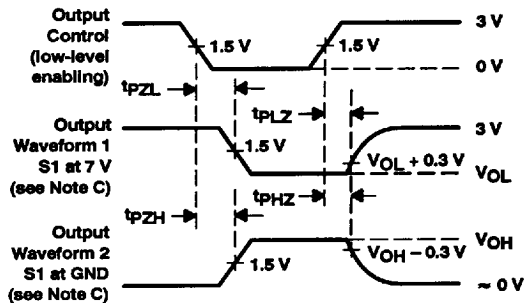
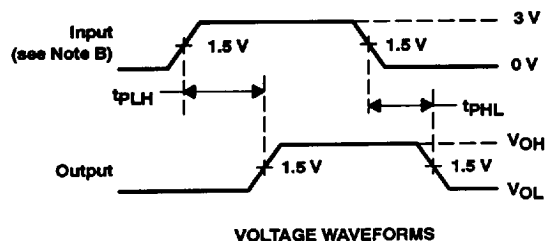
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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