

2x2 LVDS CROSSPOINT SWITCH

FEATURES

- High Speed (>1000 Mbps) Upgrade for DS90CP22 2x2 LVDS Crosspoint Switch
- LVPECL Crosspoint Switch Available in SN65LVCP23
- Low-Jitter Fully Differential Data Path
- 50 ps (Typ), of Peak-to-Peak Jitter With PRBS = $2^{23}-1$ Pattern
- Less Than 200 mW (Typ), 300 mW (Max) Total Power Dissipation
- Output (Channel-to-Channel) Skew Is 10 ps (Typ), 50 ps (Max)
- Configurable as 2:1 Mux, 1:2 Demux, Repeater or 1:2 Signal Splitter
- Inputs Accept LVDS, LVPECL, and CML Signals
- Fast Switch Time of 1.7 ns (Typ)
- Fast Propagation Delay of 0.65 ns (Typ)
- 16 Lead SOIC and TSSOP Packages
- Inter-Operates With TIA/EIA-644-A LVDS Standard
- Operating Temperature: -40°C to 85°C

APPLICATIONS

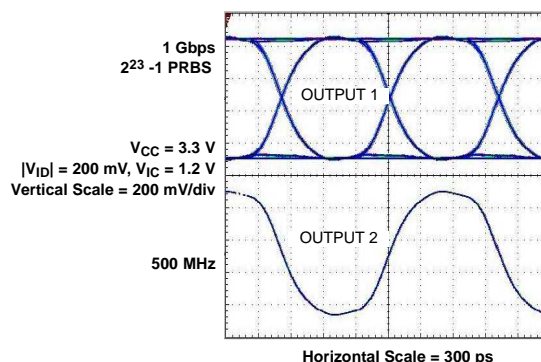
- Base Stations
- Add/Drop Muxes
- Protection Switching for Serial Backplanes
- Network Switches/Routers
- Optical Networking Line Cards/Switches
- Clock Distribution

DESCRIPTION

The SN65LVCP22 is a 2x2 crosspoint switch providing greater than 1000 Mbps operation for each path. The dual channels incorporate wide common-mode (0 V to 4 V) receivers, allowing for the receipt of LVDS, LVPECL, and CML signals. The dual outputs are LVDS drivers to provide low-power, low-EMI, high-speed operation. The SN65LVCP22 provides a single device supporting 2:2 buffering (repeating), 1:2 splitting, 2:1 multiplexing, 2x2 switching, and LVPECL/CML to LVDS level translation on each channel. The flexible operation of the SN65LVCP22 provides a single device to support the redundant serial bus transmission needs (working and protection switching cards) of fault-tolerant switch systems found in optical networking, wireless infrastructure, and data communications systems. TI offers additional gigabit repeater/ translator and crosspoint products in the SN65LVDS100 and SN65LVDS122.

The SN65LVCP22 uses a fully differential data path to ensure low-noise generation, fast switching times, low pulse width distortion, and low jitter. Output channel-to-channel skew is less than 10 ps (typ) and 50 ps (max) to ensure accurate alignment of outputs in all applications. Both SOIC and TSSOP package options are available to allow easy upgrade for existing solutions, and board area savings where space is critical.

OUTPUTS OPERATING SIMULTANEOUSLY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE DESIGNATOR	PART NUMBER ⁽¹⁾	SYMBOLIZATION
SOIC	SN65LVCP22D	LVCP22
TSSOP	SN65LVCP22PW	LVCP22

(1) Add the suffix R for taped and reeled carrier

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
SOIC (D)	High-K ⁽²⁾	1361 mW	13.9 mW/ $^\circ\text{C}$	544 mW
TSSOP (PW)	High-K ⁽²⁾	1074 mW	10.7 mW/ $^\circ\text{C}$	430 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

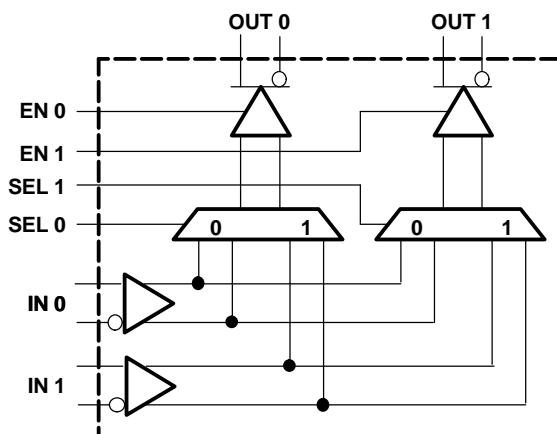
THERMAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS	VALUE	UNITS
θ_{JB}	Junction-to-board thermal resistance	D		11.2	$^\circ\text{C/W}$
		PW		18.4	
θ_{JC}	Junction-to-case thermal resistance	D		23.7	$^\circ\text{C/W}$
		PW		16.0	
P_D	Device power dissipation	Typical	$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, 1 Gbps	198	mW
		Maximum	$V_{CC} = 3.6\text{ V}$, $T_A = 85^\circ\text{C}$, 1 Gbps	313	

FUNCTION TABLE

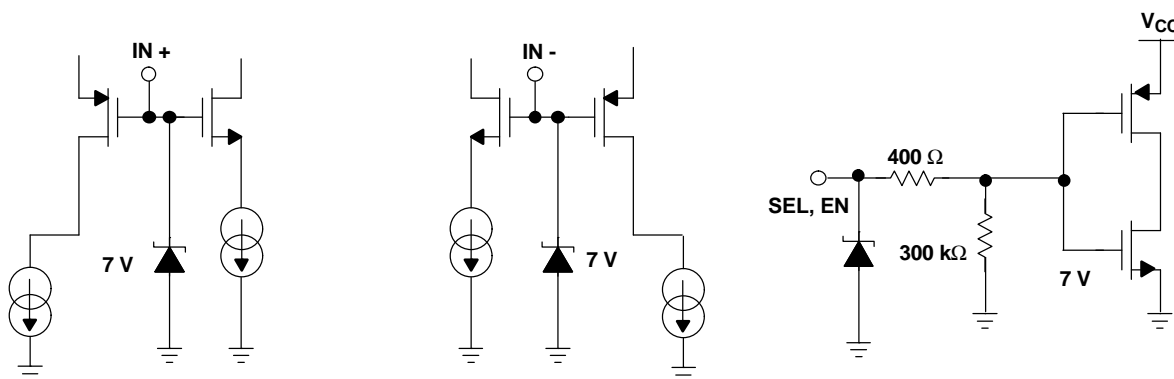
SEL0	SEL1	OUT0	OUT1	FUNCTION
0	0	IN0	IN0	1:2 Splitter
0	1	IN0	IN1	Repeater
1	0	IN1	IN0	Switch
1	1	IN1	IN1	1:2 Splitter

FUNCTIONAL BLOCK DIAGRAM

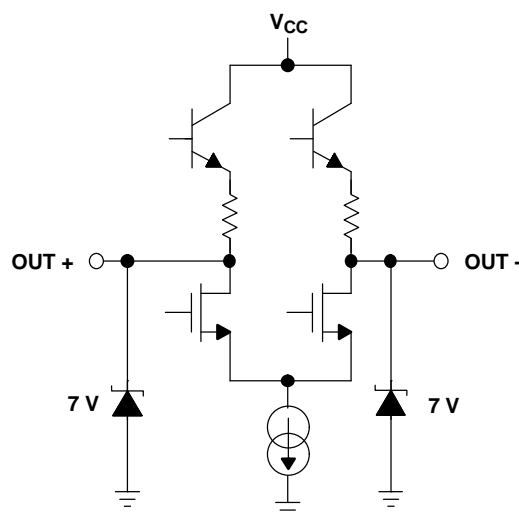


EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUTS



OUTPUTS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

			UNITS
Supply voltage ⁽²⁾ range, V_{CC}			–0.5 V to 4 V
CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1)			–0.5 V to 4 V
LVDS receiver input voltage (IN+, IN–)			–0.7 V to 4.3 V
LVDS driver output voltage (OUT+, OUT–)			–0.5 V to 4 V
LVDS output short circuit current			Continuous
Storage temperature range			–65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			235°C
Continuous power dissipation			See Dissipation Rating Table
Electrostatic discharge	Human body model ⁽³⁾	All pins	±5 kV
	Charged-device mode ⁽⁴⁾	All pins	±500 V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	0		4	V
Junction temperature			125	°C
Operating free-air temperature, $T_A^{(1)}$	–40		85	°C
Magnitude of differential input voltage $ V_{ID} $	0.1		3	V

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)					
V_{IH} High-level input voltage		2		V_{CC}	V
V_{IL} Low-level input voltage		GND		0.8	V
I_{IH} High-level input current	$V_{IN} = 3.6\text{ V or }2.0\text{ V}, V_{CC} = 3.6\text{ V}$		±3	±20	µA
I_{IL} Low-level input current	$V_{IN} = 0.0\text{ V or }0.8\text{ V}, V_{CC} = 3.6\text{ V}$		±1	±10	µA
V_{CL} Input clamp voltage	$I_{CL} = -18\text{ mA}$		-0.8	-1.5	V
LVDS OUTPUT SPECIFICATIONS (OUT0, OUT1)					
$ V_{OD} $ Differential output voltage	$R_L = 75\ \Omega$, See Figure 2	270	365	475	mV
	$R_L = 75\ \Omega, V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}$, See Figure 2	285	365	440	
$\Delta V_{OD} $ Change in differential output voltage magnitude between logic states	$V_{ID} = \pm 100\text{ mV}$, See Figure 2	–25		25	mV
V_{OS} Steady-state offset voltage	See Figure 3	1	1.2	1.45	V
ΔV_{OS} Change in steady-state offset voltage between logic states	See Figure 3	–25		25	mV
$V_{OC(PP)}$ Peak-to-peak common-mode output voltage	See Figure 3		50	150	mV
I_{OZ} High-impedance output current	$V_{OUT} = \text{GND or } V_{CC}$			±10	µA
I_{OFF} Power-off leakage current	$V_{CC} = 0\text{ V}, 1.5\text{ V}; V_{OUT} = 3.6\text{ V or GND}$			±10	µA
I_{OS} Output short-circuit current	$V_{OUT+} \text{ or } V_{OUT-} = 0\text{ V}$			–24	mA
I_{OSB} Both outputs short-circuit current	$V_{OUT+} \text{ and } V_{OUT-} = 0\text{ V}$	–12		12	mA
C_O Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$		3		pF
LVDS RECEIVER DC SPECIFICATIONS (IN0, IN1)					
V_{TH} Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{TL} Negative-going differential input voltage threshold	See Figure 1 and Table 1	–100			mV
$V_{ID(HYS)}$ Differential input voltage hysteresis			25		mV
V_{CMR} Common-mode voltage range	$V_{ID} = 100\text{ mV}, V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.05		3.95	V
I_{IN} Input current	$V_{IN} = 4\text{ V}, V_{CC} = 3.6\text{ V or }0.0$		±1	±10	µA
	$V_{IN} = 0\text{ V}, V_{CC} = 3.6\text{ V or }0.0$		±1	±10	
C_{IN} Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$		3		pF
SUPPLY CURRENT					
I_{CCD} Total supply current	$R_L = 75\ \Omega, C_L = 5\text{ pF}, 500\text{ MHz (1000 Mbps)}, \text{EN0=EN1=High}$		60	87	mA
I_{CCZ} 3-state supply current	EN0 = EN1 = Low		25	35	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

parameter	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET} Input to SEL setup time	See Figure 6	1	0.5		ns
t_{HOLD} Input to SEL hold time	See Figure 6	1.1	0.5		ns
t_{SWITCH} SEL to switched output	See Figure 6		1.7	2.5	ns
t_{PHZ} Disable time, high-level-to-high-impedance	See Figure 5		2	4	ns
t_{PLZ} Disable time, low-level-to-high-impedance	See Figure 5		2	4	ns
t_{PZH} Enable time, high-impedance -to-high-level output	See Figure 5		2	4	ns
t_{PZL} Enable time, high-impedance-to-low-level output	See Figure 5		2	4	ns
t_{LHT} Differential output signal rise time (20%-80%) ⁽¹⁾	$C_L = 5$ pF, See Figure 4	150	280	450	ps
t_{HLT} Differential output signal fall time (20%-80%) ⁽¹⁾	$C_L = 5$ pF, See Figure 4	150	280	450	ps
t_{JIT} Added peak-to-peak jitter	$V_{ID} = 200$ mV, 50% duty cycle, $V_{CM} = 1.2$ V, 500 MHz, $C_L = 5$ pF		20	40	ps
	$V_{ID} = 200$ mV, PRBS = 2 ²³ -1 data pattern, $V_{CM} = 1.2$ V at 1000 Mbps, $C_L = 5$ pF		50	105	ps
t_{Jrms} Added random jitter (rms)	$V_{ID} = 200$ mV, 50% duty cycle, $V_{CM} = 1.2$ V at 500 MHz, $C_L = 5$ pF		1.1	1.8	ps _{RMS}
t_{PLHD} Propagation delay time, low-to-high-level output ⁽¹⁾		400	650	1000	ps
t_{PHLD} Propagation delay time, high-to-low-level output ⁽¹⁾		400	650	1000	ps
t_{skew} Pulse skew ($ t_{PLHD} - t_{PHLD} $) ⁽²⁾	$C_L = 5$ pF, See Figure 4		20	100	ps
t_{CCS} Output channel-to-channel skew, splitter mode	$C_L = 5$ pF, See Figure 4		10	50	ps
f_{MAX} Maximum operating frequency ⁽³⁾		1			GHz

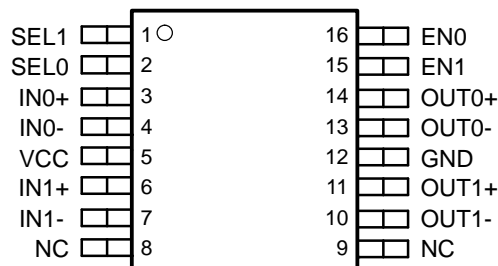
(1) Input: $V_{IC} = 1.2$ V, $V_{ID} = 200$ mV, 50% duty cycle, 1 MHz, $t_r/t_f = 500$ ps

(2) t_{skew} is the magnitude of the time difference between the t_{PLHD} and t_{PHLD} of any output of a single device.

(3) Signal generator conditions: 50% duty cycle, t_r or $t_f \leq 100$ ps (10% to 90%), transmitter output criteria: duty cycle = 45% to 55% $V_{OD} \geq 300$ mV.

PIN ASSIGNMENTS

D or PW PACKAGE
(TOP VIEW)



NC - No internal connection

PARAMETER MEASUREMENT INFORMATION

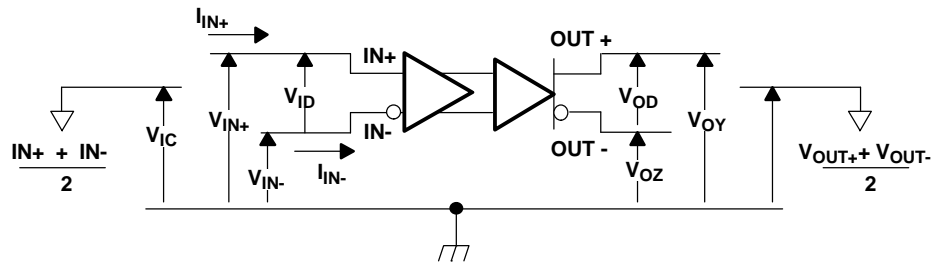


Figure 1. Voltage and Current Definitions

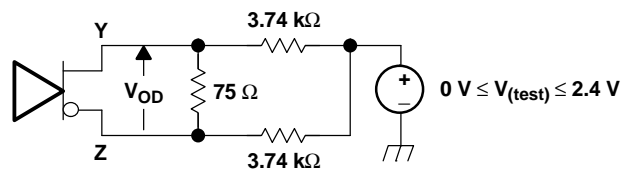
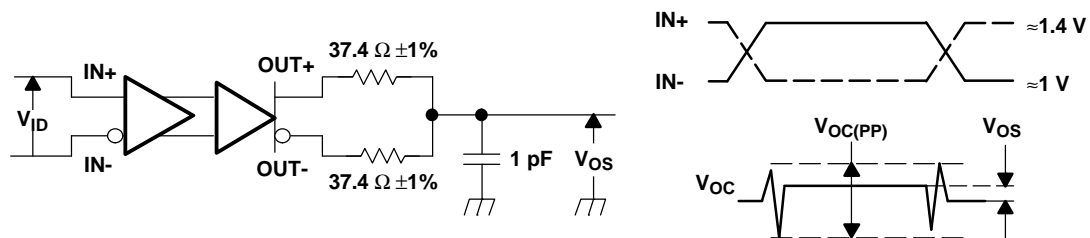


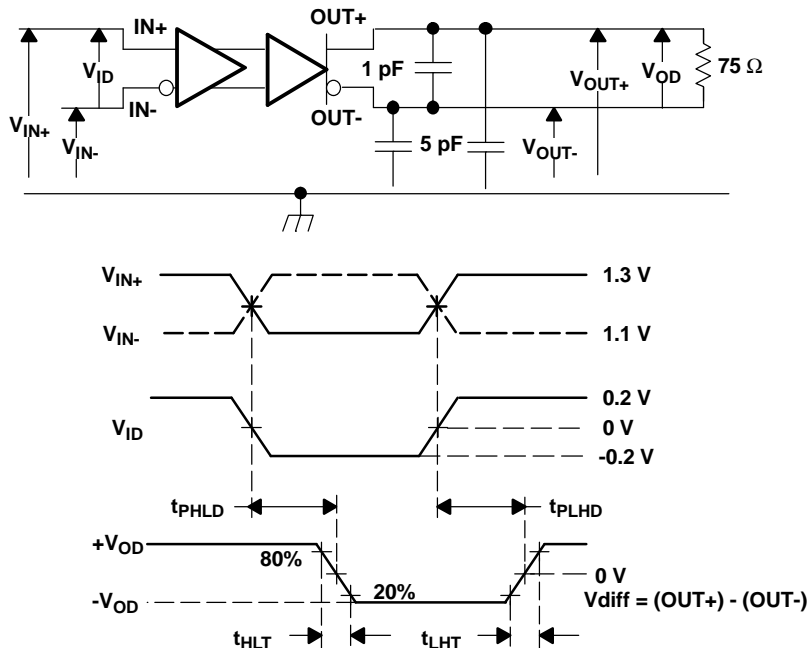
Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns; $R_L = 100 \Omega$; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

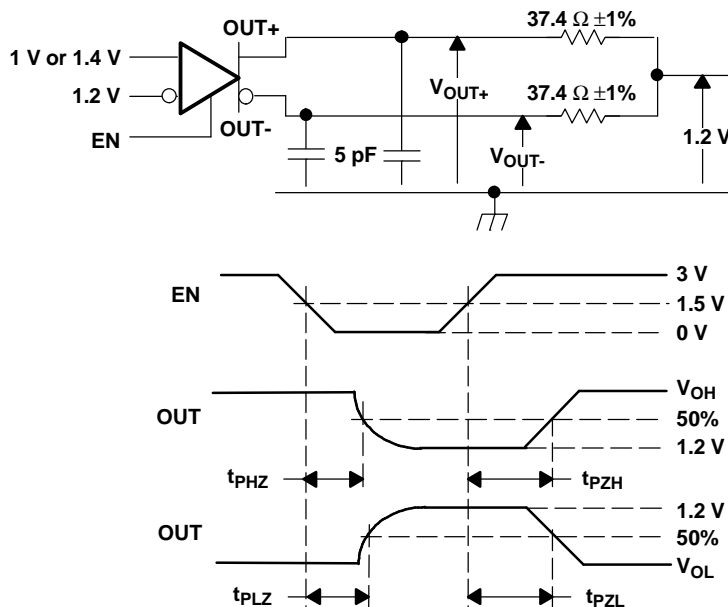
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq .25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Timing Test Circuit and Waveforms



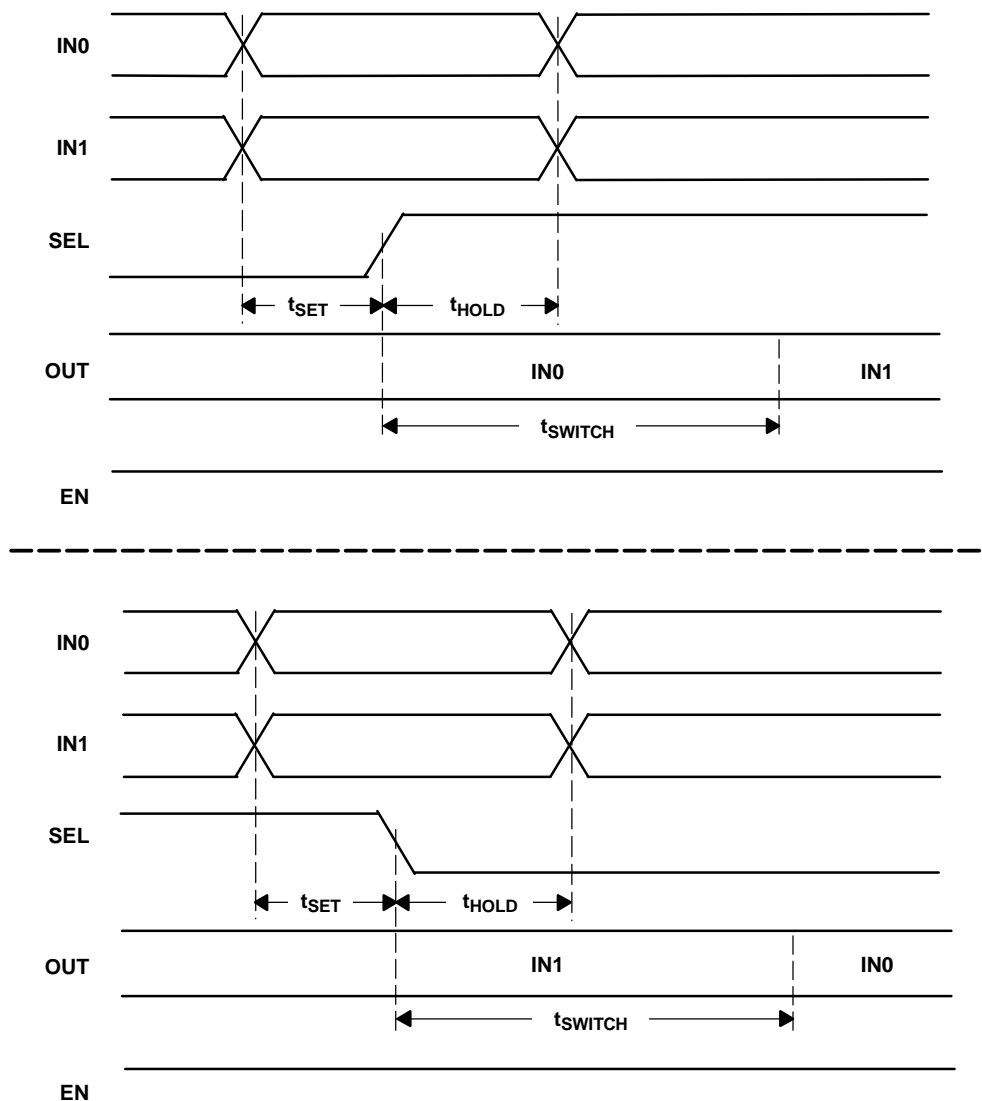
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE	OUTPUT ⁽¹⁾
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

(1) H = high level, L = low level



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 6. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

**DIFFERENTIAL OUTPUT VOLTAGE
vs
RESISTIVE LOAD**

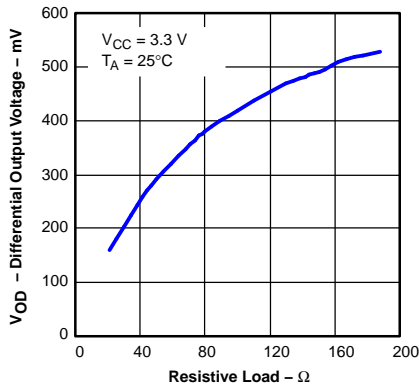


Figure 7.

**SUPPLY CURRENT
vs
FREQUENCY**

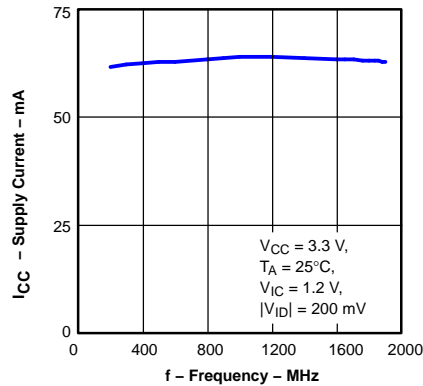


Figure 8.

**PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**

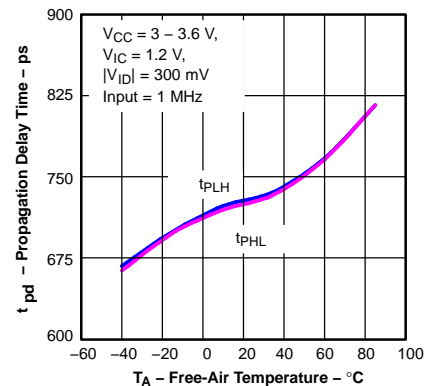


Figure 9.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**

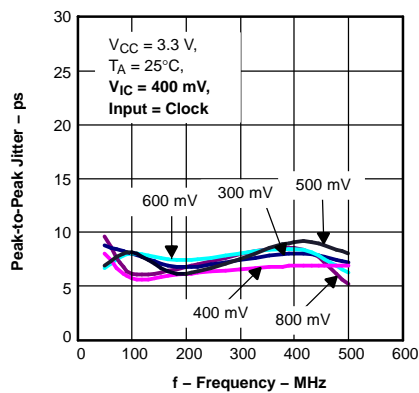


Figure 10.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**

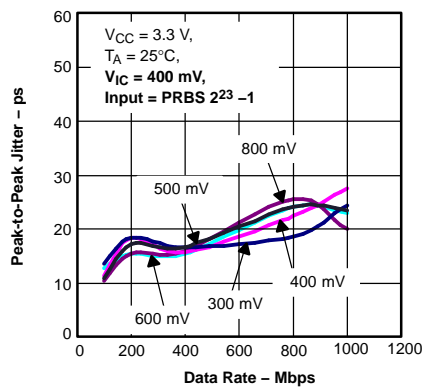


Figure 11.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**

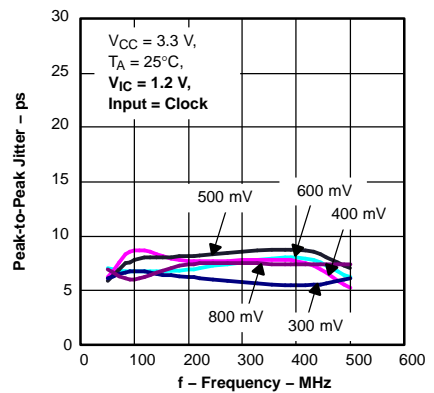


Figure 12.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**

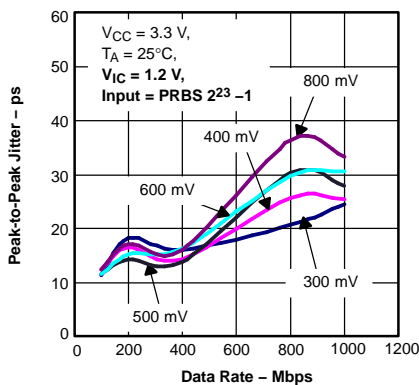


Figure 13.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**

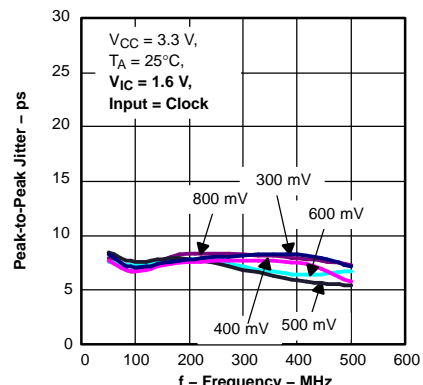


Figure 14.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**

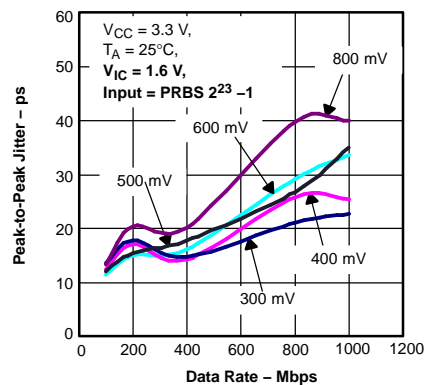


Figure 15.

TYPICAL CHARACTERISTICS (continued)

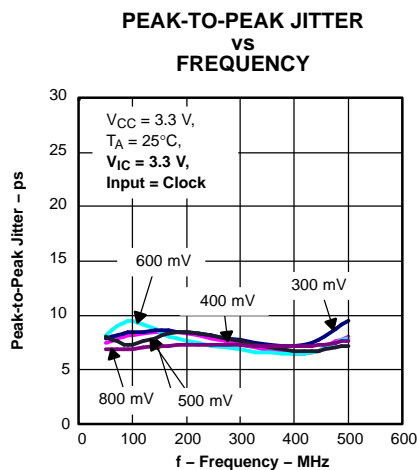


Figure 16.

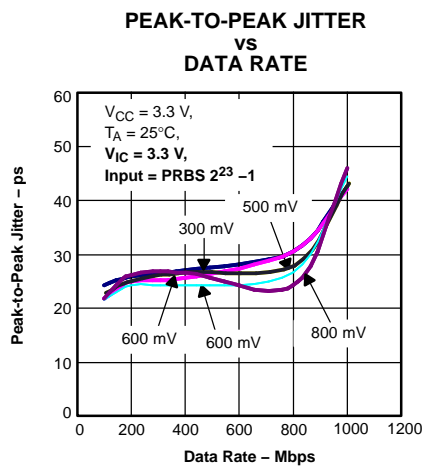


Figure 17.

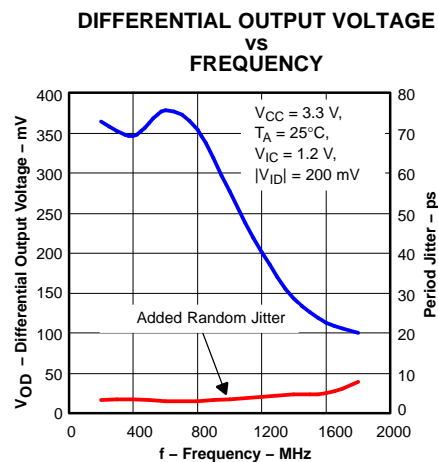


Figure 18.

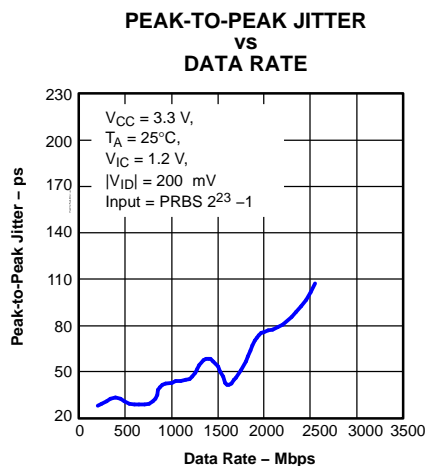


Figure 19.

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

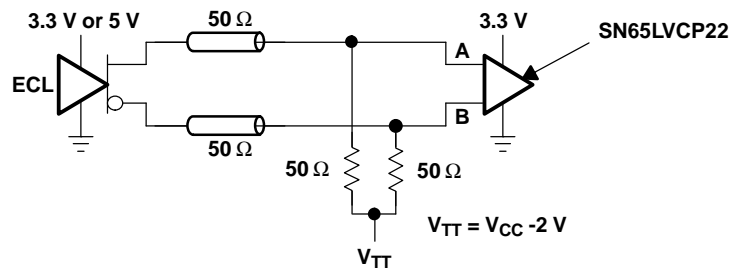


Figure 20. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

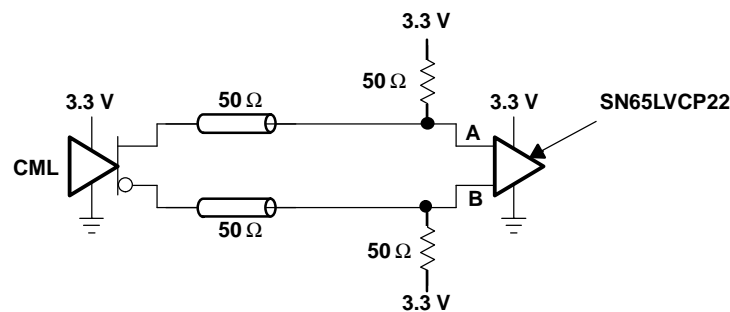


Figure 21. Current-Mode Logic (CML)

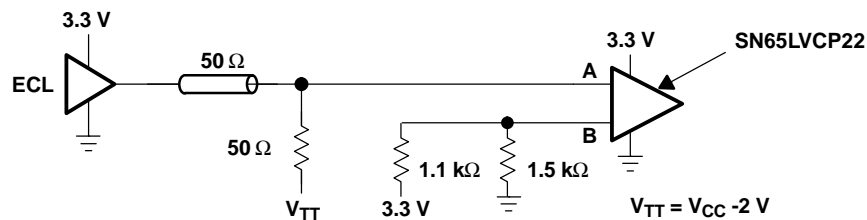


Figure 22. Single-Ended (LVPECL)

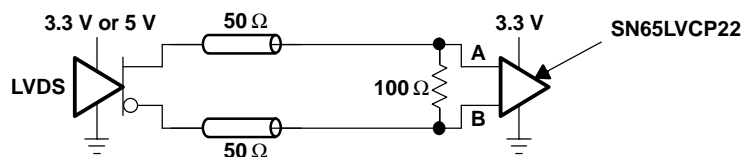


Figure 23. Low-Voltage Differential Signaling (LVDS)

APPLICATION INFORMATION (continued)

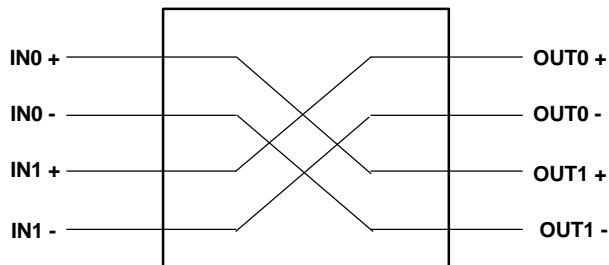


Figure 24. 2 x 2 Crosspoint

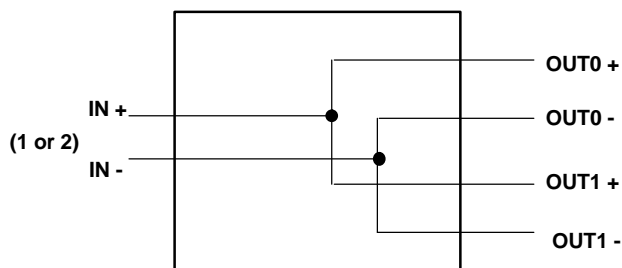


Figure 25. 1:2 Splitter



Figure 26. Dual Repeater

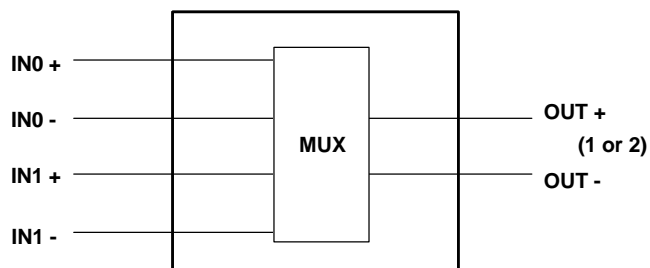


Figure 27. 2:1 MUX

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVCP22D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP22DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP22DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP22DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP22PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP22PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVCP22PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated