

Thyristors

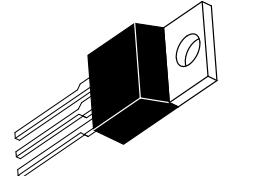
Silicon-Controlled Rectifiers

... designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass-Passivated Junctions
- Blocking Voltage to 800 Volts
- TO-220 Construction — Low Thermal Resistance, High Heat Dissipation and Durability

MCR218
Series

SCRs
8 AMPERES RMS
50 thru 800 VOLTS



CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage ⁽¹⁾ ($T_J = 25$ to 125°C , Gate Open)	V_{DRM} V_{RRM}	50 100 200 400 600 800	Volts
Forward Current RMS (All Conduction Angles)	$I_{T(\text{RMS})}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	80	Amps
Circuit Fusing Considerations ($t = 8.3$ ms)	I^2t	26	A^2s
Forward Peak Gate Power	P_{GM}	5	Watts
Forward Average Gate Power	$P_{G(\text{AV})}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to +150	$^\circ\text{C}$

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

MCR218 Series

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM} , Gate Open) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	I_{DRM}, I_{RRM}	—	—	10 2	μA mA
Peak On-State Voltage ⁽¹⁾ ($I_{TM} = 16\text{ A}$ Peak)	V_{TM}	—	1.5	1.8	Volts
Gate Trigger Current (Continuous dc) ($V_D = 12\text{ V}$, $R_L = 100\text{ Ohms}$)	I_{GT}	—	10	25	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12\text{ V}$, $R_L = 100\text{ Ohms}$) (Rated V_{DRM} , $R_L = 1000\text{ Ohms}$, $T_J = 125^\circ\text{C}$)	V_{GT}	— 0.2	—	1.5 —	Volts
Holding Current (Anode Voltage = 24 Vdc, Peak Initiating On-State Current = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms)	I_H	—	16	30	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM} , Exponential Waveform, Gate Open, $T_J = 125^\circ\text{C}$)	dv/dt	—	100	—	$\text{V}/\mu\text{s}$

1. Pulse Test: Pulse Width = 1 ms, Duty Cycle $\leq 2\%$.

FIGURE 1 — CURRENT DERATING

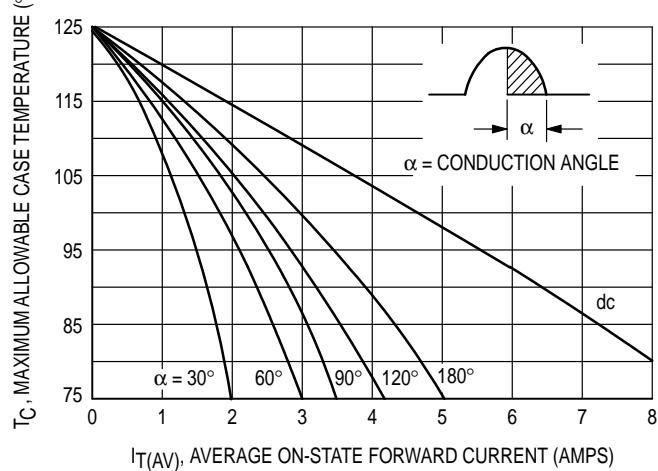


FIGURE 2 — ON-STATE POWER DISSIPATION

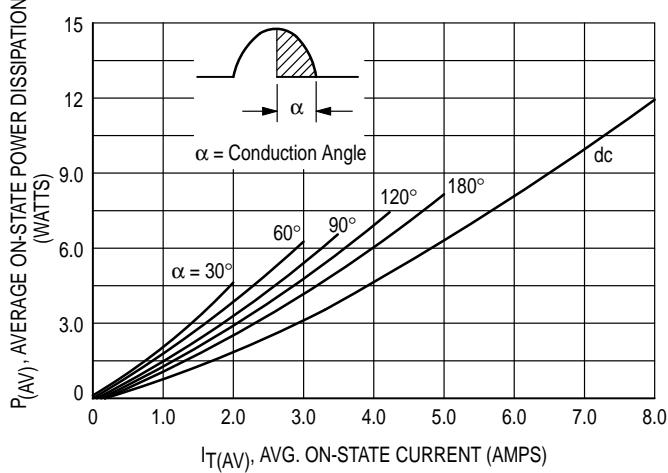


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

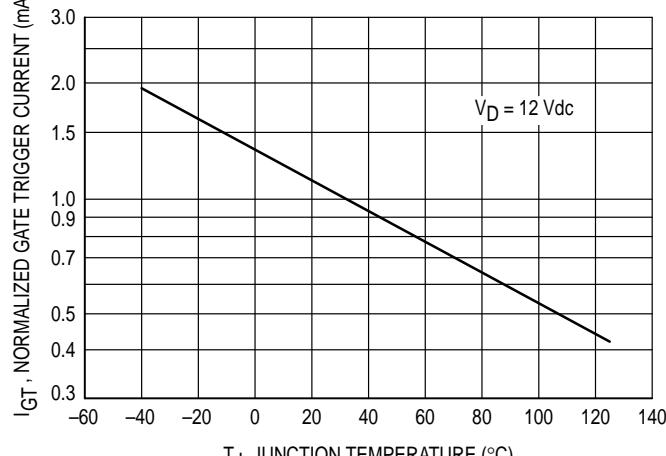
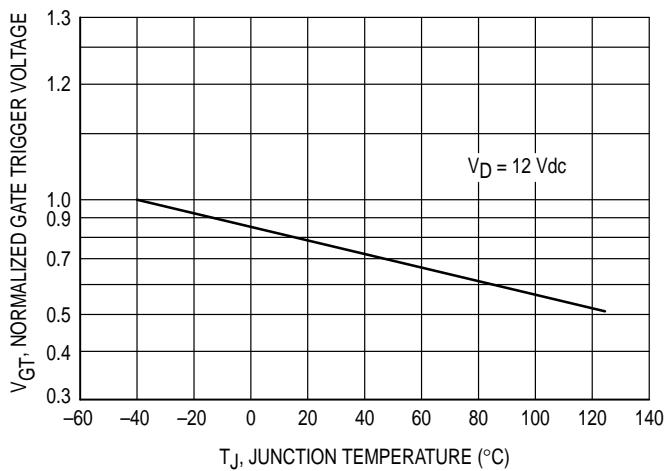
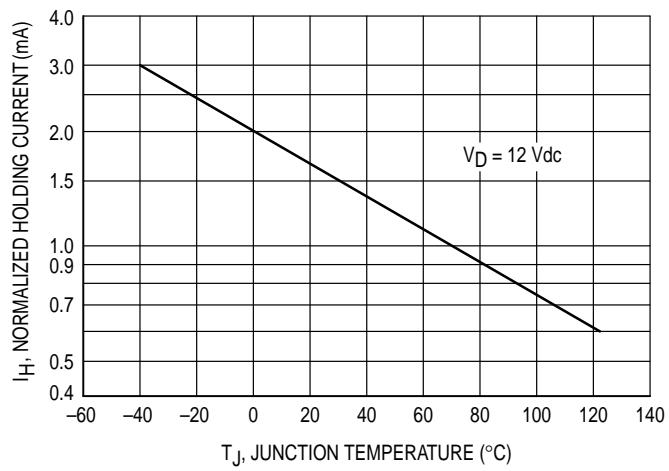
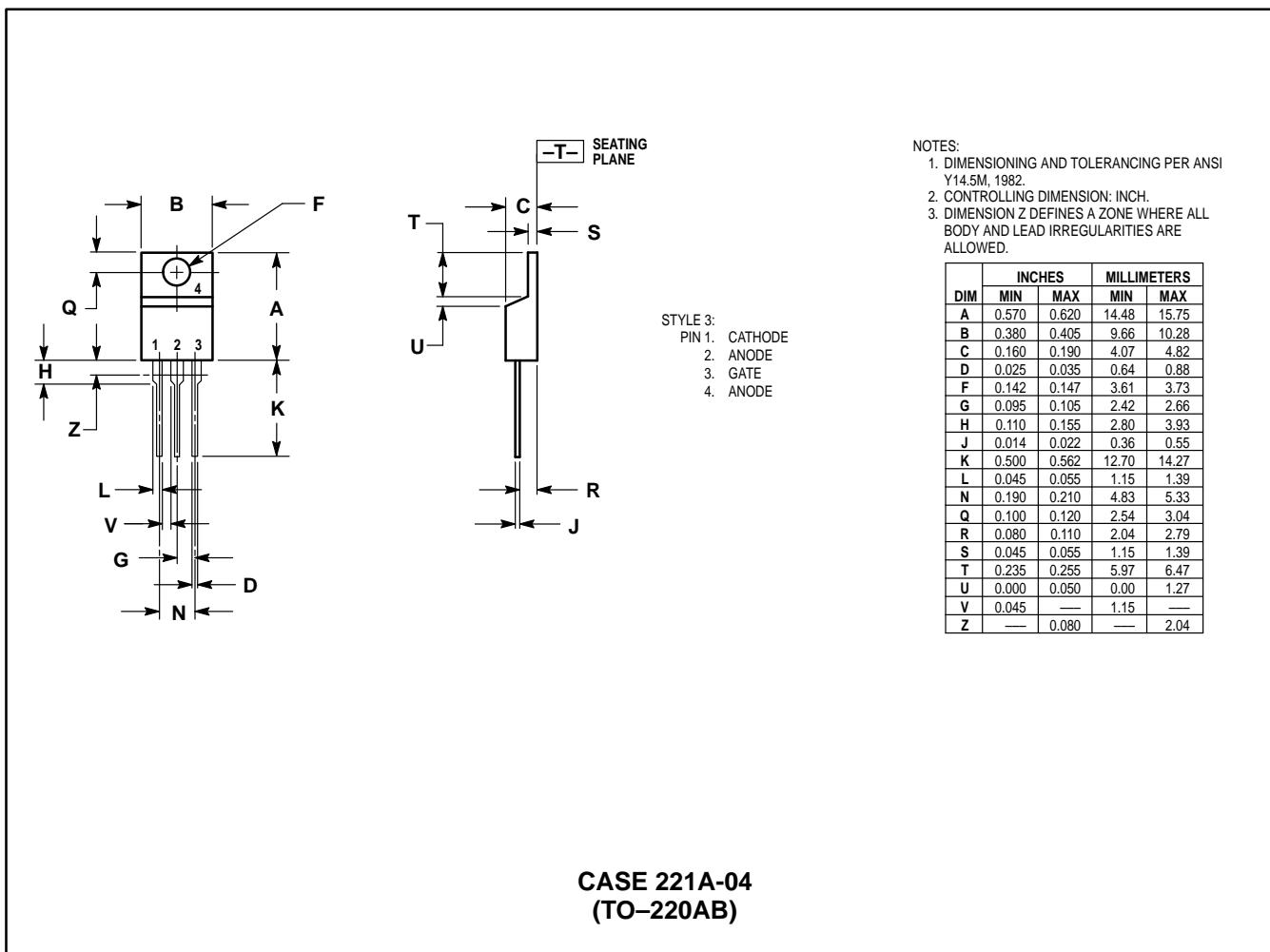


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE**FIGURE 5 — NORMALIZED HOLDING CURRENT**

PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

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