PRELIMINARY

CY62126V

64K x 16 Static RAM

Features

- **2.7V–3.6V operation**
- **CMOS for optimum speed/power**
- **Low active power (70 ns)**
  - **198 mW (max.) (55 mA)**
- **Low standby power (70 ns, LL version)**
  - **54 µW (max.) (15 µA)**
- **Automatic power-down when deselected**
- **Independent control of Upper and Lower Bytes**
- **Available in 44-pin TSOP II (forward)**

Functional Description

The CY62126V is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption by 99% when deselected. The device enters power-down mode when $\overline{CE}$ is HIGH.

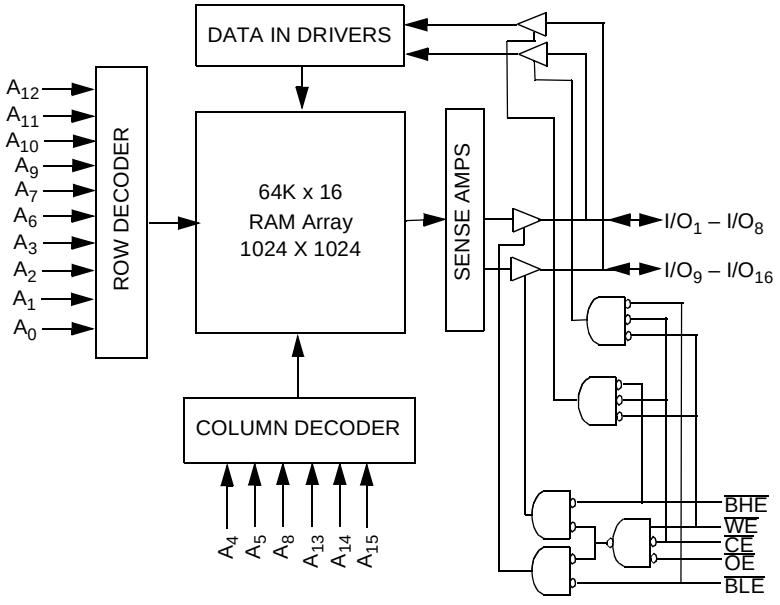
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If byte high enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY62126V is available in standard 44-pin TSOP Type II (forward pinout) and mini-BGA packages.

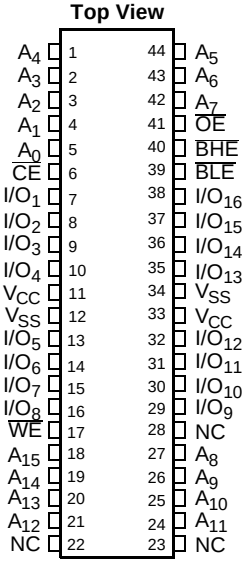
Logic Block Diagram



62126V–1

Pin Configurations

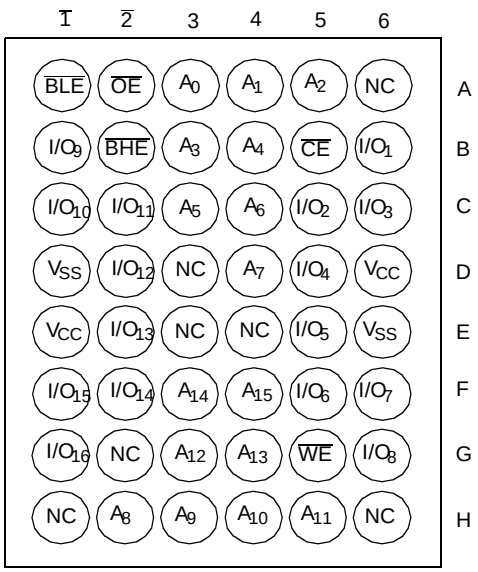
TSOP II (Forward)
Top View



62126V–2

Pin Configurations (continued)

Mini-BGA



62126V–3

Selection Guide

			62126V-55	62126V-70	Units
Maximum Access Time			55	70	ns
Maximum Operating Current			55	55	mA
Maximum CMOS Standby Current			0.3	0.3	mA
		L	50	50	µA
	Com'l	LL	15	15	µA
	Ind'l	LL	30	30	µA

Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... –0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	2.7V–3.6V
Industrial	–40°C to +85°C	

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

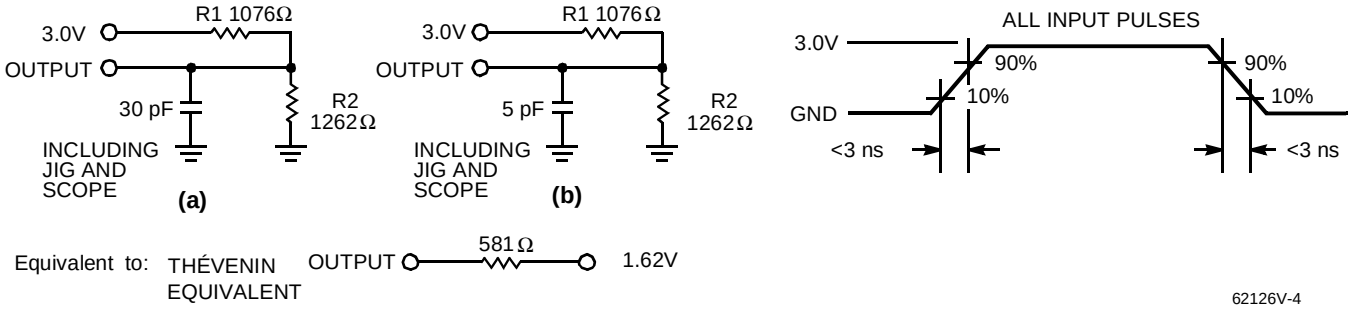
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			62126V Min.	62126V Typ.[3]	62126V Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA			2.2			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA					0.4	V
V_{IH}	Input HIGH Voltage				2.0		V_{CC}+ 0.3	V
V_{IL}	Input LOW Voltage[1]				–0.3		0.4	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$					55	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}					2	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0				0.5	0.3	mA
				L		0.5	50	µA
			Com'l	LL		0.5	15	µA
			Ind'l	LL		0.5	30	µA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	9	pF
C_{OUT}	Output Capacitance		9	pF

AC Test Loads and Waveforms



Notes:

3. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}=3.0V). Parameters are guaranteed by design and characterization, and not 100% tested.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics[5] Over the Operating Range

Parameter	Description	62126V–55		62126V–70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t_{DBE}	Byte Enable to Data Valid		25		35	ns
t_{LZBE}	Byte Enable to LOW Z[7]	5		5		ns
t_{HZBE}	Byte Disable to HIGH Z[6,7]		20		25	ns
WRITE CYCLE[8]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t_{AW}	Address Set-Up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6,7]		25		25	ns
t_{BW}	Byte Enable to End of Write	45		60		ns

Shaded areas contain advance information.

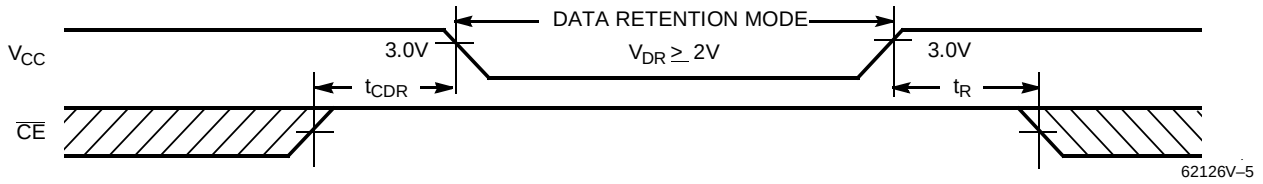
Note:

5. Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30pF load capacitance.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, and t_{HZBE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZWE} is less than t_{LZWE}, and t_{HZBE} is less than t_{LZBE}, for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write. Refer to truth table for further conditions from $\overline{BHE}$ and $\overline{BLE}$.

Data Retention Characteristics (Over the Operating Range for "L" and "LL" version only)

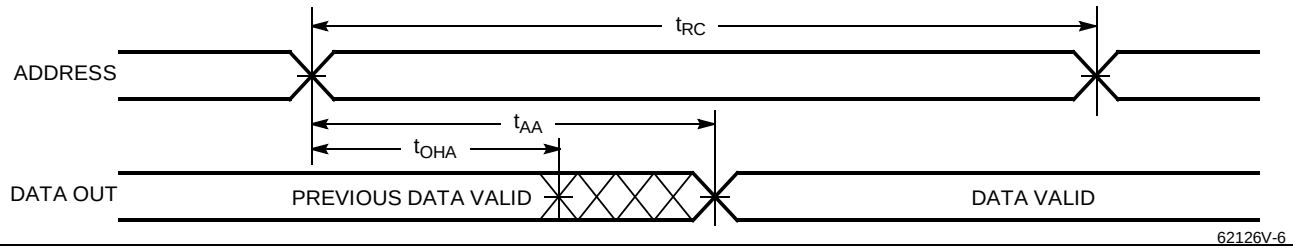
Parameter	Description			Conditions[9]	Min.	Typ	Max.	Unit
V_{DR}	V_{CC} for Data Retention				2.0		3.6	V
I_{CCDR}	Data Retention Current		L	$V_{CC}=V_{DR}=3.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$		0.5	50	µA
		Com'l	LL			0.5	15	µA
		Ind'l	LL			0.5	30	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time				0			ns
t_R	Operation Recovery Time				t_{RC}			ns

Data Retention Waveform

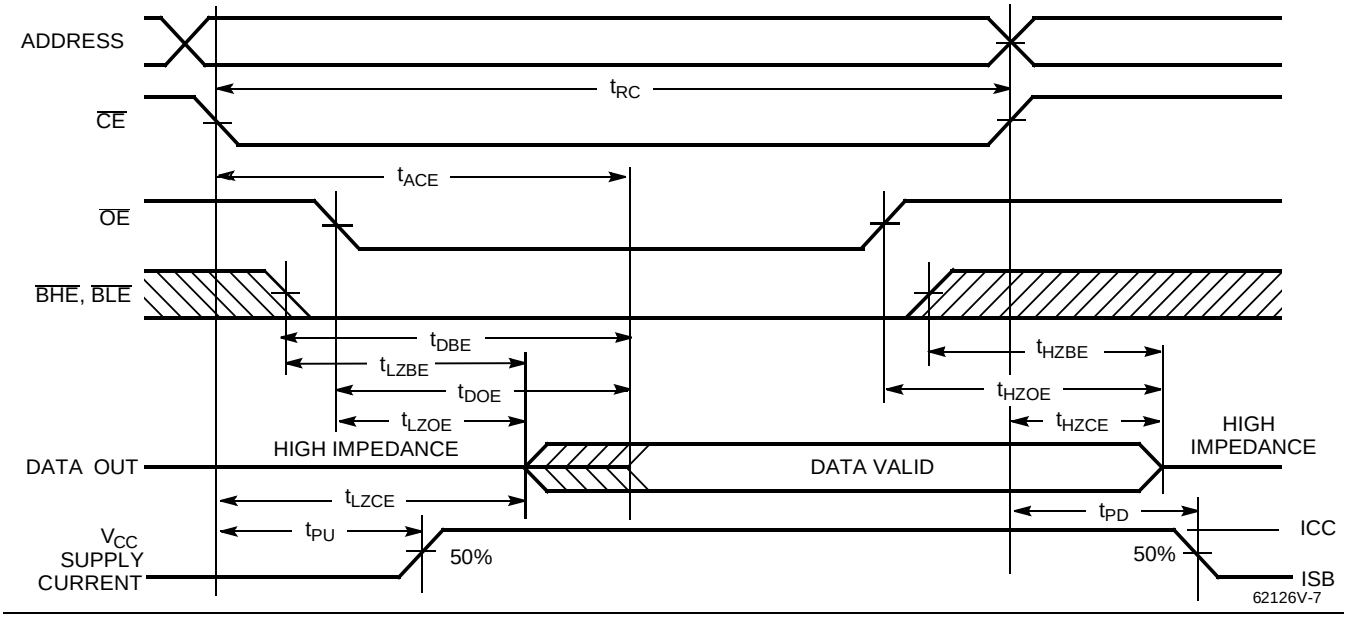


Switching Waveforms

Read Cycle No.1[10,11]



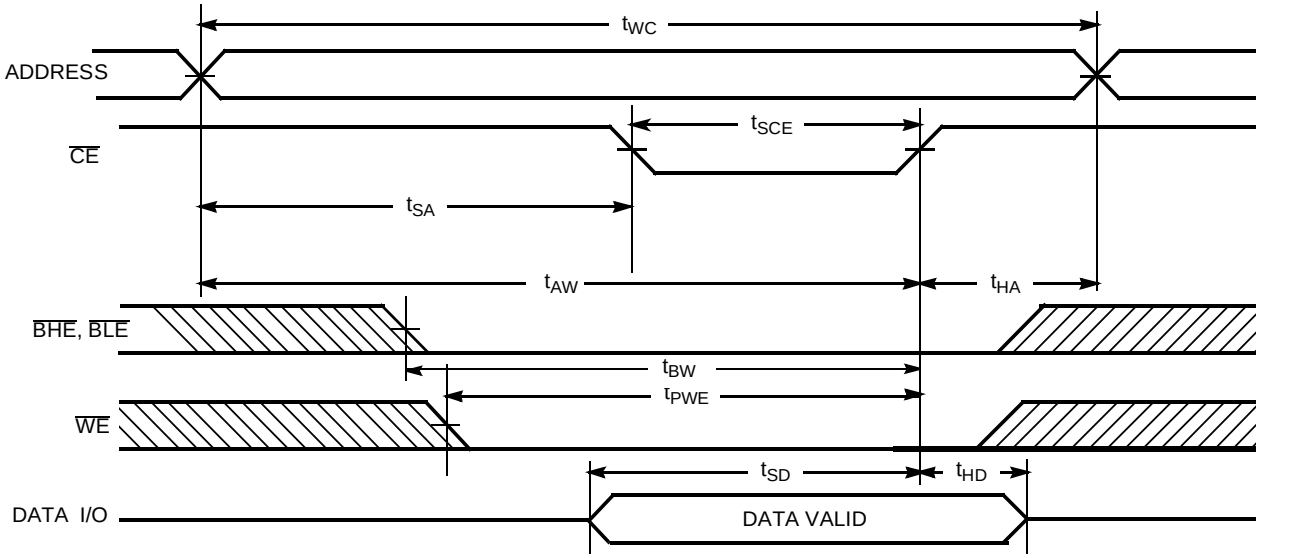
Read Cycle No. 2 ($\overline{OE}$ Controlled)[11,12,13]



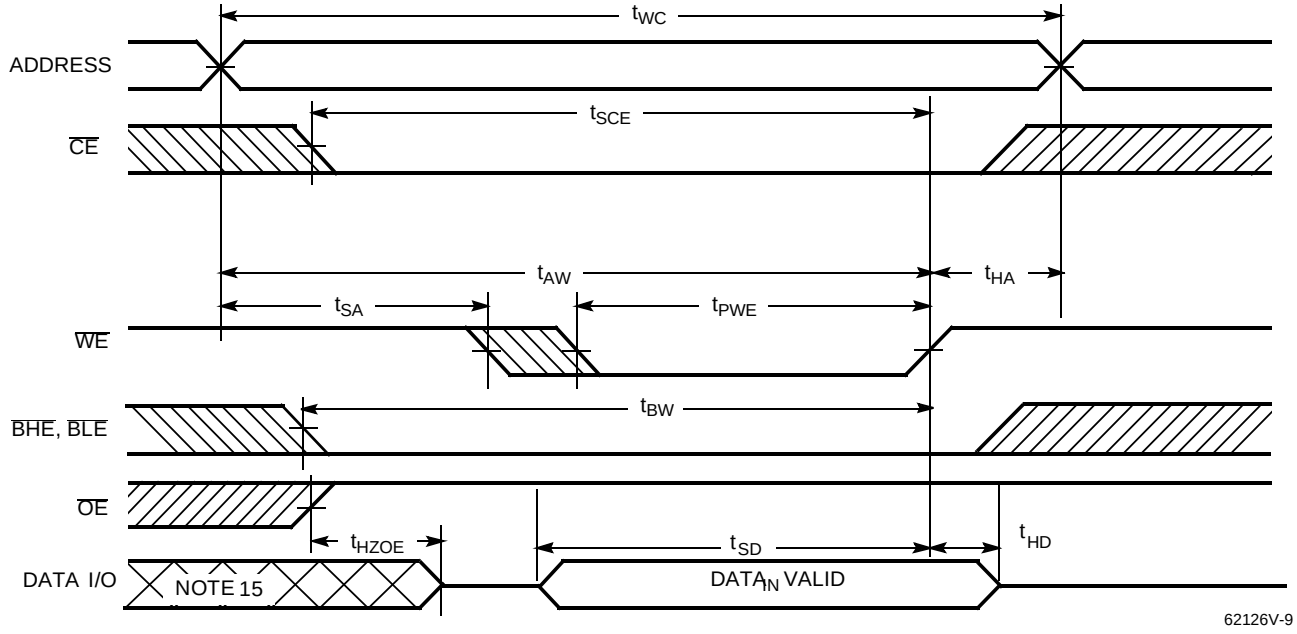
Notes:
9. No input may exceed V_{CC} + 0.3V.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH} or $\overline{BHE}$ and $\overline{BLE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[13,14]



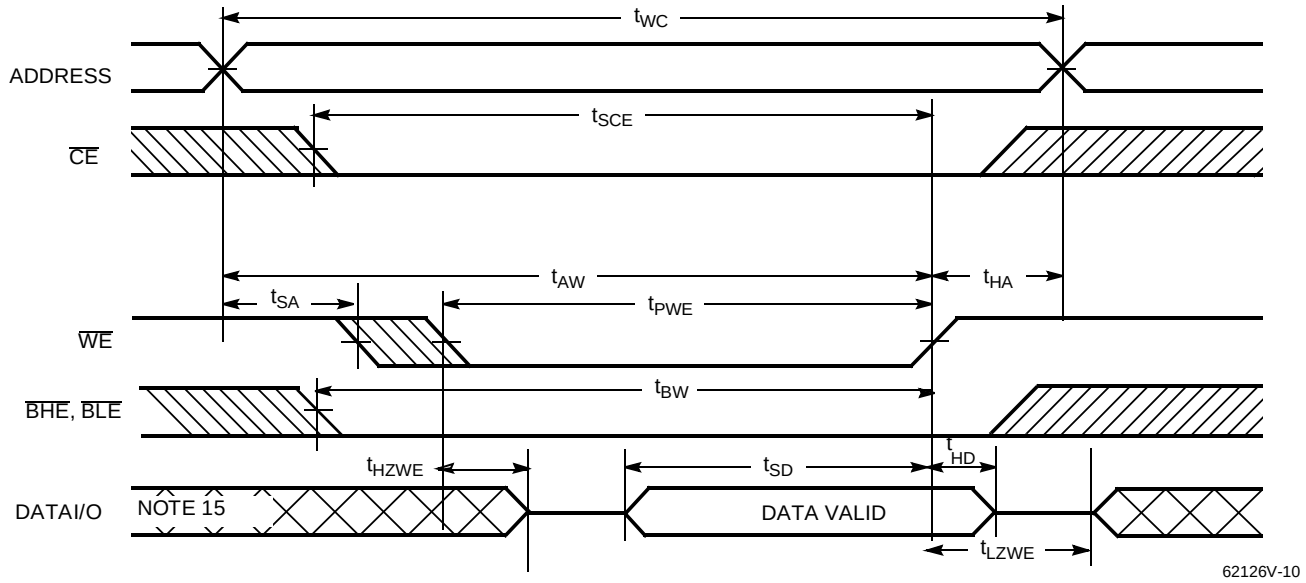
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[13,14]



Notes:
14. If $\overline{CE}$, $\overline{BHE}$, or $\overline{BLE}$ go HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[13,14]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62127V-55ZC	Z44	44-Lead TSOP II	Commercial
	CY62127VL-55ZC	Z44	44-Lead TSOP II	
	CY62127VLL-55ZC	Z44	44-Lead TSOP II	
	CY62127VLL-55ZI	Z44	44-Lead TSOP II	Industrial
55	CY62127V-70BAC	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY62127VL-70BAC	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY62127VLL-70BAC	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY62127VLL-70BAI	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
70	CY62127V-70ZC	Z44	44-Lead TSOP II	Commercial
	CY62127VL-70ZC	Z44	44-Lead TSOP II	
	CY62127VLL-70ZC	Z44	44-Lead TSOP II	
	CY62127VLL-70ZI	Z44	44-Lead TSOP II	Industrial
70	CY62127V-70BAC	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY62127VL-70BAC	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY62127VLL-70BAC	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY62127VLL-70BAI	BA48	48-ball mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial

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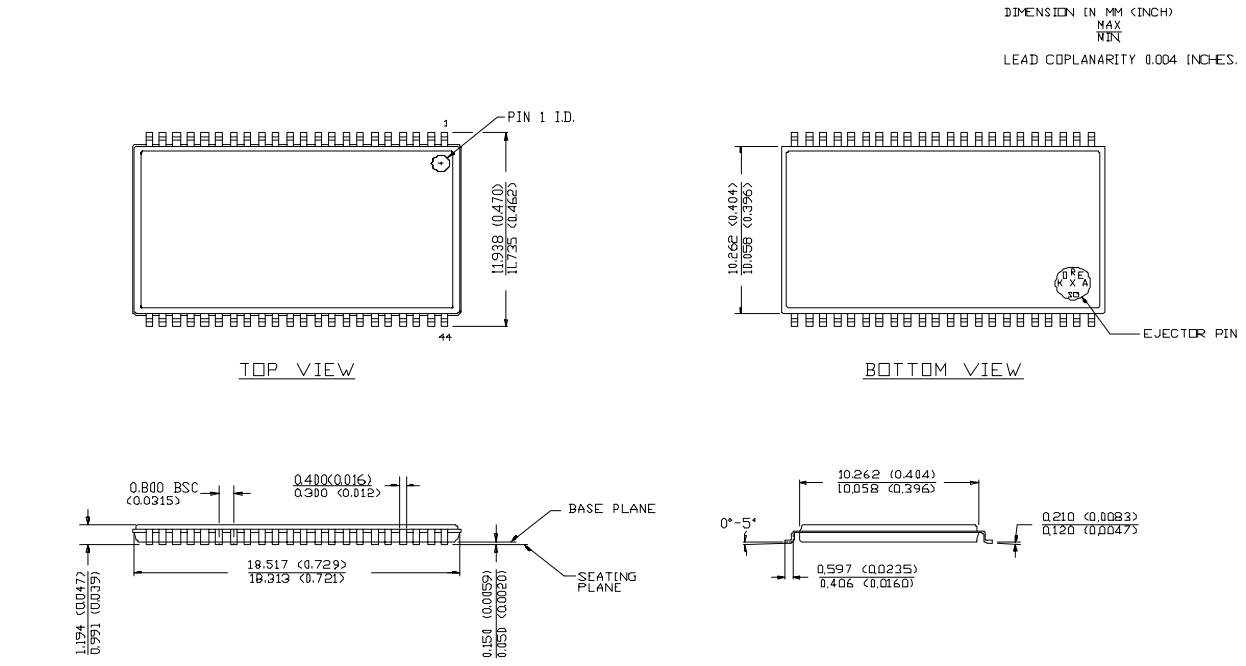
Package Diagrams

44-Pin TSOP II Z44



Package Diagrams (continued)

48-Ball (7.00 mm x 7.00 mm) Mini Ball Grid Array BA48