

Quad D-Type Flip-Flop With Clear

MM74HC175

Description

The MM74HC175 high speed D-type flip-flop with complementary outputs utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads. Information at the D inputs of the MM74HC175 is transferred to the Q and $\bar{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip-flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four $\bar{Q}$ outputs to a logical "1." The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 15 ns
- Wide Operating Supply Voltage Range: 2–6 V
- Low Input Current: 1 μ A Maximum
- Low Quiescent Supply Current: 160 μ A Maximum (74HC)
- High Output Drive Current: 4 mA Minimum (74HC)
- These are Pb-Free Devices

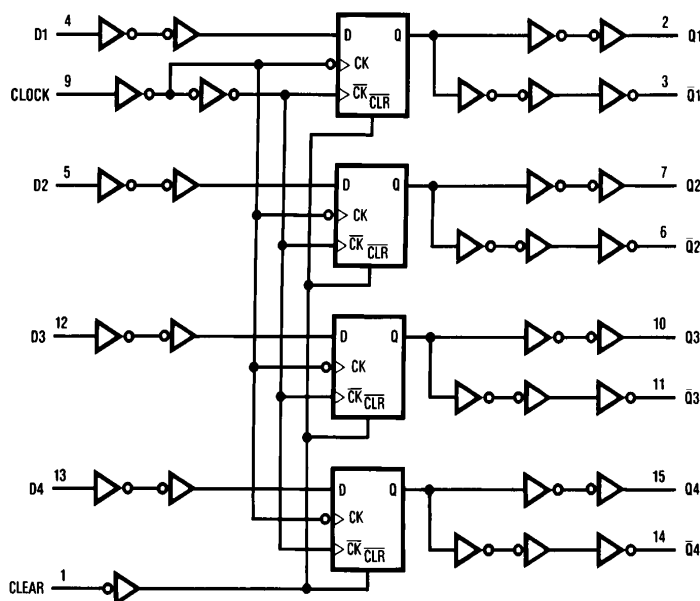
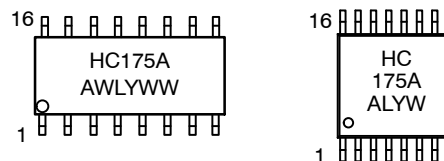


Figure 1. Logic Diagram

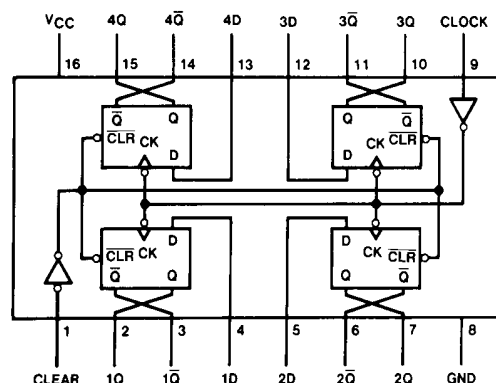


MARKING DIAGRAMS



HC175A = Specific Device Code
A = Assembly Location
L/WL = Wafer Lot
Y/Y = Year of Production, Last Number
W/WW = Work Week Number

CONNECTION DIAGRAM



(Top View)

TRUTH TABLE (Each Flip Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Irrelevant
 $\uparrow$ = Transition from LOW-to-HIGH level
 Q_0 = The level of Q before the indicated steady-state input conditions were established

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.
NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 4.

MM74HC175

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}, I_{OK}	Clamp Diode Current	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC V_{CC} or GND Current, per Pin	± 50	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
P_D	Power Dissipation (Note 2) S. O. Package Only	600 500	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating – plastic “N” package: 12 mW/°C from 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise or Fall Times $V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	– – –	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A –40°C to 85°C	T _A = –55°C to 125°C	Unit
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0	–	1.5	1.5	1.5	V
			4.5	–	3.15	3.15	3.15	
			6.0	–	4.2	4.2	4.2	
V _{IL}	Maximum LOW Level Input Voltage		2.0	–	0.5	0.5	0.5	V
			4.5	–	1.35	1.35	1.35	
			6.0	–	1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
			6.0	6.0	5.9	5.9	5.9	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	4.2	3.98	3.84	3.7	V
			6.0	5.7	5.48	5.34	5.2	
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
			6.0	0	0.1	0.1	0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.2	0.26	0.33	0.4	V
			6.0	0.2	0.26	0.33	0.4	

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DC ELECTRICAL CHARACTERISTICS (Note 3) (continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Unit
				Typ	Guaranteed Limits			
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0	–	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0	–	8	80	160	μA

3. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
f _{MAX}	Maximum Operating Frequency		60	35	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock to Q or $\bar{Q}$		15	25	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Reset to Q or $\bar{Q}$		13	21	ns
t _{REC}	Minimum Removal Time, Clear to Clock		–	20	ns
t _S	Minimum Setup Time, Data to Clock		–	20	ns
t _H	Minimum Hold Time, Data from Clock		–	0	ns
t _W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.0 V to 6.0 V, C_L = 50 pF, t_r = t_f = 6 ns unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A –40°C to 85°C	T _A = –55°C to 125°C	Unit
				Typ	Guaranteed Limits			
f _{MAX}	Maximum Operating Frequency		2.0	12	6	5	4	MHz
			4.5	60	30	24	20	
			6.0	70	35	28	24	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock to Q or $\bar{Q}$		2.0	80	150	190	225	ns
			4.5	15	30	38	45	
			6.0	13	26	32	38	
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Reset to Q or $\bar{Q}$		2.0	64	125	158	186	ns
			4.5	14	25	32	37	
			6.0	12	21	27	32	
t _{REM}	Minimum Removal Time, Clear to Clock		2.0	–	100	125	150	ns
			4.5	–	20	25	30	
			6.0	–	17	21	25	
t _S	Minimum Setup Time, Data to Clock		2.0	–	100	125	150	ns
			4.5	–	20	25	30	
			6.0	–	17	21	25	
t _H	Minimum Hold Time, Data from Clock		2.0	–	0	0	0	ns
			4.5	–	0	0	0	
			6.0	–	0	0	0	
t _W	Minimum Pulse Width, Clock or Clear		2.0	30	80	100	120	ns
			4.5	9	16	20	24	
			6.0	8	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Time		2.0	–	1000	1000	1000	ns
			4.5	–	500	500	500	
			6.0	–	400	400	400	
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0	30	75	95	110	ns
			4.5	9	15	19	22	
			6.0	8	13	16	19	

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AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.0\text{ V to }6.0\text{ V}$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A –40°C to 85°C	T _A = –55°C to 125°C	Unit
				Typ	Guaranteed Limits			
C _{PD}	Power Dissipation Capacitance (Note 4)	(per package)	–	150				pF
			–	–	–	–		
C _{IN}	Maximum Input Capacitance		–	5	10	10	10	pF

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

Device	Package	Shipping [†]
MM74HC175MX	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MM74HC175MTCX	TSSOP-16 (Pb-Free)	2500 Units / Tube

DISCONTINUED (Note 5)

MM74HC175M	SOIC-16 (Pb-Free)	48 Units / Tube
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

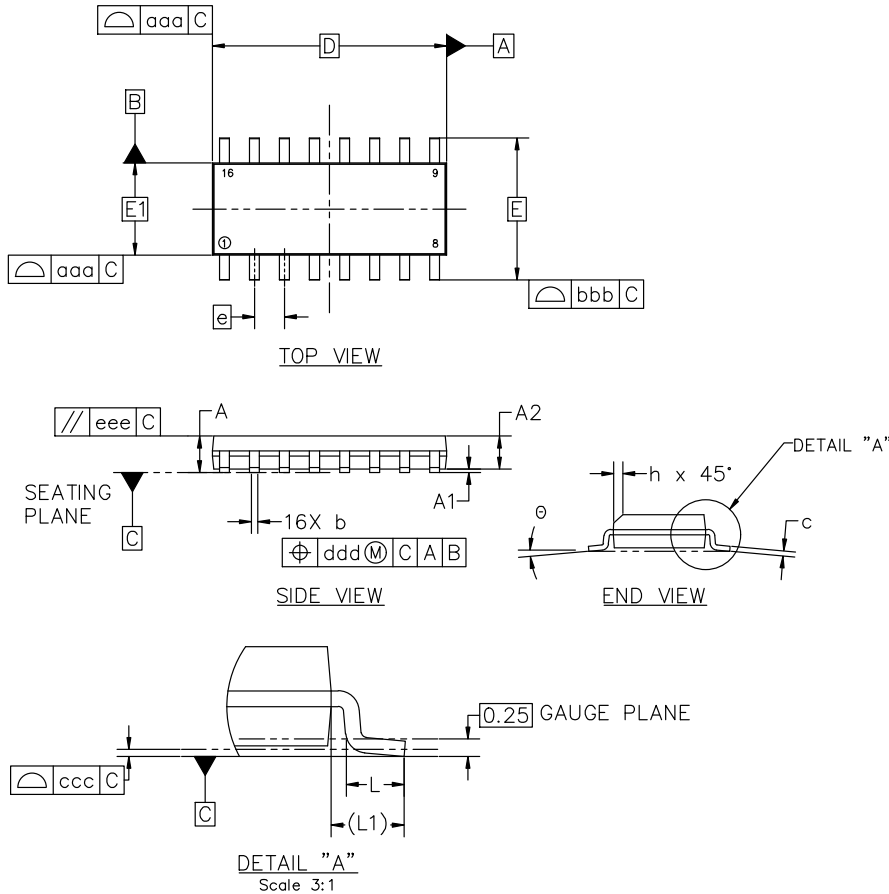
5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

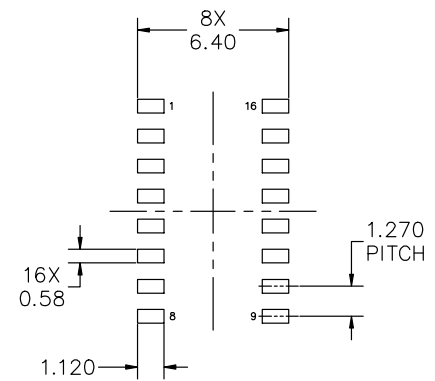
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

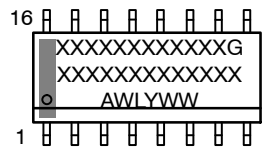
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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*



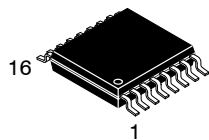
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

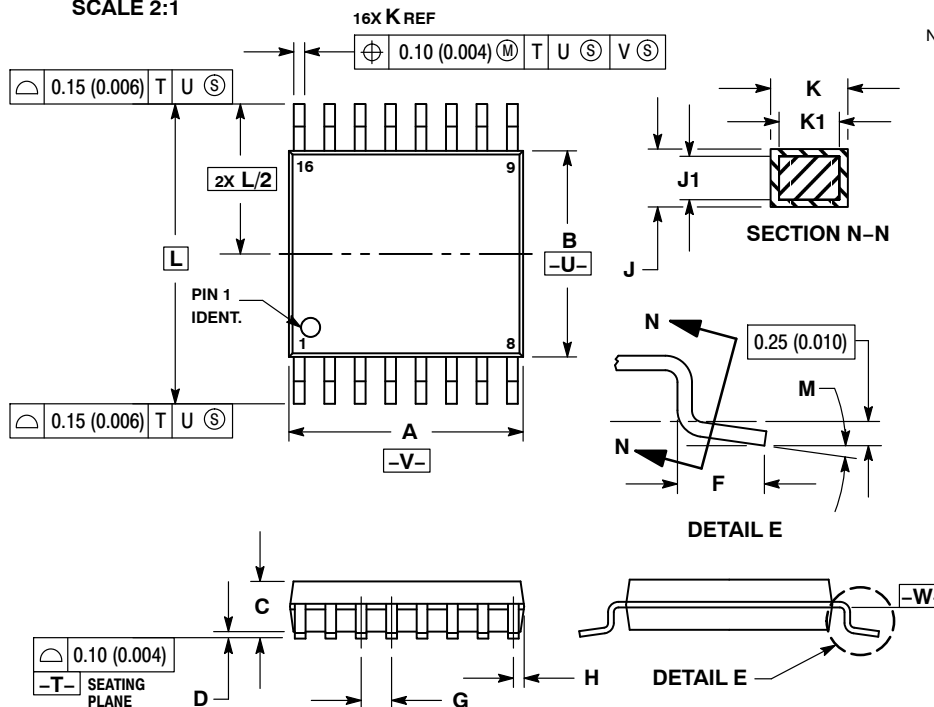
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STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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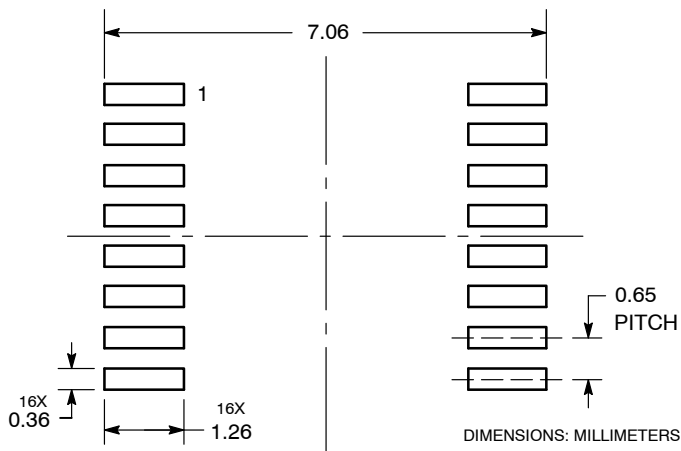
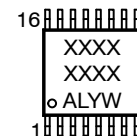

TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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