REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to reflect current requirements. Editorial changes throughout. - gap	01-02-15	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	07-01-29	Joseph Rodenbeck
C	Correction to Table I; ICC2 remove devices 05-07 and 08 from the device type column. ksr	07-06-11	Robert M. Heber

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			
REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
92-07-20

REVISION LEVEL
C

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 8K X 8-BIT PROM, MONOLITHIC SILICON

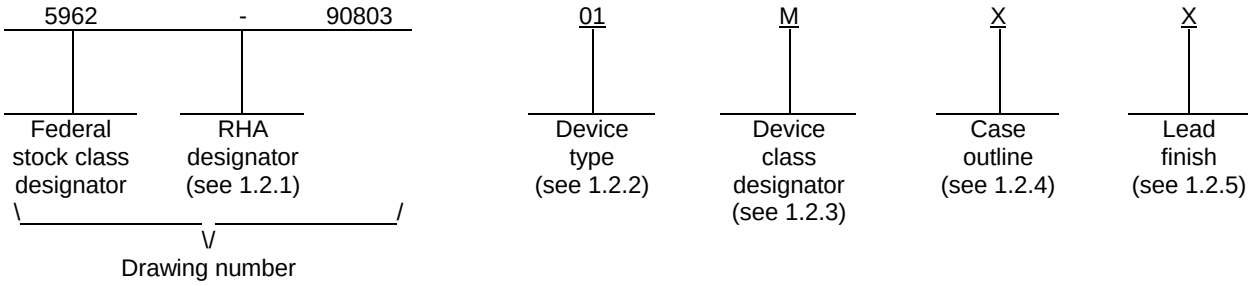
SIZE	CAGE CODE	
A	**67268**	**5962-90803**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C261	8K X 8-bit PROM	55 ns
02	7C261	8K X 8-bit PROM	45 ns
03	7C261	8K X 8-bit PROM	35 ns
04	7C261	8K X 8-bit PROM	25 ns
05	7C263, 7C264	8K X 8-bit PROM	55 ns
06	7C263, 7C264	8K X 8-bit PROM	45 ns
07	7C263, 7C264	8K X 8-bit PROM	35 ns
08	7C263, 7C264	8K X 8-bit PROM	25 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range to ground potential (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC voltage applied to the outputs in the high-Z state ..... -0.5 V dc to +7.0 V dc
DC input voltage ..... -3.0 V dc to +7.0 V dc
DC program voltage ..... 13.0 V dc
Maximum power dissipation ..... 1.0 W 2/
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... +4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) ..... 0 V dc
Input high voltage (V_{IH}) ..... 2.0 V dc minimum
Input low voltage (V_{IL}) ..... 0.8 V dc maximum 3/
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

_____
1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
3/ V_{IL} negative undershoots to a minimum of -3.0 V dc are allowed for pulse widths < 10 ns.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.10.1 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.10.2 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.3 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guaranteed over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$	I_{OH} = -4 mA	1, 2, 3	01-03 05-07	2.4		V
			I_{OH} = -2 mA		04, 08			
Output low voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$	I_{OL} = 16 mA	1, 2, 3	01-03 05-07		0.4	V
			I_{OL} = 6 mA		04, 08			
Input high voltage 1/	V_{IH}			1, 2, 3	All	2.0		V
Input low voltage 1/	V_{IL}			1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	$V_{IN} = V_{CC}$ to GND		1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	$V_{OUT} = V_{CC}$ to GND		1, 2, 3	All	-10	10	µA
Output short circuit current 2/, 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND		1, 2, 3	All		-100	mA
Power supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 0 to 3.0 V, f = f_{MAX} 4/		1, 2, 3	01-03 05-07		120	mA
					04, 08		140	
Standby supply current	I_{CC2}	V_{CC} = 5.5 V, $\overline{CS} \ge V_{IH}$ I_{OUT} = 0 mA		1, 2, 3	01-03		30	mA
					04		50	
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V T_A = +25°C, f = 1 MHz (see 4.4.1d)		4	All		10	pF
Output capacitance 3/	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V T_A = +25°C, f = 1 MHz (see 4.4.1d)		4	All		10	pF
Functional tests		See 4.4.1c		7, 8	All			
Address to output valid	t_{AA}	See figures 3 and 4 and note 5/		9, 10, 11	01, 05		55	ns
					02, 06		45	
					03, 07		35	
					04, 08		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip select active to output valid	t_{ACS}	See figures 3 and 4 and note 5/	9, 10, 11	01		55	ns
				02		45	
				03		40	
				04		25	
				05		35	
				06		30	
				07		20	
				08		15	
Chip select active to power-up 3/	t_{PU}		9, 10, 11	01-04	0		ns
Chip select inactive to power-down 3/	t_{PD}		9, 10, 11	01		55	ns
				02		45	
				03		35	
				04		25	
Chip select inactive to high-Z 3/	t_{HZCS}	See figures 3 and 4 and note 5/ and 6/	9, 10, 11	01		55	ns
				02		45	
				03, 05		35	
				04, 07		25	
				06		30	
				08		15	

1/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ At $f = f_{max}$, address inputs are cycling at the maximum frequency of $1/t_{AA}$.
5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4.
6/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input, $C_L = 5$ pF (including scope and jig). See figure 4.

Device types	All	
Case outlines	J, K, and L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	A_{12}	O_5
19	A_{11}	O_6
20	$\overline{CS}$	O_7
21	A_{10}	NC
22	A_9	A_{12}
23	A_8	A_{11}
24	V_{CC}	$\overline{CS}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Type	Mode	Outputs	A_{12}	A_{11}	$\overline{CS}$	A_{10}	A_9	A_8	V_{CC}	Power
All	Read	D_{OUT}	A_{12}	A_{11}	V_{IL}	A_{10}	A_9	A_8	V_{CC}	I_{CC}
01-04	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{SB}
05-08	Not selected	High-Z	A_{12}	A_{11}	V_{IH}	A_{10}	A_9	A_8	V_{CC}	I_{CC}
All	Program 1/	D_{IN}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{ILP}	V_{IHP}	V_{CCP}	I_{CC}
All	Program inhibit 1/	High-Z	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{IHP}	V_{CC}	I_{CC}
All	Program verify 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC}
All	Blank check 1/	D_{OUT}	V_{ILP}	V_{PP}	V_{ILP}	Latch	V_{IHP}	V_{ILP}	V_{CC}	I_{CC}

1/ See 4.5.

FIGURE 2. Truth table.

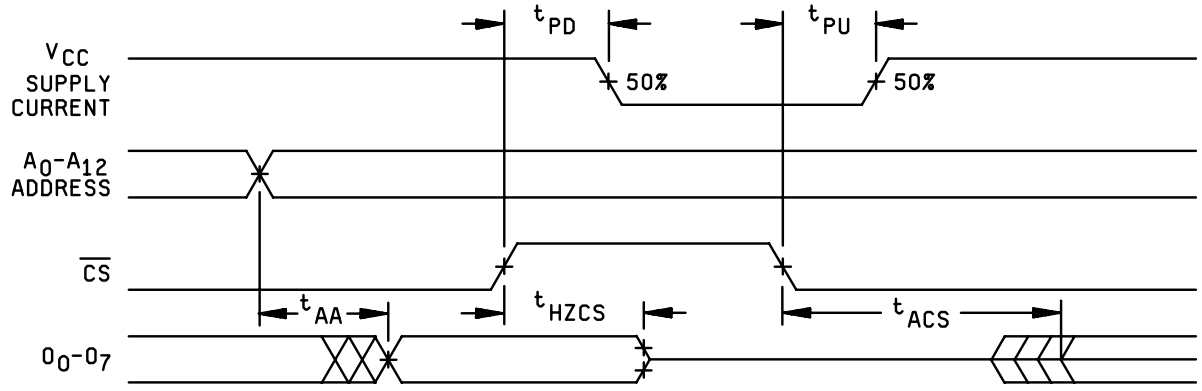
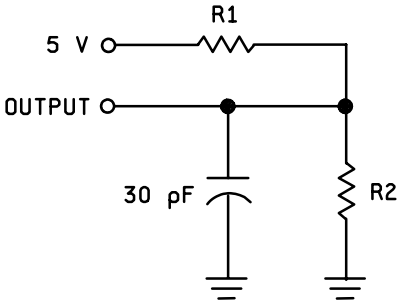
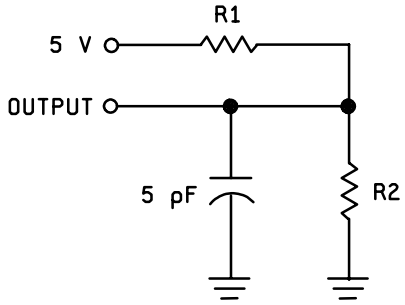


FIGURE 3. Switching waveforms.



Circuit A
Output load



Circuit B
Output load for t_{HZCS}

NOTE: Including scope and jig. (minimum values)

	Device types	
Load	01-03, 05-07	04, 08
R1	250 Ω	658 Ω
R2	167 Ω	403 Ω

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuit and test conditions.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

e. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 4.4). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

f. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements. 1/, 2/, 3/, 4/, 5/

Line No.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			(1, 7, 9) or (2, 8A, 10)
2	Static burn-in I method 1015	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ * indicates PDA applies to subgroup 1 and 7.
4/ ** see 4.4.1d.
5/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC2} standby	±10 percent of specified value in table I
I_{IX}	±10 percent of specified value in table I
I_{OZ}	±10 percent of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-06-11

Approved sources of supply for SMD 5962-90803 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9080301MKA	0C7V7	WS57C49C-55HMB
	0C7V7	QP7C261-55KMB
	3/	CY7C261-55KMB
5962-9080301MLA	0C7V7	WS57C49C-55KMB
	0C7V7	QP7C261-55DMB
	3/	CY7C261-55DMB
5962-9080301M3A	0C7V7	WS57C49C-55ZMB
	0C7V7	QP7C261-55LMB
	3/	CY7C261-55LMB
5962-9080301M3C	0C7V7	WS57C49C-55ZMB
5962-9080302MKA	0C7V7	WS57C49C-45HMB
	0C7V7	QP7C261-45KMB
	3/	CY7C261-45KMB
5962-9080302MLA	0C7V7	WS57C49C-45KMB
	0C7V7	QP7C261-45DMB
	0C7V7	CY7C261-45DMB
5962-9080302M3A	0C7V7	WS57C49C-45ZMB
	0C7V7	QP7C261-45LMB
	3/	CY7C261-45LMB
5962-9080302M3C	0C7V7	WS57C49C-45ZMB
5962-9080303MKA	0C7V7	WS57C49C-35HMB
	0C7V7	QP7C261-35KMB
	3/	CY7C261-35KMB
5962-9080303MLA	0C7V7	WS57C49C-35KMB
	0C7V7	QP7C261-35DMB
	0C7V7	CY7C261-35DMB
	65786	CY7C261-35DMB
5962-9080303M3A	0C7V7	WS57C49C-35ZMB
	0C7V7	QP7C261-35LMB
	3/	CY7C261-35LMB
5962-9080303M3C	0C7V7	WS57C49C-35ZMB
5962-9080304MKA	0C7V7	QP7C261-25KMB
	0C7V7	CY7C261-25KMB
5962-9080304MLA	0C7V7	QP7C261-25DMB
	3/	CY7C261-25DMB
5962-9080304M3A	0C7V7	QP7C261-25LMB
	0C7V7	CY7C261-25LMB
5962-9080305MJA	0C7V7	WS57C49C-55YMB
	0C7V7	QP7C264-55DMB
	3/	CY7C264-55DMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9080305MKA	0C7V7	WS57C49C-55HMB
	0C7V7	QP7C263-55KMB
	3/	CY7C263-55KMB
5962-9080305MLA	0C7V7	WS57C49C-55KMB
	0C7V7	QP7C263-55DMB
	3/	CY7C263-55DMB
5962-9080305M3A	0C7V7	WS57C49C-55ZMB
	0C7V7	QP7C263-55LMB
	3/	CY7C263-55LMB
5962-9080305M3C	0C7V7	WS57C49C-55ZMB
5962-9080306MJA	0C7V7	WS57C49C-45YMB
	0C7V7	QP7C264-45DMB
	3/	CY7C264-45DMB
5962-9080306MKA	0C7V7	WS57C49C-45HMB
	0C7V7	QP7C263-45KMB
	3/	CY7C263-45KMB
5962-9080306MLA	0C7V7	WS57C49C-45KMB
	0C7V7	QP7C263-45DMB
	3/	CY7C263-45DMB
5962-9080306M3A	0C7V7	WS57C49C-45ZMB
	0C7V7	QP7C263-45LMB
	3/	CY7C263-45LMB
5962-9080306M3C	0C7V7	WS57C49C-45ZMB
5962-9080307MJA	0C7V7	WS57C49C-35YMB
	0C7V7	QP7C264-35DMB
	3/	CY7C264-35DMB
5962-9080307MKA	0C7V7	WS57C49C-35HMB
	0C7V7	QP7C263-35KMB
	3/	CY7C263-35KMB
5962-9080307MLA	0C7V7	WS57C49C-35KMB
	0C7V7	QP7C261-35DMB
	3/	CY7C263-35DMB
5962-9080307M3A	0C7V7	WS57C49C-35ZMB
	0C7V7	QP7C263-35LMB
	3/	CY7C263-35LMB
5962-9080307M3C	0C7V7	WS57C49C-35ZMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9080308MJA	0C7V7	QP7C264-25DMB
	0C7V7	CY7C264-25DMB
5962-9080308MKA	0C7V7	QP7C263-25KMB
	0C7V7	CY7C263-25KMB
5962-9080308MLA	0C7V7	QP7C263-25DMB
	0C7V7	CY7C263-25DMB
5962-9080308M3A	0C7V7	QP7C263-25LMB
	0C7V7	CY7C263-25LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Ct. Santa Clara, CA 95051-0812
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.