



CYPRESS

CY7C194
CY7C195
CY7C196

64K x 4 Static RAM

Features

- High speed
— 12 ns
- Output enable (OE) feature (7C195 and 7C196)
- CMOS for optimum speed/power
- Low active power
— 880 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

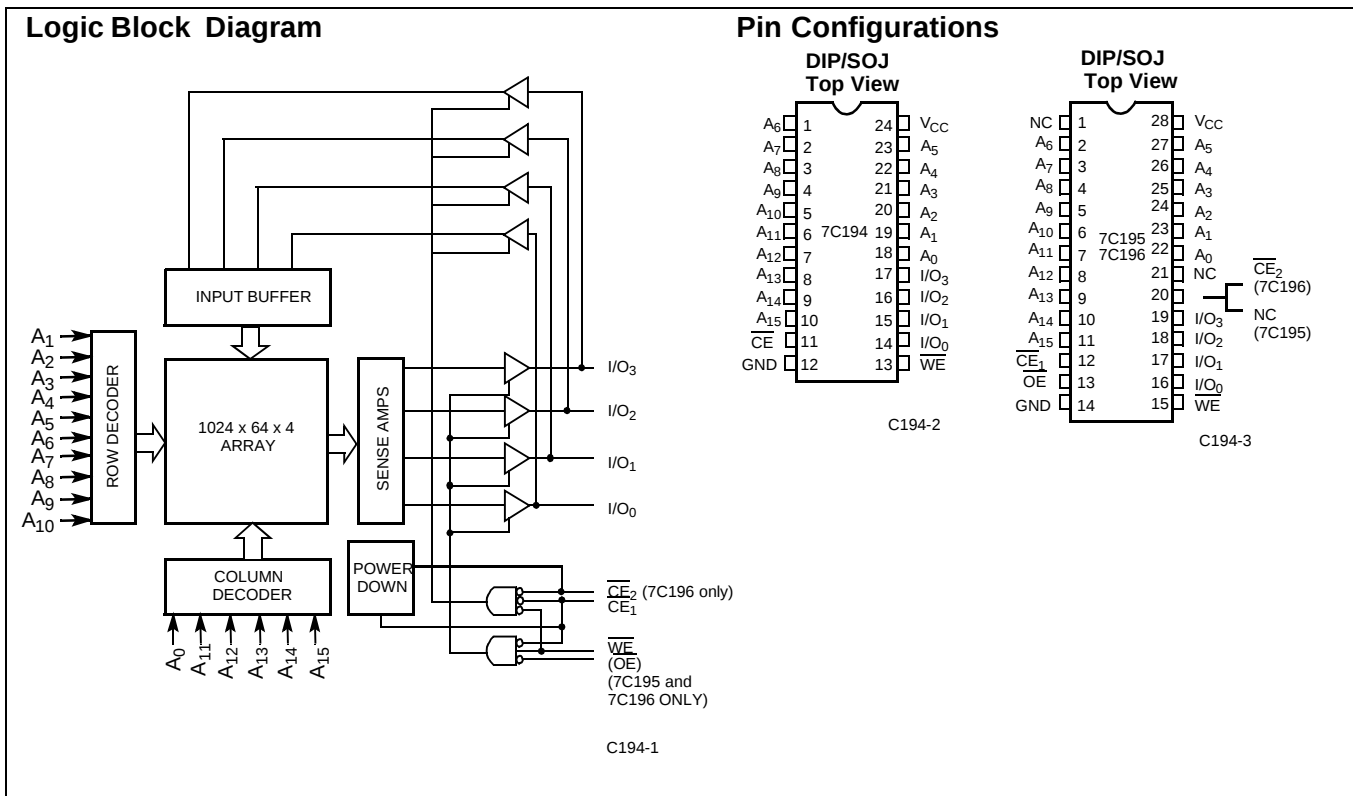
The CY7C194, CY7C195, and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW Chip En-

able(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the Chip Enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) is written into the memory location, specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the Chip Enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) LOW, while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

A die coat is used to ensure alpha immunity.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential..... -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}^{[1]}$	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.},$ $V_{OUT} = GND$		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		155		145	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs ^[4]	Max. $V_{CC}, \overline{CE}_{1,2} \geq V_{IH},$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs ^[4]	Max. $V_{CC}, \overline{CE}_{1,2} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$		10		10	mA

Notes:

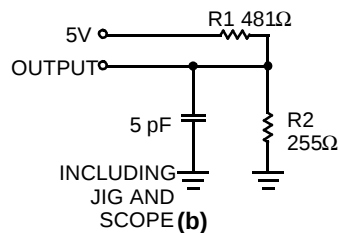
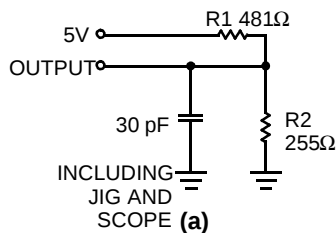
1. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range (continued)

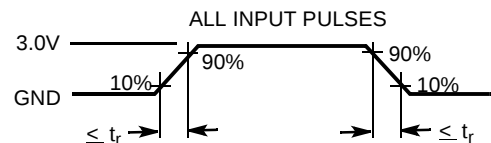
Parameter	Description	Test Conditions	7C194-20 7C195-20 7C196-20		7C194-25, 35, 45 7C195-25, 35 7C196-25, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.},$ $V_{OUT} = GND$		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		135		115	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs ^[4]	Max. $V_{CC}, \overline{CE}_{1,2} \geq V_{IH},$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs ^[4]	Max. $V_{CC}, \overline{CE}_{1,2} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0$		15		15	mA

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms^[6]


C194-4



C194-5

Equivalent to: THÉVENIN EQUIVALENT
 167Ω
 OUTPUT $\text{---} \text{---} \text{---} 1.73V$

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- $t_r \leq 3 \text{ ns}$ for the -12 and -15 speeds. $t_r \leq 5 \text{ ns}$ for the -20 and slower speeds.

Switching Characteristics Over the Operating Range^[7]

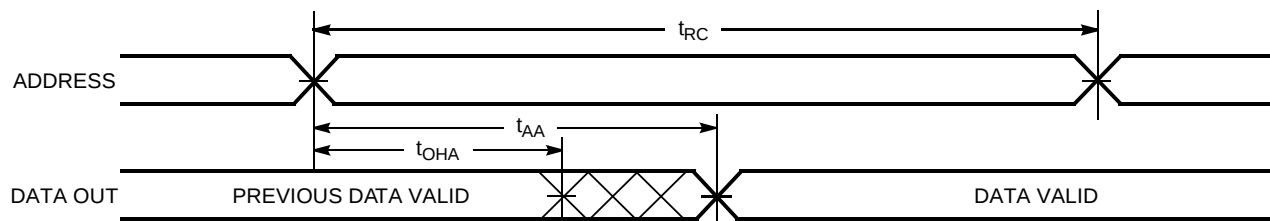
Parameter	Description		7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		7C194-20 7C195-20 7C196-20		7C194-25 7C195-25 7C196-25		7C194-35 7C195-35 7C196-35		7C194-45 7C196-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE															
t _{RC}	Read Cycle Time		12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid			12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change		3		3		3		3		3		3		ns
t _{ACE1} , t _{ACE2}	$\overline{\text{CE}}$ LOW to Data Valid			12		15		20		25		35		45	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	7C195, 7C196		5		7		9		10		16		16	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	7C195, 7C196	0		0		0		3		3		3		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[8]	7C195, 7C196		5		7		9		11		15		15	ns
t _{LZCE1} , t _{LZCE2}	$\overline{\text{CE}}$ LOW to Low Z ^[8]		3		3		3		3		3		3		ns
t _{HZCE1} , t _{HZCE2}	$\overline{\text{CE}}$ HIGH to High Z ^[8,8]			5		7		9		11		15		15	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up		0		0		0		0		0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down			12		15		20		25		35		45	ns
WRITE CYCLE ^[10]															
t _{WC}	Write Cycle Time		12		15		20		25		35		45		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End		9		10		15		18		22		22		ns
t _{AW}	Address Set-Up to Write End		9		10		15		20		25		35		ns
t _{HA}	Address Hold from Write End		0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start		0		0		0		0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width		8		9		15		18		22		22		ns
t _{SD}	Data Set-Up to Write End		8		9		10		10		15		15		ns
t _{HD}	Data Hold from Write End		0		0		0		0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[8]		3		3		3		3		3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[8, 9]			7		7		10	0	13	0	15	0	20	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of CE₁ LOW, CE₂ LOW, and WE LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

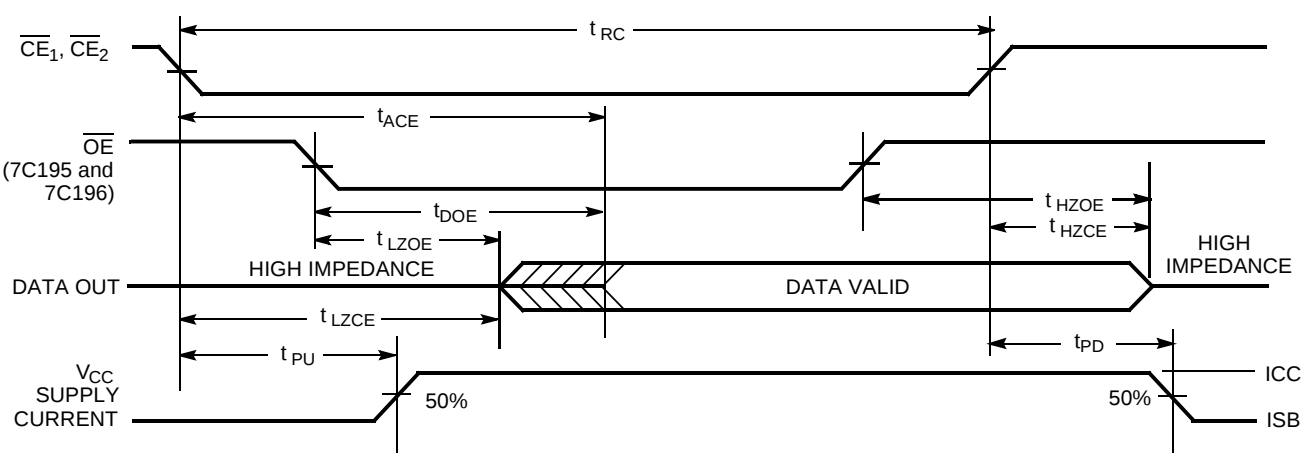
Switching Waveforms

Read Cycle No. 1^[11, 12]



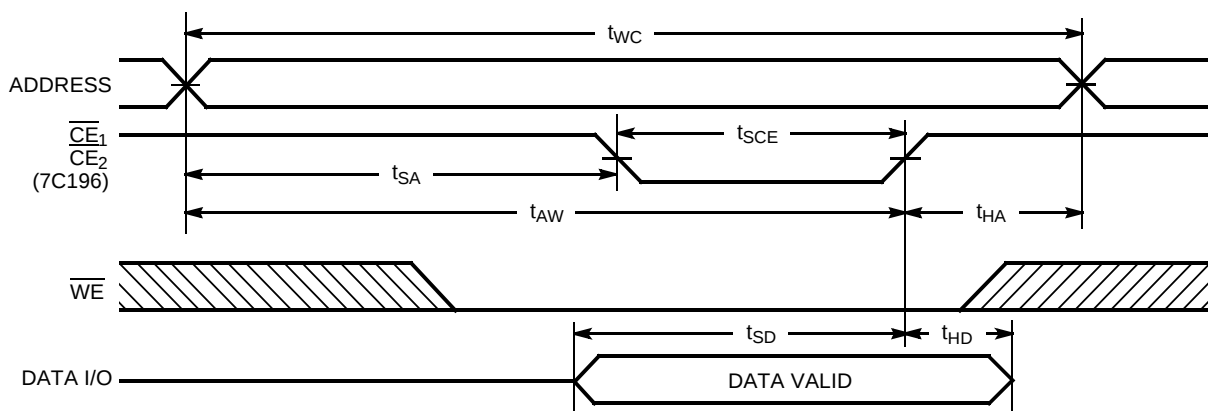
C194-8

Read Cycle No. 2^[11, 13]



C194-6

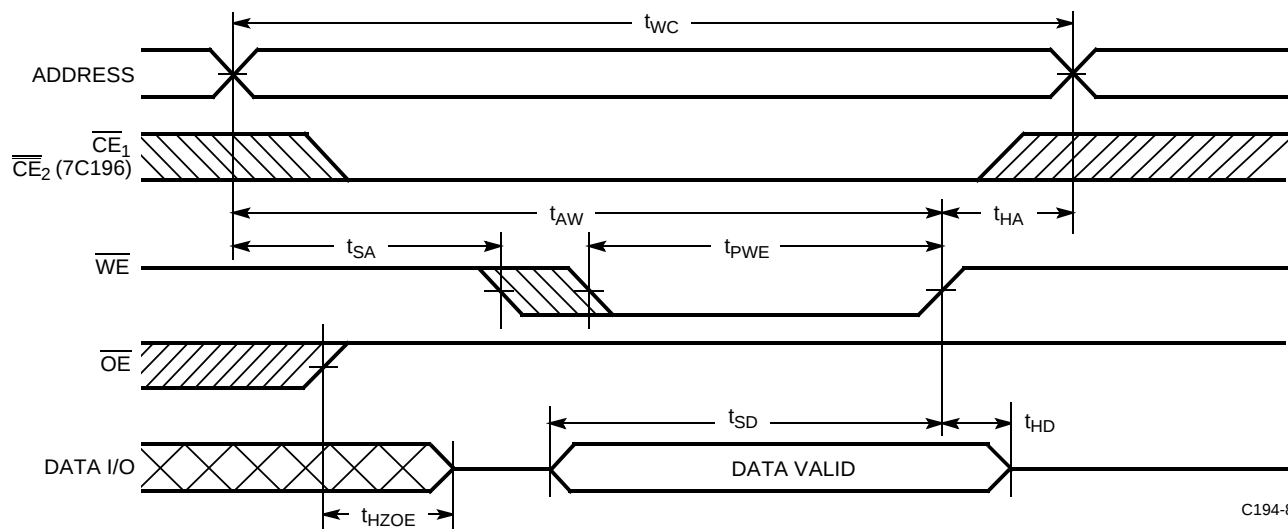
Write Cycle No. 1 (CE Controlled)^[10, 14, 15]



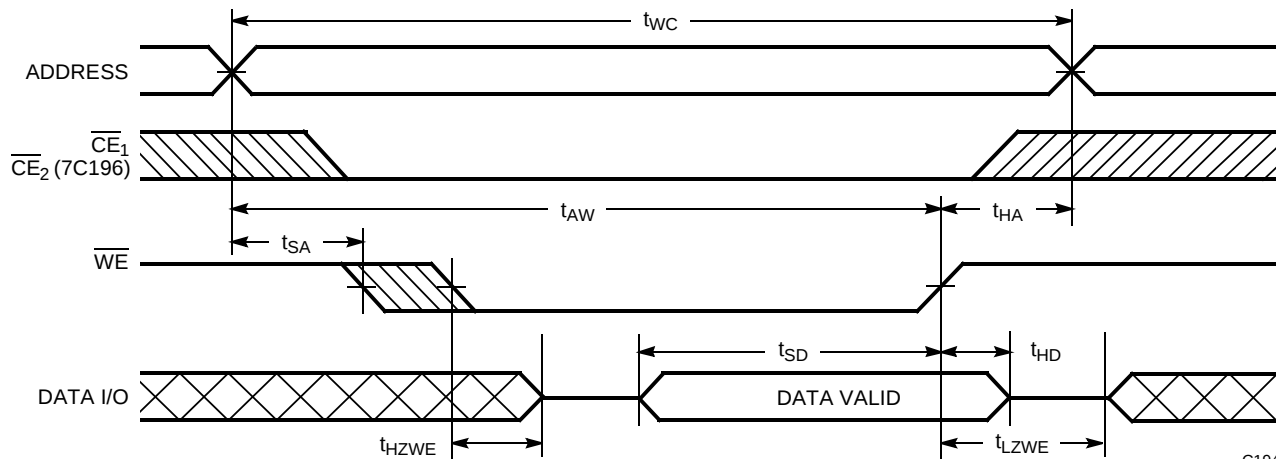
C194-7

Notes:

11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected: $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IL}$ (7C196), and $\overline{OE} = V_{IL}$ (7C195 and 7C196).
13. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition LOW.
14. Data I/O will be high impedance if $\overline{OE} = V_{IH}$ (7C195 and 7C196).
15. If any CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for 7C195 and 7C196 only) ^[10, 14, 15]


C194-8

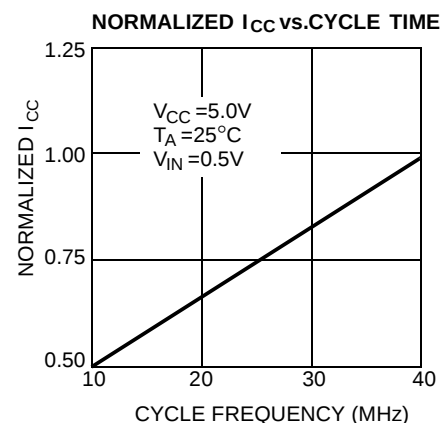
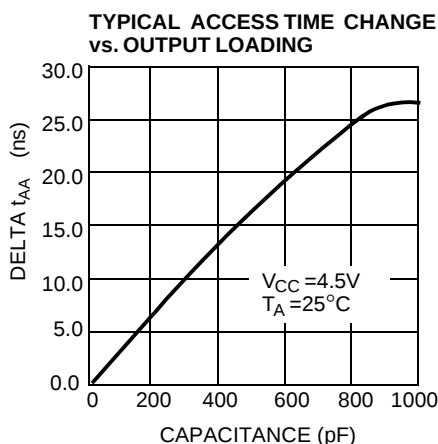
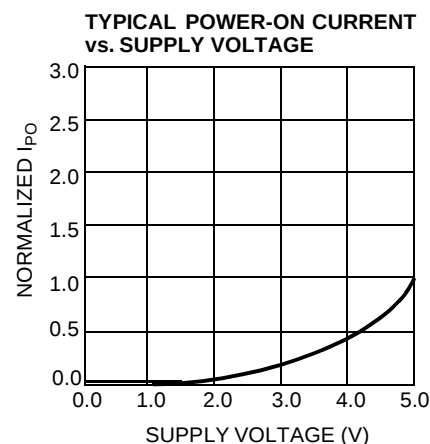
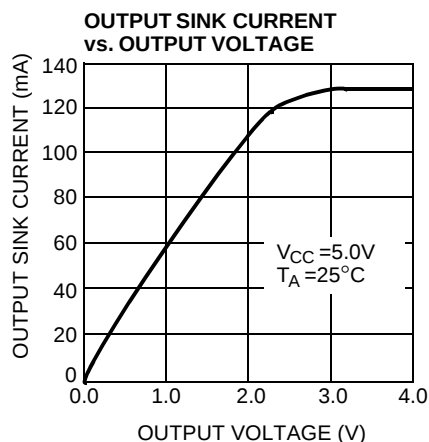
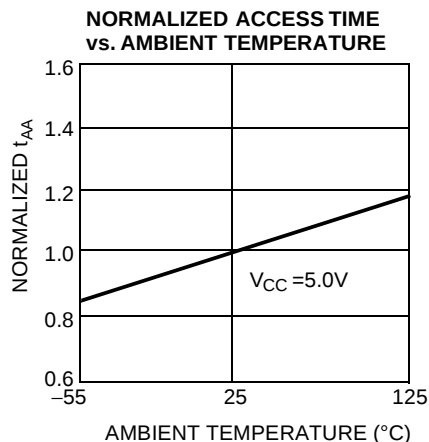
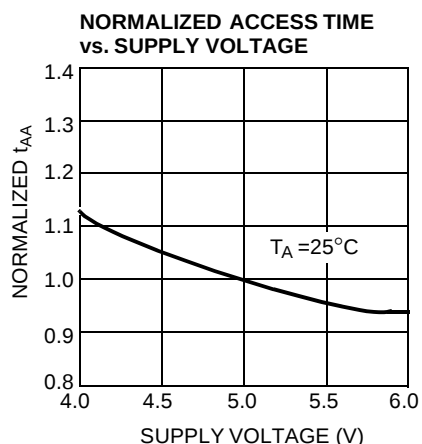
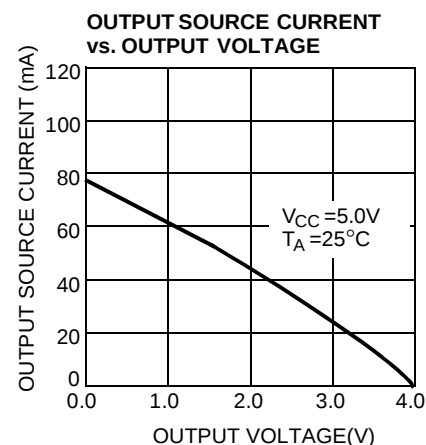
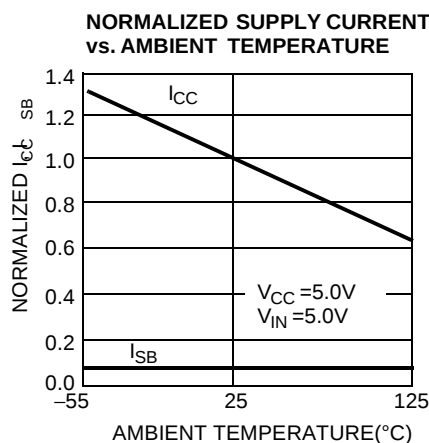
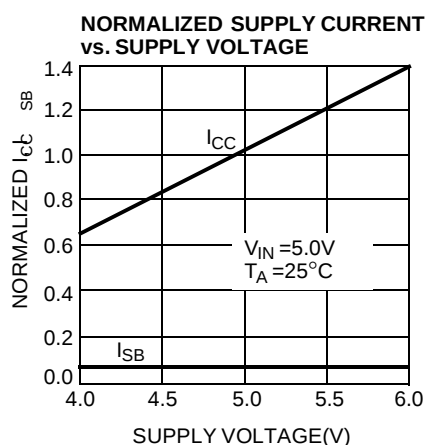
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) ^[15, 16]


C194-9

Note:

16. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Typical DC and AC Characteristics



7C194 Truth Table

CE	WE	Data I/O	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7C195 Truth Table

CE₁	WE	OE	Data I/O	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect	Active (I_{CC})

7C196 Truth Table

CE₁	CE₂	WE	OE	Data I/O	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	H	X	X			
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Deselect	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C194-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-12VC	V13	24-Lead Molded SOJ	
15	CY7C194-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-15VC	V13	24-Lead Molded SOJ	
20	CY7C194-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-20VC	V13	24-Lead Molded SOJ	
25	CY7C194-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-25VC	V13	24-Lead Molded SOJ	
35	CY7C194-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-35VC	V13	24-Lead Molded SOJ	
45	CY7C194-45PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-45VC	V13	24-Lead Molded SOJ	

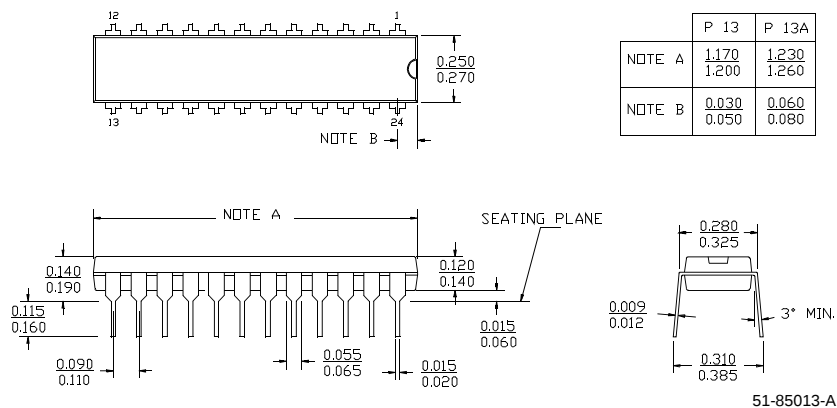
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C195-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-12VC	V21	28-Lead Molded SOJ	
15	CY7C195-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-15VC	V21	28-Lead Molded SOJ	
20	CY7C195-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-20VC	V21	28-Lead Molded SOJ	
25	CY7C195-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-25VC	V21	28-Lead Molded SOJ	
35	CY7C195-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-35VC	V21	28-Lead Molded SOJ	
45	CY7C195-45PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-45VC	V21	28-Lead Molded SOJ	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C196-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-12VC	V21	28-Lead Molded SOJ	
15	CY7C196-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-15VC	V21	28-Lead Molded SOJ	
20	CY7C196-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-20VC	V21	28-Lead Molded SOJ	
25	CY7C196-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-25VC	V21	28-Lead Molded SOJ	
35	CY7C196-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-35VC	V21	28-Lead Molded SOJ	

Package Diagrams

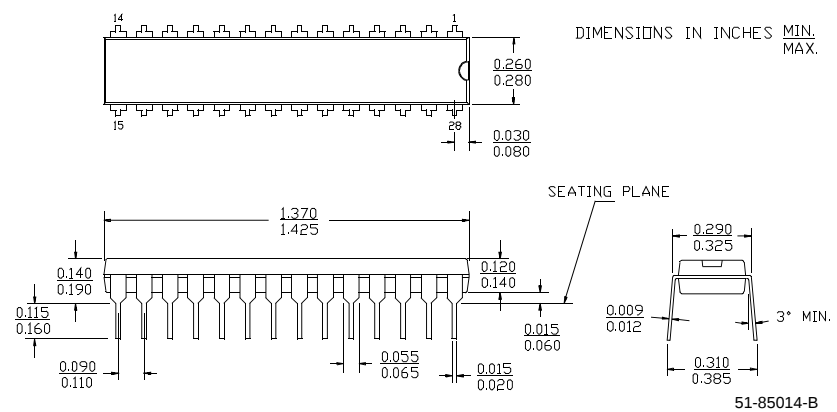
24-Lead (300-Mil) Molded DIP P13/P13A

DIMENSIONS IN INCHES MIN.
MAX.



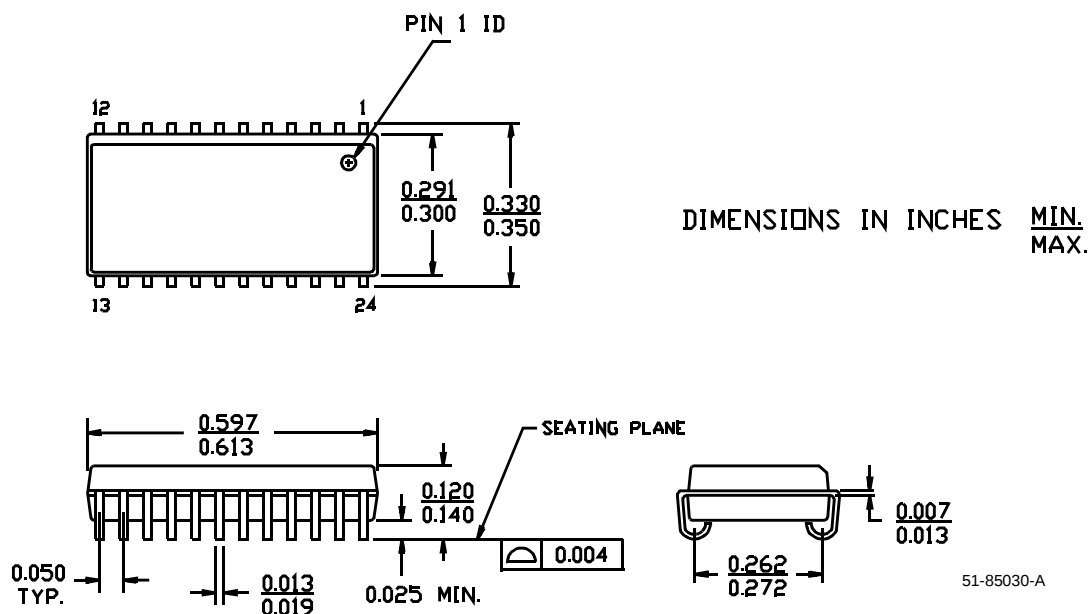
28-Lead (300-Mil) Molded DIP P21

DIMENSIONS IN INCHES MIN.
MAX.

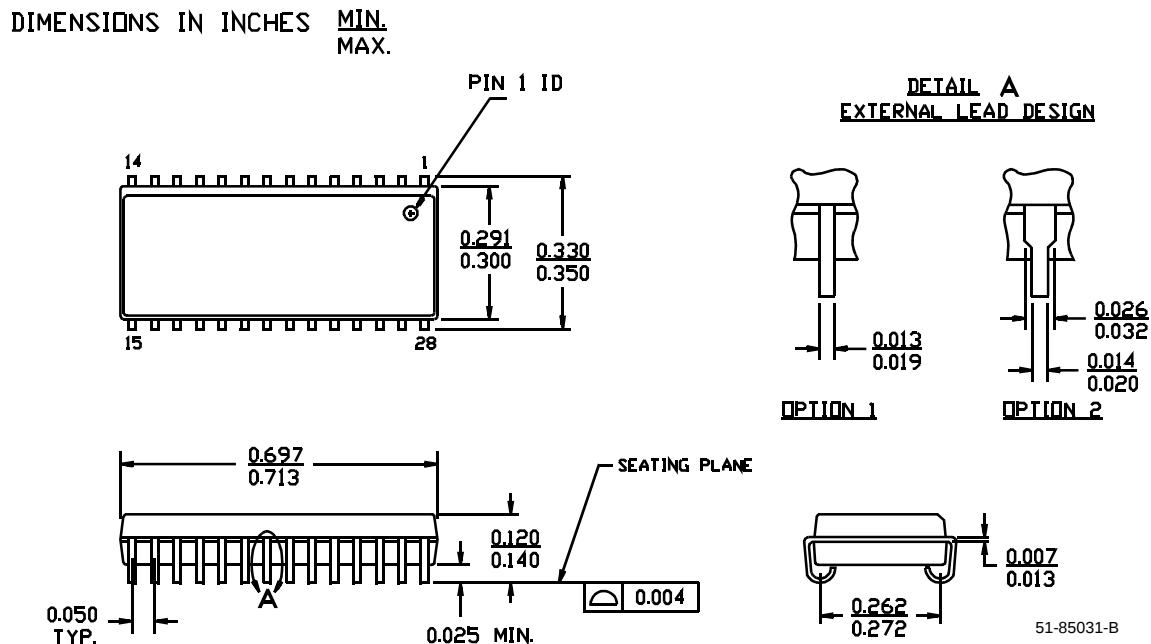


Package Diagrams (continued)

24-Lead (300-Mil) Molded SOJ V13



28-Lead (300-Mil) Molded SOJ V21





CY7C194

CY7C195

CY7C196

Document Title: CY7C194/CY7C195/CY7C196 64K x 4 Static RAM
Document Number: 38-05162

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110172	09/29/01	SZV	Change from Spec number: 38-00081 to 38-05162