MT9042B

Multitrunk System Synchronizer

Preliminary Information

ISSUE 1 October 1996

Ordering Information

MT9042BP 28 Pin PLCC

-40°C to +85°C

Features

- Meets jitter requirements for AT&T TR62411 Stratum 3, 4 and Stratum 4 Enhanced for DS1 interfaces and for ETSI ETS 300 011 for E1 interfaces
- Provides C1.5, $\overline{C3}$, C2, $\overline{C4}$, C8 and $\overline{C16}$ output clock signals
- Provides 8kHz ST-BUS framing signals
- Selectable 1.544MHz, 2.048MHz or 8kHz input reference signals
- Accepts reference inputs from two independent sources
- Provides bit error free reference switching - meets phase slope and MTIE requirements
- Operates in either Normal, Holdover and Freerun modes

Applications

- Synchronization and timing control for multitrunk T1 and E1 systems
- ST-BUS clock and frame pulse sources
- Primary Trunk Rate Converters

Description

The MT9042B Multitrunk System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for multitrunk T1 and E1 primary rate transmission links.

The MT9042B generates ST-BUS clock and framing signals that are phase locked to either a 2.048MHz, 1.544MHz, or 8kHz input reference.

The MT9042B is compliant with AT&T TR62411 Stratum 3, 4 and 4 Enhanced, and ETSI ETS 300 011. It will meet the jitter tolerance, jitter transfer, intrinsic jitter, frequency accuracy, holdover accuracy, capture range, phase slope and MTIE requirements for these specifications.

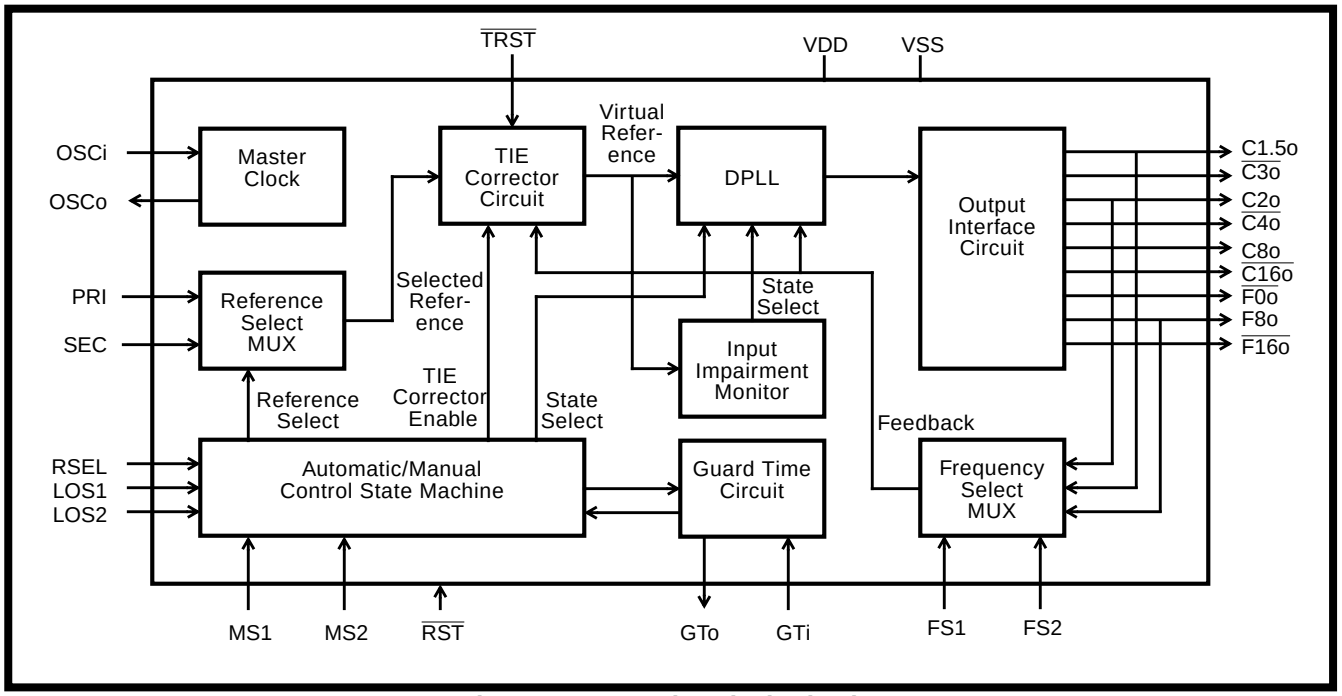

Figure 1 - Functional Block Diagram

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