

General Description

- Trench Power MOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

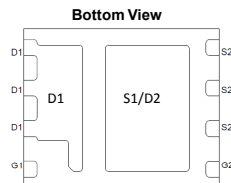
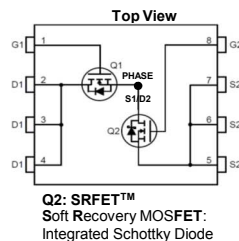
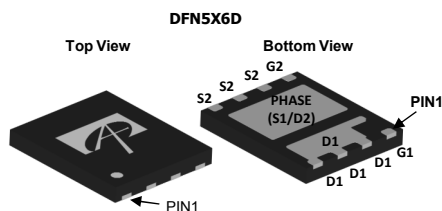
Applications

- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

	Q1	Q2
V_{DS}	30V	30V
I_D (at $V_{GS}=10V$)	50A	85A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 5.2m Ω	< 2m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 8.6m Ω	< 2.5m Ω

100% UIS Tested
100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6992	DFN 5x6D	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	V_{DS}	30	30	V
Gate-Source Voltage	V_{GS}	± 20	± 12	V
Continuous Drain Current ^G	I_D	50	85	A
Current ^G	I_D	31	67	
Pulsed Drain Current ^C	I_{DM}	100	260	
Continuous Drain Current	I_{DSM}	19	31	A
Current	I_{DSM}	15	25	
Avalanche Current ^C	I_{AS}	38	80	A
Avalanche energy $L=0.01\text{mH}$ ^C	E_{AS}	7	32	mJ
V_{DS} Spike	V_{SPIKE}	36	36	V
Power Dissipation ^B	P_D	21	45	W
	P_D	8	18	
Power Dissipation ^A	P_{DSM}	3.1	3.1	W
	P_{DSM}	2	2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	30	40	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	50	50	65	65	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	4.6	2.2	6	2.8	$^\circ\text{C/W}$

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	ID=250μA, VGS=0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.2	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		4.3 6.3	5.2 7.6	mΩ
		V _{GS} =4.5V, I _D =20A		6.8	8.6	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		67		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.71	1	V
I _S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		820		pF
C _{oss}	Output Capacitance			340		pF
C _{rss}	Reverse Transfer Capacitance			40		pF
R _g	Gate resistance	f=1MHz	0.6	1.2	1.8	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		13		nC
Q _g (4.5V)	Total Gate Charge			6.1		nC
Q _{gs}	Gate Source Charge			2		nC
Q _{gd}	Gate Drain Charge			2.4		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		6.5		ns
t _r	Turn-On Rise Time			16.5		ns
t _{D(off)}	Turn-Off DelayTime			17		ns
t _f	Turn-Off Fall Time			2.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		11		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		19		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

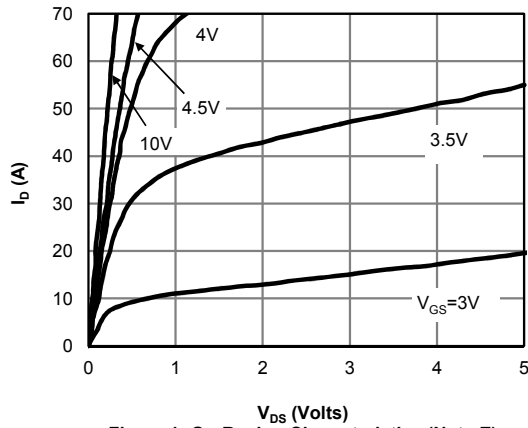


Figure 1: On-Region Characteristics (Note E)

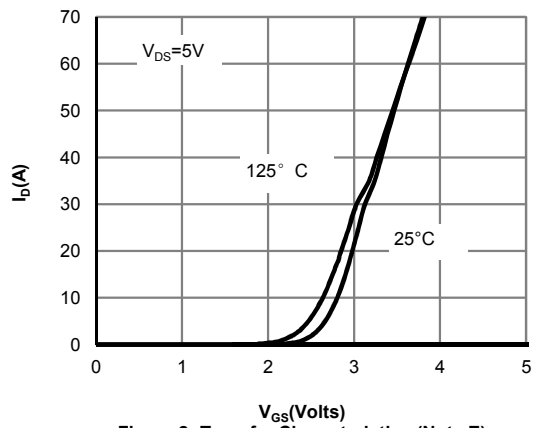


Figure 2: Transfer Characteristics (Note E)

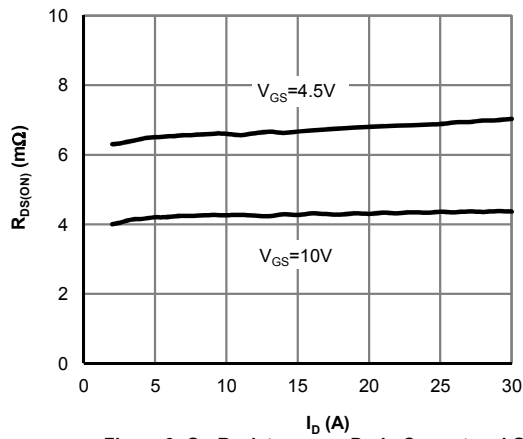


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

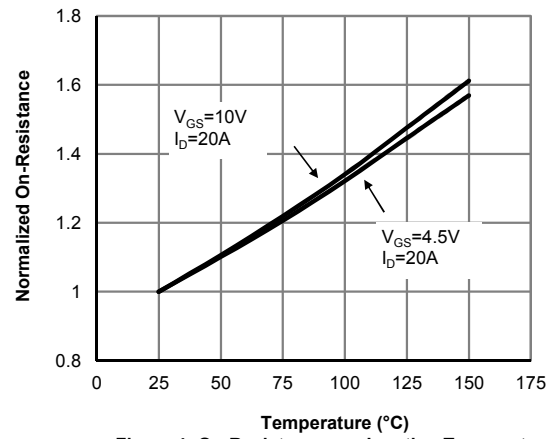


Figure 4: On-Resistance vs. Junction Temperature (Note E)

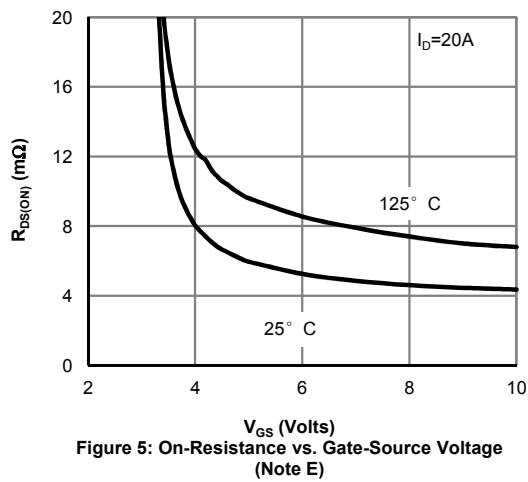


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

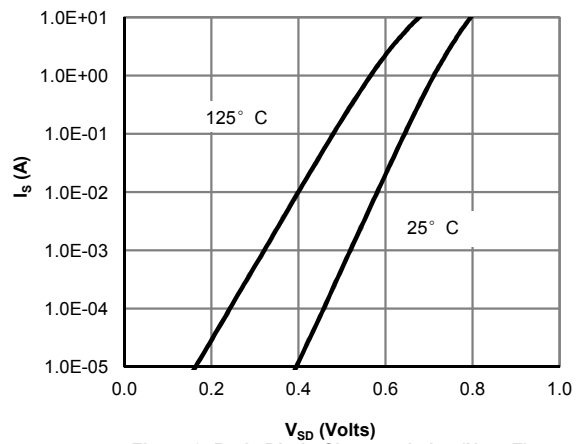


Figure 6: Body-Diode Characteristics (Note E)

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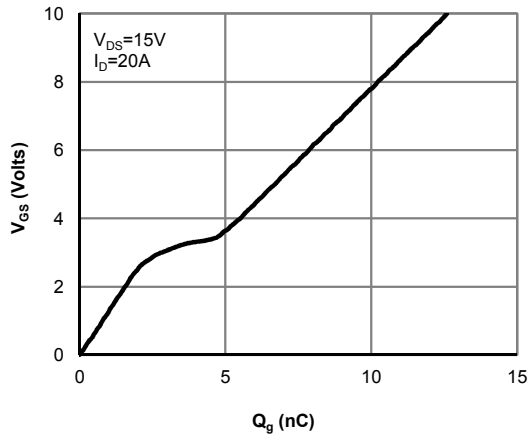


Figure 7: Gate-Charge Characteristics

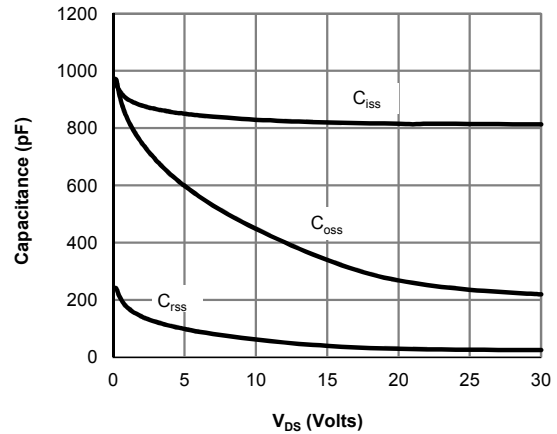


Figure 8: Capacitance Characteristics

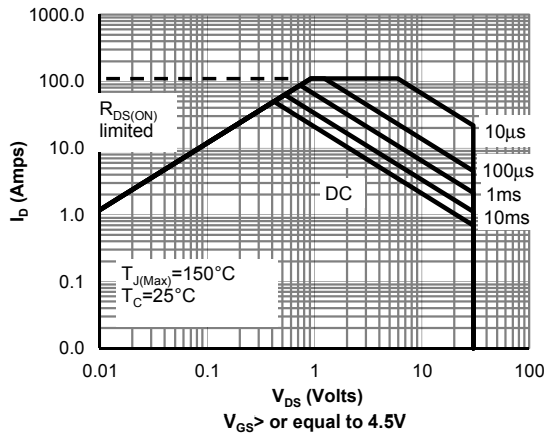


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

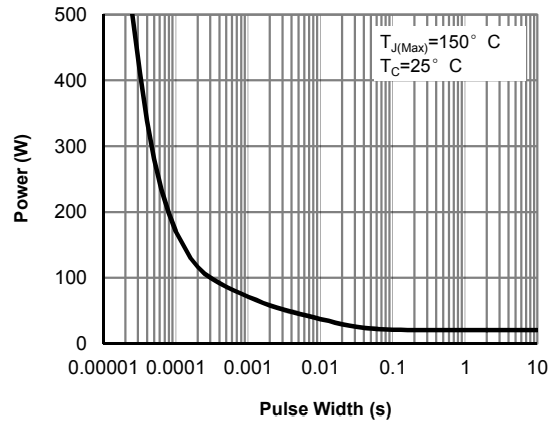


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

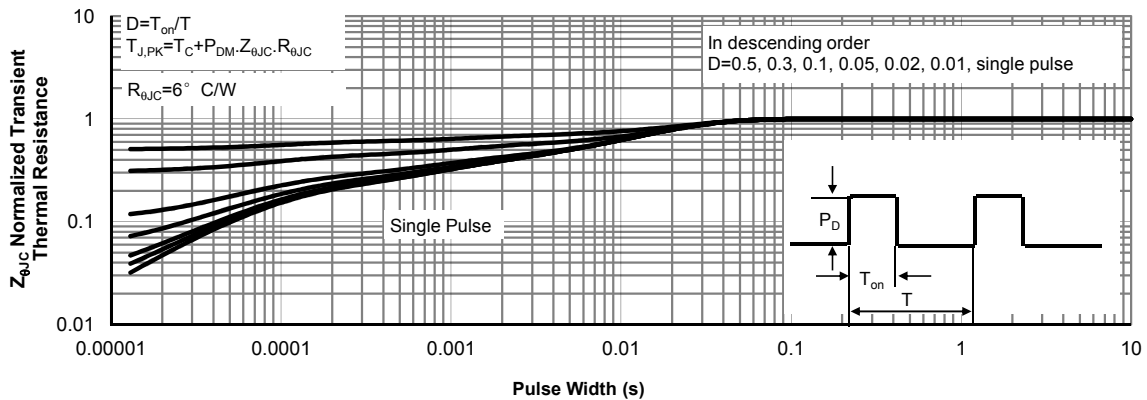
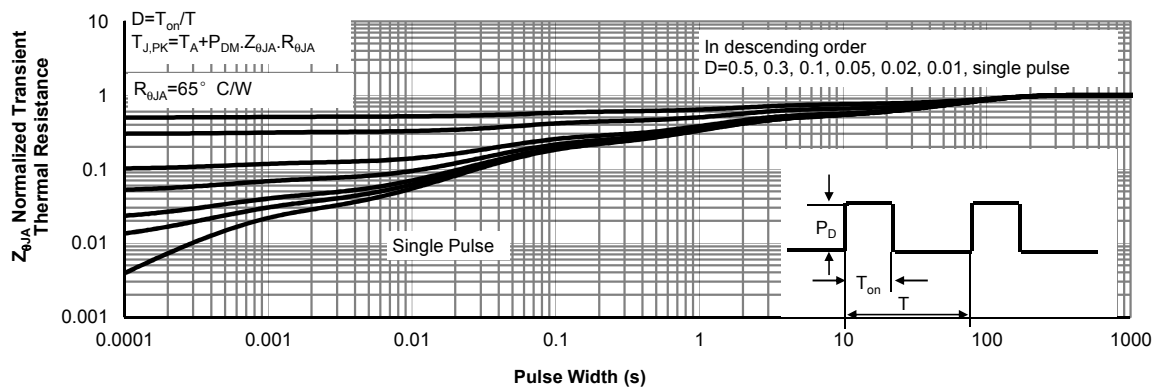
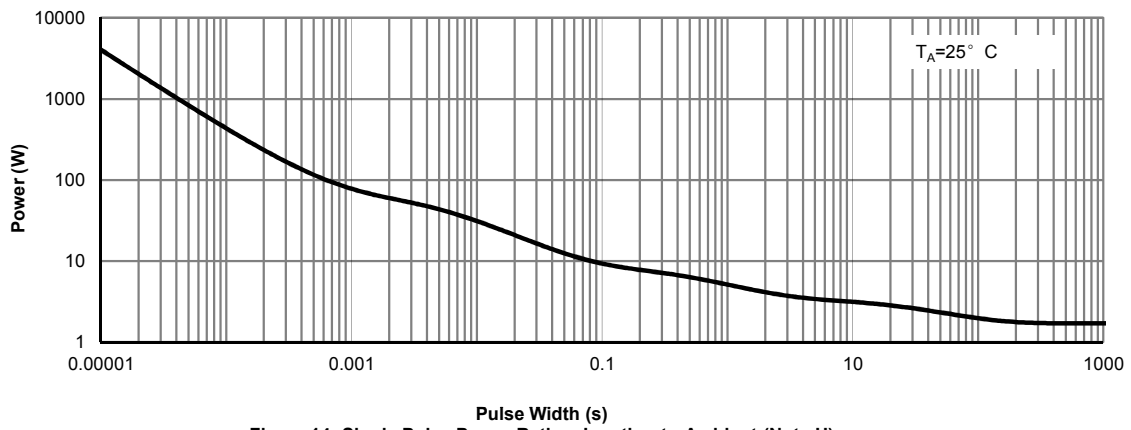
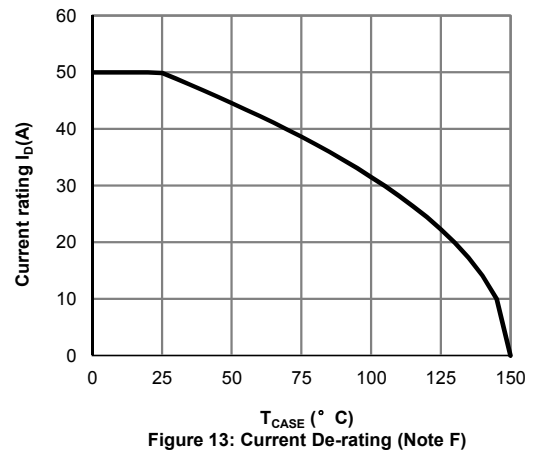
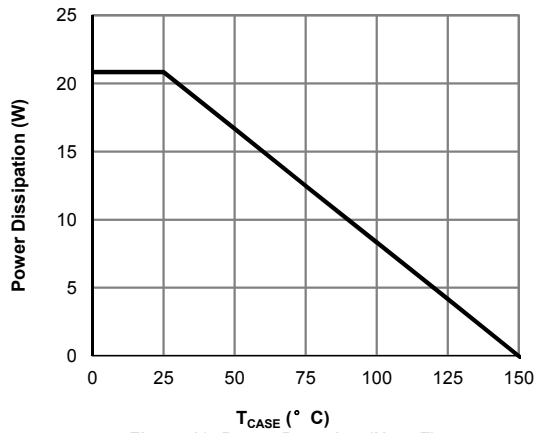


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	ID=10mA, VGS=0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			0.5 100	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.5	1.9	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		1.6 2.4	2 3	mΩ
		V _{GS} =4.5V, I _D =20A		2	2.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		100		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.45	0.7	V
I _S	Maximum Body-Diode Continuous Current				50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		3110		pF
C _{oss}	Output Capacitance			930		pF
C _{rss}	Reverse Transfer Capacitance			100		pF
R _g	Gate resistance	f=1MHz	0.9	1.9	2.9	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		49		nC
Q _g (4.5V)	Total Gate Charge			21		nC
Q _{gs}	Gate Source Charge			8		nC
Q _{gd}	Gate Drain Charge			5.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			44		ns
t _f	Turn-Off Fall Time			7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		17.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		43		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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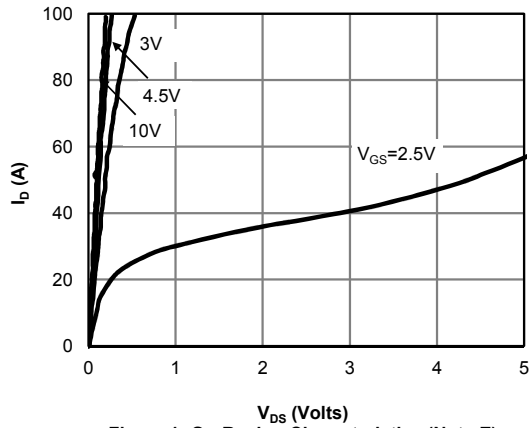


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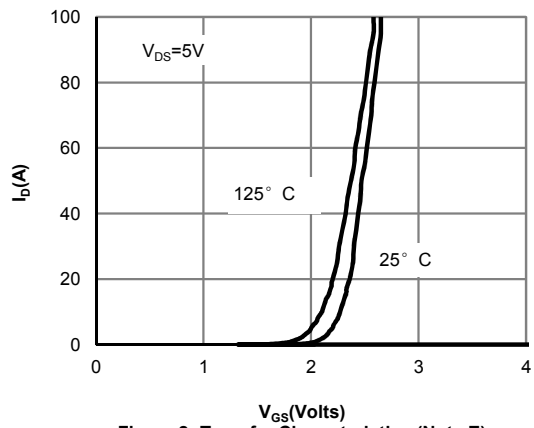


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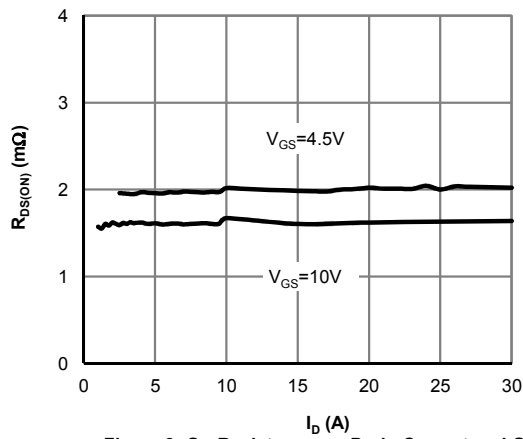


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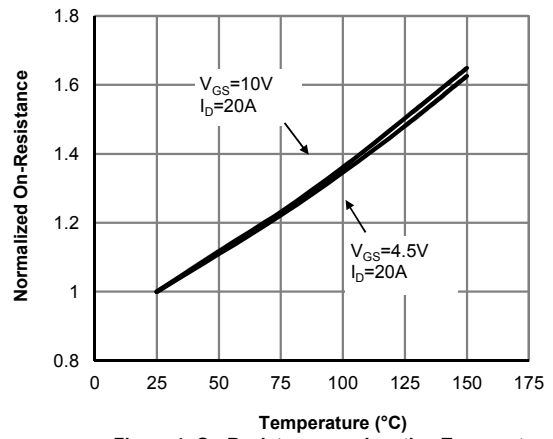


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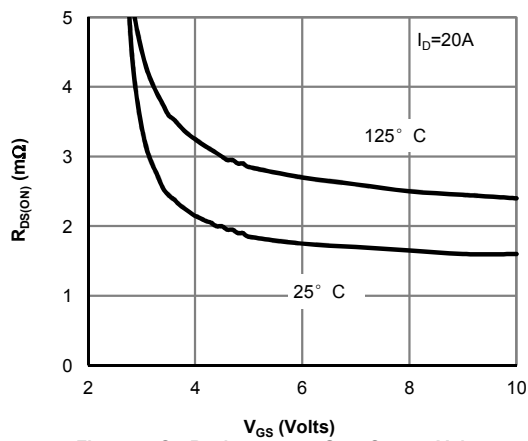


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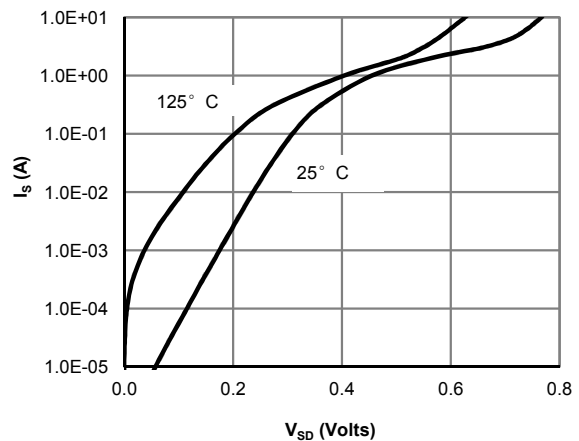


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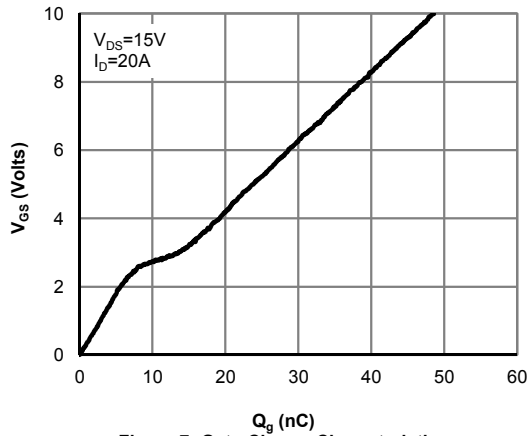


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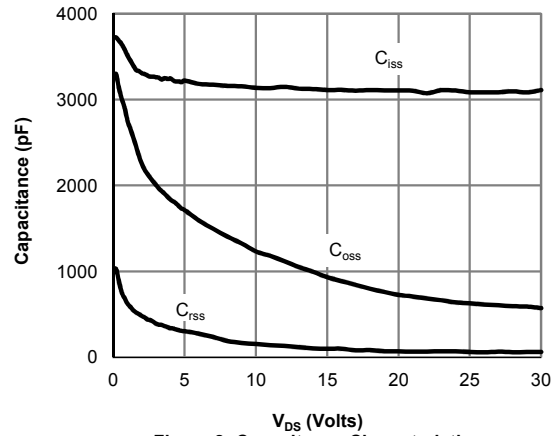


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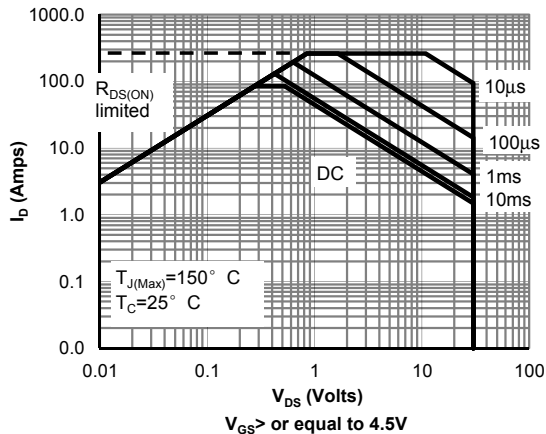


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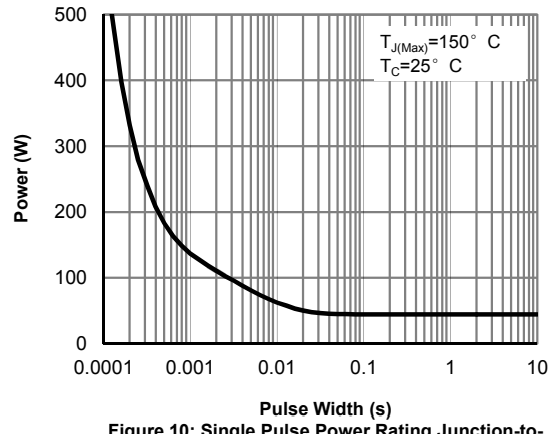


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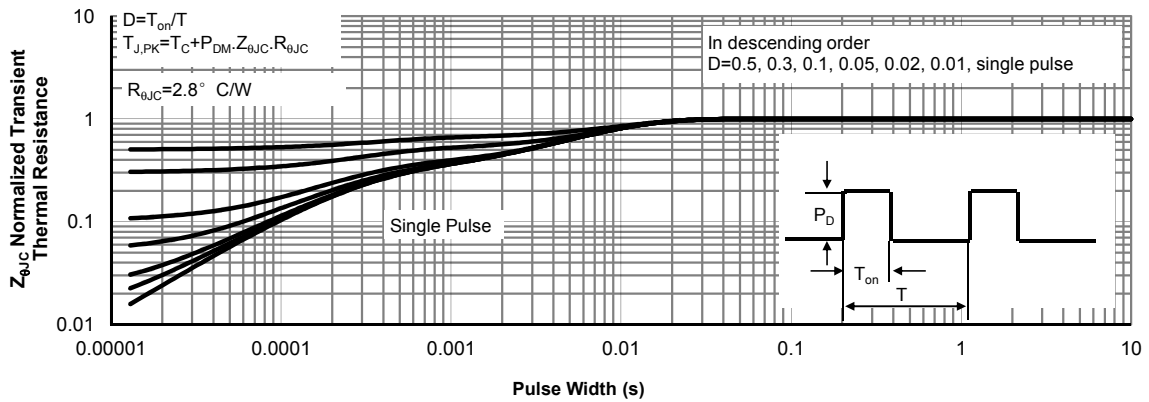
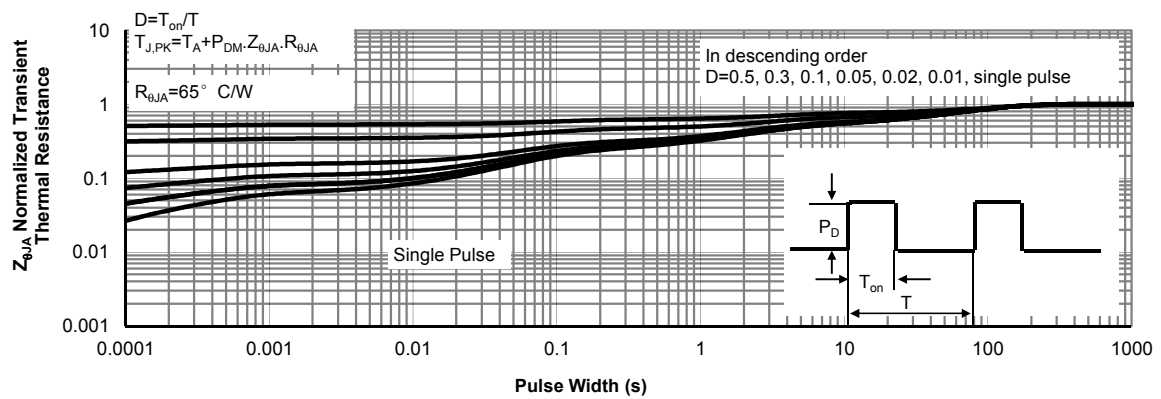
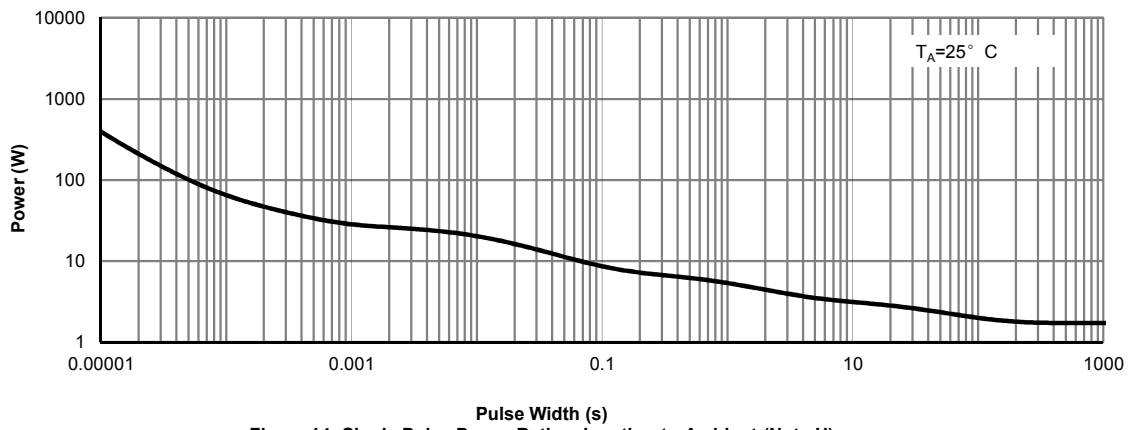
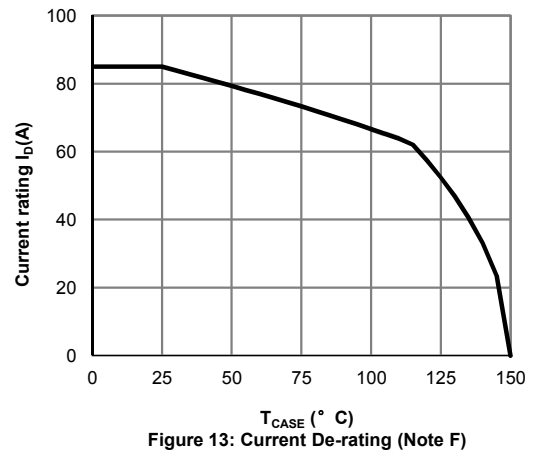
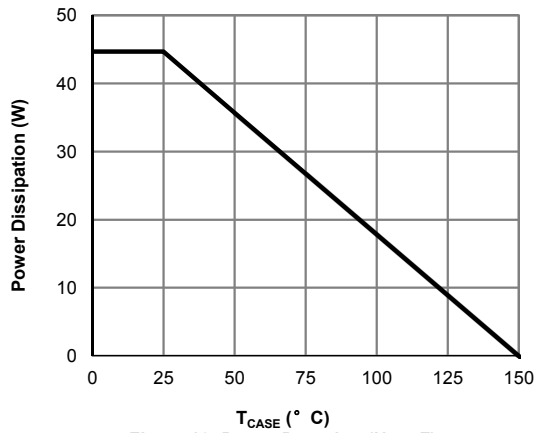
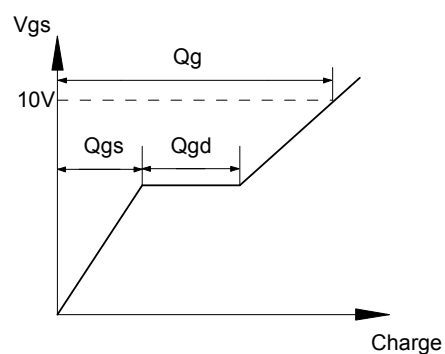
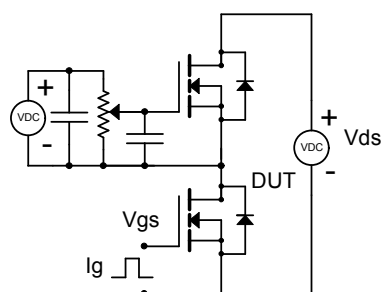


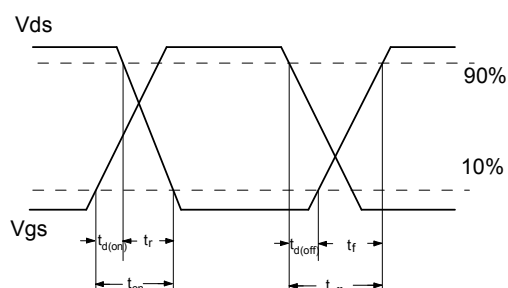
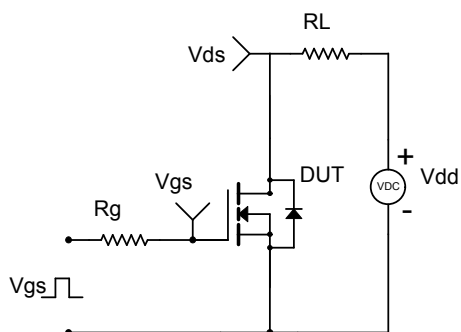
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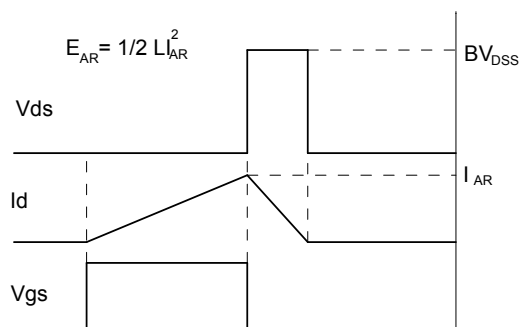
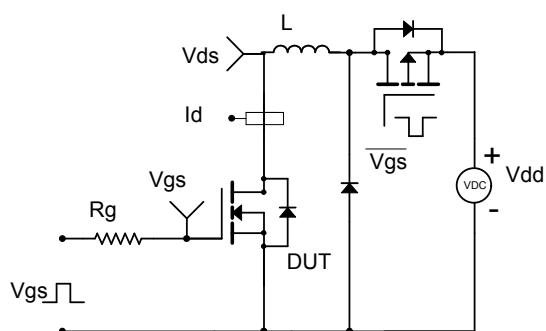




Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

