MCP1754/MCP1754S

150 mA, 16V, High-Performance LDO

Features:

- High PSRR: >70 dB @ 1 kHz, Typical
- 56.0 µA Typical Quiescent Current
- Input Operating Voltage Range: 3.6V to16.0V
- 150 mA Output Current for All Output Voltages
- Low-Dropout Voltage, 300 mV Typical @ 150 mA
- 0.4% Typical Output Voltage Tolerance
- Standard Output Voltage Options (1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 4.0V, 5.0V)
- Output Voltage Range 1.8V to 5.5V in 0.1V Increments (tighter increments also possible per design)
- Output Voltage Tolerances of ±2.0% Over Entire Temperature Range
- Stable with Minimum 1.0 µF Output Capacitance
- Power Good Output
- Shutdown Input
- True Current Foldback Protection
- Short-Circuit Protection
- Overtemperature Protection

Applications:

- Battery-Powered Devices
- Battery-Powered Alarm Circuits
- Smoke Detectors
- CO_2 Detectors
- Pagers and Cellular Phones
- Smart Battery Packs
- PDAs
- Digital Cameras
- Microcontroller Power
- Consumer Products
- Battery-Powered Data Loggers

Related Literature:

- AN765, *"Using Microchip's Micropower LDOs"* (DS00765), Microchip Technology Inc., 2007
- AN766, *"Pin-Compatible CMOS Upgrades to BiPolar LDOs"* (DS00766), Microchip Technology Inc., 2003
- AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), Microchip Technology Inc., 2001

Description:

The MCP1754/MCP1754S is a family of CMOS low dropout (LDO) voltage regulators that can deliver up to 150 mA of current while consuming only 56.0 µA of quiescent current (typical). The input operating range is specified from 3.6V to 16.0V, making it an ideal choice for four to six primary cell battery-powered applications, 12V mobile applications and one to three-cell Li-Ion-powered applications.

The MCP1754/MCP1754S is capable of delivering 150 mA with only 300 mV (typical) of input to output voltage differential. The output voltage tolerance of the MCP1754/MCP1754S is typically ±0.2% at +25°C and ±2.0% maximum over the operating junction temperature range of -40°C to +125°C. Line regulation is ±0.01% typical at +25°C.

Output voltages available for the MCP1754/MCP1754S range from 1.8V to 5.5V. The LDO output is stable when using only 1 µF of output capacitance. Ceramic, tantalum or aluminum electrolytic capacitors may all be used for input and output. Overcurrent limit and overtemperature shutdown provide a robust solution for any application.

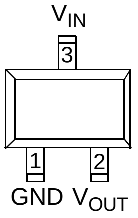
The MCP1754/MCP1754S family introduces a true current foldback feature. When the load impedance decreases beyond the MCP1754/MCP1754S load rating, the output current and voltage will gracefully foldback towards 30 mA at about 0V output. When the load impedance decreases and returns to the rated load, the MCP1754/MCP1754S follows the same foldback curve as the device comes out of current foldback.

Package options for the MCP1754S include the SOT-23A, SOT-89-3, SOT-223-3 and 2x3 DFN-8.

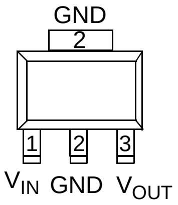
Package options for the MCP1754 include the SOT-23-5, SOT-223-5, and 2x3 DFN-8.

Package Types – MCP1754S

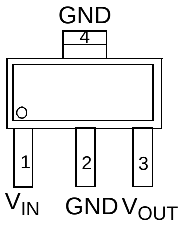
3-Pin SOT-23A



3-Pin SOT-89

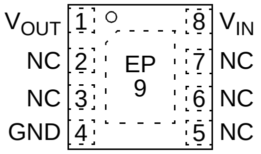


SOT-223-3



(**Note:** The 3-lead SOT-223 (DB) is not a standard package for output voltages below 3.0V)

8-Lead 2X3 DFN(*)

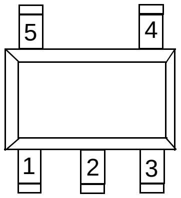


Tab is connected to GND

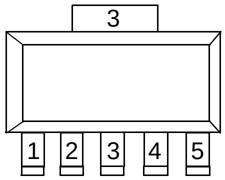
* Includes Exposed Thermal Pad (EP); see Table 3-2.

Package Types – MCP1754

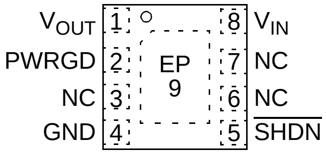
SOT23-5



SOT-223-5



8-Lead 2X3 DFN(*)



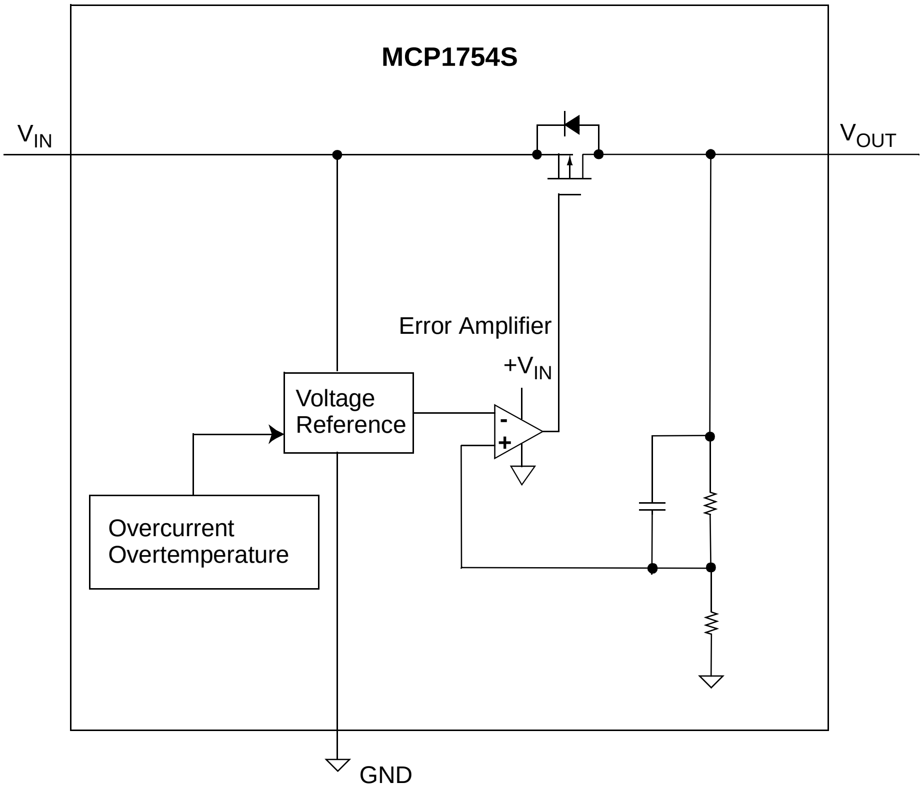
Tab is connected to GND

PIN	FUNCTION
1	V_{IN}
2	GND
3	$\overline{\text{SHDN}}$
4	PWRGD
5	V_{OUT}

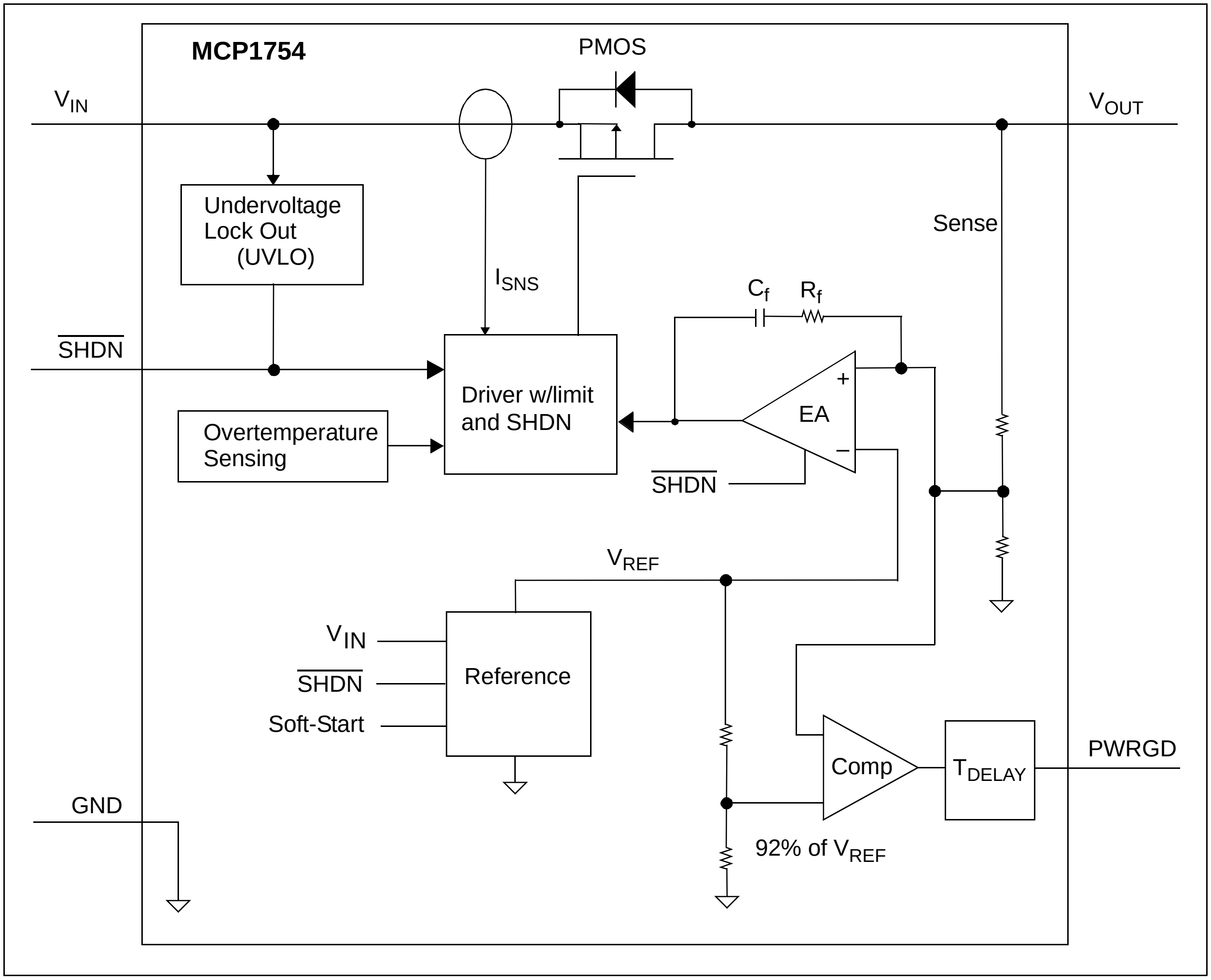
PIN	FUNCTION
1	$\overline{\text{SHDN}}$
2	V_{IN}
3	GND
4	V_{OUT}
5	PWRGD

* Includes Exposed Thermal Pad (EP); see Table 3-1.

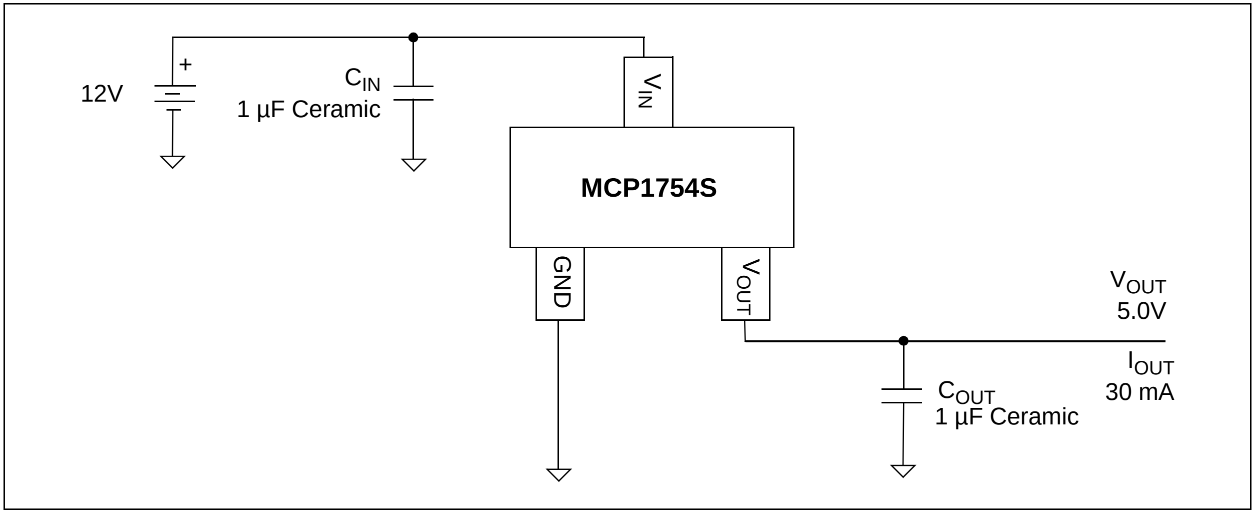
Functional Block Diagram – MCP1754S



Functional Block Diagram – MCP1754



Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN}	+17.6V
VIN, PWRGD, $\overline{SHDN}$	(GND-0.3V) to (V_{IN}+0.3V)
VOUT	(GND-0.3V) to (+5.5V)
Internal Power Dissipation	Internally-Limited (**Note 6**)
Output Short Circuit Current	Continuous
Storage temperature	-55°C to +150°C
Maximum Junction Temperature	165°C (**Note 7**)
Operating Junction Temperature	-40°C to +150°C
ESD protection on all pins	≥ 4 kV HBM and ≥ 200V MM

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, **Note 1**, I_{LOAD} = 1 mA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C, $t_{r(VIN)}$ = 0.5V/µs, $\overline{SHDN} = V_{IN}$, PWRGD = 10K to V_{OUT}.
Boldface type applies for junction temperatures, T_J **(Note 7)** of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input/Output Characteristics						
Input Operating Voltage	V_{IN}	**3.6**	—	**16.0**	V	
Output Voltage Operating Range	$V_{OUT\text{-}RANGE}$	**1.8**	—	**5.5**	V	
Input Quiescent Current	I_q	—	56	**90**	µA	I_L = 0 mA
Input Quiescent Current for $\overline{SHDN}$ mode	$I_{\overline{SHDN}}$	—	0.1	**5**	µA	$\overline{SHDN}$ = GND
Ground Current	I_{GND}	—	150	**250**	µA	I_{LOAD} = 150 mA
Maximum Output Current	I_{OUT}	**150**	—	—	mA	
Output Soft Current Limit	I_{OUT_SCL}	—	250	—	mA	$V_{IN} = V_{IN(MIN)}$, $V_{OUT} \geq 0.1V$, Current measured 10 ms after load is applied
Output Pulse Current Limit	I_{OUT_PCL}	—	250	—	mA	Pulse Duration < 100 ms, Duty Cycle < 50%, $V_{OUT} \geq 0.1V$, **Note 6**
Output Short Circuit Foldback Current	I_{OUT_SC}	—	30	—	mA	$V_{IN} = V_{IN(MIN)}$, V_{OUT} = GND
Output Voltage Overshoot on Startup	V_{OVER}	—	0.5	—	$\%V_{OUT}$	V_{IN} = 0 to 16V, I_{LOAD} = 150 mA
Output Voltage Regulation	V_{OUT}	**V_R-2.0%**	V_R±0.2%	**V_R+2.0%**	V	**Note 2**
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	22		ppm/°C	**Note 3**

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 3.6V$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage when the input voltage $V_{IN} = V_{Rated} + V_{DROPOUT(MAX)}$ or V_{IN} = 3.6V (whichever is greater); I_{OUT} = 1 mA.

3: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW}) * 10^6/(V_R * \Delta Temperature)$, $V_{OUT\text{-}HIGH}$ = highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R + 1V$ or V_{IN} = 3.6V (whichever is greater).

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, Note 1, I_{LOAD} = 1 mA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C, $t_{r(VIN)}$ = 0.5V/µs, $\overline{SHDN} = V_{IN}$, PWRGD = 10K to V_{OUT}.
Boldface type applies for junction temperatures, T_J **(Note 7)** of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Line Regulation	ΔV_{OUT}/ (V_{OUT} x ΔV_{IN})	**-0.05**	±0.01	**+0.05**	%/V	$V_R + 1V \leq V_{IN} \leq 16V$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-1.1**	-0.4	**0**	%	I_L = 1.0 mA to 150 mA, Note 4
Dropout Voltage (Note 5)	$V_{DROPOUT}$	—	300	**500**	mV	I_L = 150 mA
Dropout Current	I_{DO}	—	50	**85**	µA	$V_{IN} = 0.95V_R$, I_{OUT} = 0 mA
Undervoltage Lockout						
Undervoltage Lockout	UVLO	—	2.95	—	V	Rising V_{IN}
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	—	285	—	mV	Falling V_{IN}
Shutdown Input						
Logic High Input	$V_{SHDN-HIGH}$	**2.4**	—	$V_{IN(MAX)}$	V	
Logic Low Input	$V_{SHDN-LOW}$	0.0	—	**0.8**	V	
Shutdown Input Leakage Current	$\overline{SHDN}_{ILK}$	—	0.100	**0.500**	µA	$\overline{SHDN}$ = GND
		—	0.500	**2.0**		$\overline{SHDN}$ = 16V
Power Good Output						
PWRGD Input Voltage Operating Range	V_{PWRGD_VIN}	**1.7**	—	V_{IN}	V	I_{SINK} = 1 mA
PWRGD Threshold Voltage (Referenced to V_{OUT})	V_{PWRGD_TH}	**90**	92	**94**	$\%V_{OUT}$	Falling Edge of V_{OUT}
PWRGD Threshold Hysteresis	V_{PWRGD_HYS}	—	2.0	—	$\%V_{OUT}$	Rising Edge of V_{OUT}
PWRGD Output Voltage Low	V_{PWRGD_L}	—	0.2	**0.6**	V	I_{PWRGD_SINK} = 5.0 mA, V_{OUT} = 0V
PWRGD Output Sink Current	I_{PWRGD_L}	**5.0**	—	—	mA	$V_{PWRGD} \leq 0.4V$
PWRGD Leakage Current	I_{PWRGD_LK}	—	40	**700**	nA	V_{PWRGD} Pullup = 10 kΩ to V_{IN}, V_{IN} = 16V
PWRGD Time Delay	T_{PG}	—	100	—	µs	Rising Edge of V_{OUT}, R_{PULLUP} = 10 kΩ
Detect Threshold to PWRGD Active Time Delay	T_{VDET_PWRGD}	—	200	—	µs	Falling Edge of V_{OUT} after Transition from $V_{OUT} = V_{PRWRGD\_TH}$ + 50 mV, to V_{PWRGD_TH} - 50 mV, R_{PULLUP} = 10kΩ to V_{IN}

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 3.6V$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage when the input voltage $V_{IN} = V_{Rated} + V_{DROPOUT(MAX)}$ or V_{IN} = 3.6V (whichever is greater); I_{OUT} = 1 mA.

3: $TCV_{OUT} = (V_{OUT-HIGH} – V_{OUT-LOW}) *10^6/(V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R$ + 1V or V_{IN} = 3.6V (whichever is greater).

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, **Note 1**, I_{LOAD} = 1 mA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C, $t_{r(VIN)}$ = 0.5V/µs, $\overline{SHDN} = V_{IN}$, PWRGD = 10K to V_{OUT}.
Boldface type applies for junction temperatures, T_J (**Note 7**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
AC Performance						
Output Delay From V_{IN} To V_{OUT} = 90% V_{REG}	T_{DELAY}	—	240	—	µs	V_{IN} = 0V to 16V, V_{OUT} = 90% V_R, $t_{r\ (VIN)}$= 5V/µs, C_{OUT} = 1 µF, $\overline{SHDN} = V_{IN}$
Output Delay From V_{IN} To V_{OUT} > 0.1V	T_{DELAY_START}	—	80	—	µs	V_{IN} = 0V to 16V, $V_{OUT} \geq 0.1V$, $t_{r\ (VIN)}$= 5V/µs, C_{OUT} = 1 µF, $\overline{SHDN} = V_{IN}$
Output Delay From $\overline{SHDN}$ to V_{OUT} = 90% V_{REG}	T_{DELAY_SHDN}	—	160	—	µs	V_{IN} = 16V, V_{OUT} = 90% V_R, C_{OUT} = 1 µF, $\overline{SHDN}$ = GND to V_{IN}
Output Noise	e_N	—	3	—	$µV/(Hz)^{1/2}$	I_L = 50 mA, f = 1 kHz, C_{OUT} = 1 µF
Power Supply Ripple Rejection Ratio	PSRR	—	72	—	dB	V_R = 5V, f = 1 kHz, I_L = 150 mA, V_{INAC} = 1V pk-pk, C_{IN} = 0 µF, $V_{IN} = V_R + 1.5V$
Thermal Shutdown Temperature	T_{SD}	—	150	—	°C	**Note 6**
Thermal Shutdown Hysteresis	ΔTSD	—	10	—	°C	

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 3.6V$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage when the input voltage $V_{IN} = V_{Rated} + V_{DROPOUT(MAX)}$ or V_{IN} = 3.6V (whichever is greater); I_{OUT} = 1 mA.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) *10^6/(V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R + 1V$ or V_{IN} = 3.6V (whichever is greater).

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40		+125	°C	
Operating Temperature Range	T_J	-40		+150	°C	
Storage Temperature Range	T_A	-55		+150	°C	
Thermal Package Resistance						
Thermal Resistance, SOT-223-3	θ_{JA} θ_{JC}	— —	62 15	— —	°C/W	
Thermal Resistance, SOT-23A-3	θ_{JA} θ_{JC}	— —	336 110	— —	°C/W	
Thermal Resistance, SOT-89-3	θ_{JA} θ_{JC}	— —	153.3 100	— —	°C/W	
Thermal Resistance, SOT-223-5	θ_{JA} θ_{JC}	— —	62 15	— —	°C/W	
Thermal Resistance, 2X3 DFN	θ_{JA} θ_{JC}	— —	93 26	— —	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

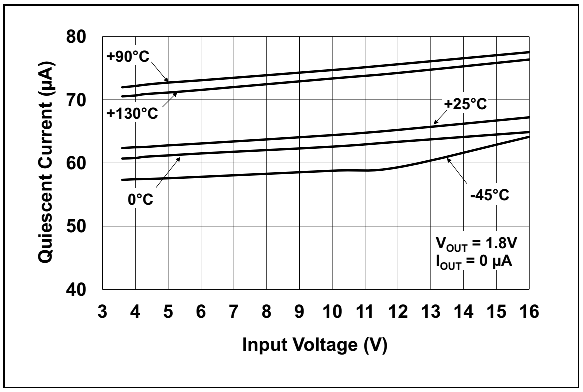


FIGURE 2-1: Quiescent Current vs. Input Voltage.

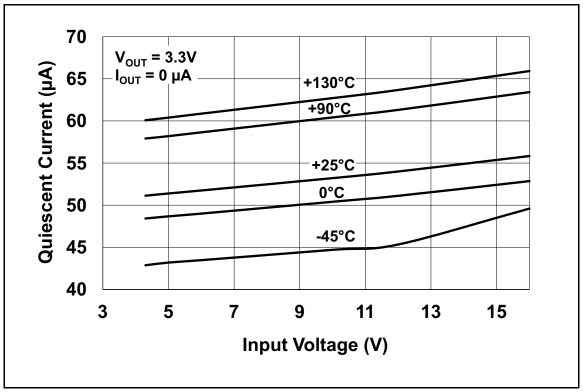


FIGURE 2-2: Quiescent Current vs. Input Voltage.

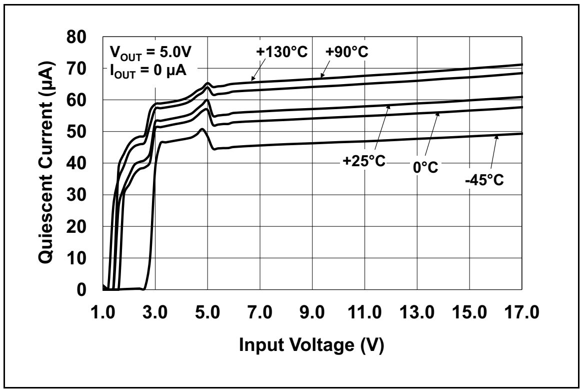


FIGURE 2-3: Quiescent Current vs. Input Voltage.

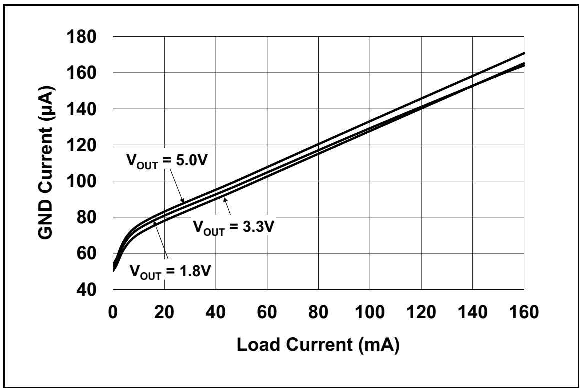


FIGURE 2-4: Ground Current vs. Load Current.

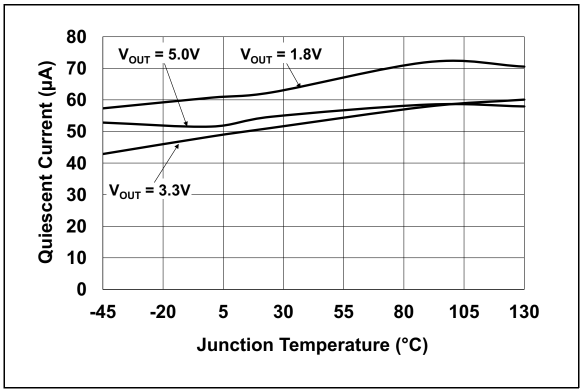


FIGURE 2-5: Quiescent Current vs. Junction Temperature.

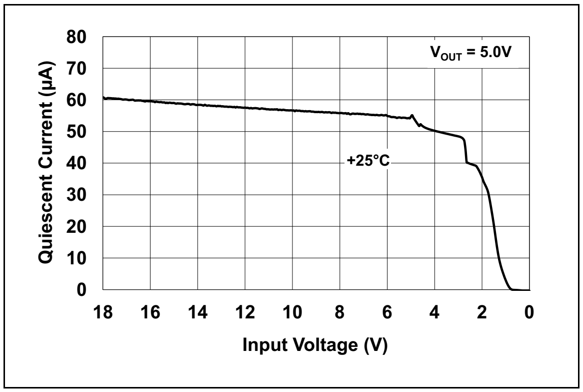


FIGURE 2-6: Quiescent Current vs. Input Voltage.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

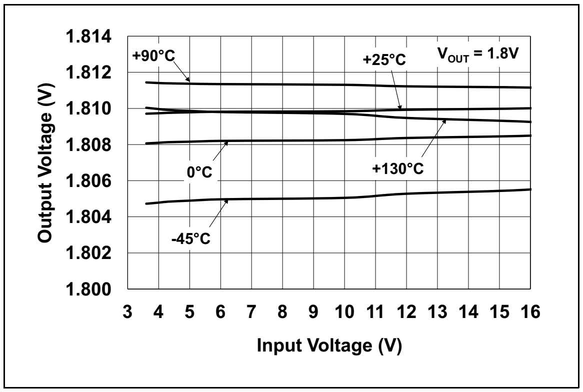


FIGURE 2-7: Output Voltage vs. Input Voltage.

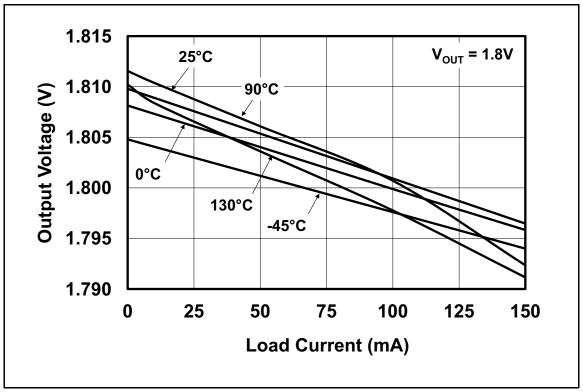


FIGURE 2-10: Output Voltage vs. Load Current.

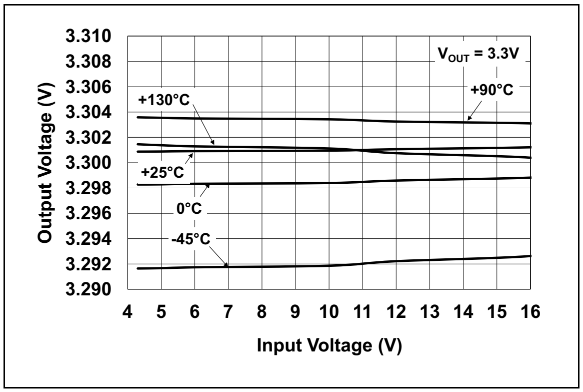


FIGURE 2-8: Output Voltage vs. Input Voltage.

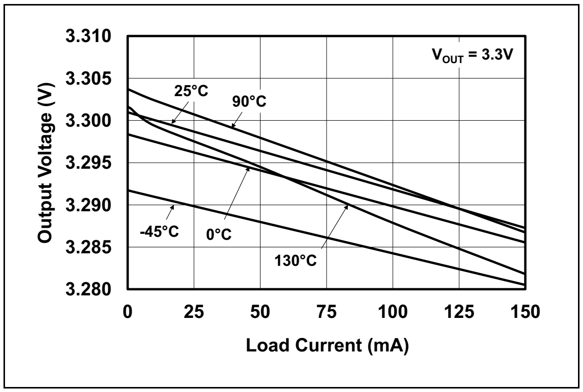


FIGURE 2-11: Output Voltage vs. Load Current.

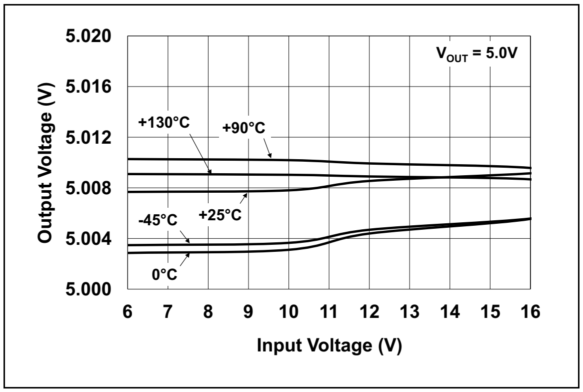


FIGURE 2-9: Output Voltage vs. Input Voltage.

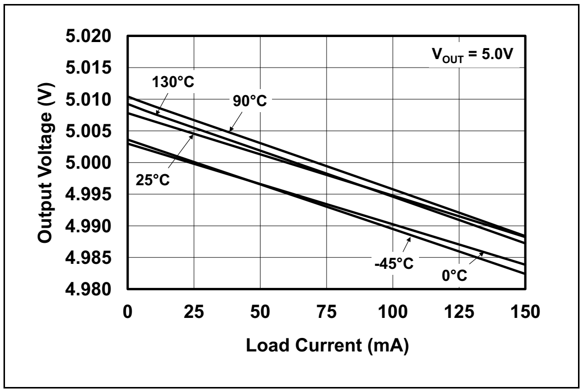


FIGURE 2-12: Output Voltage vs. Load Current.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25 °C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

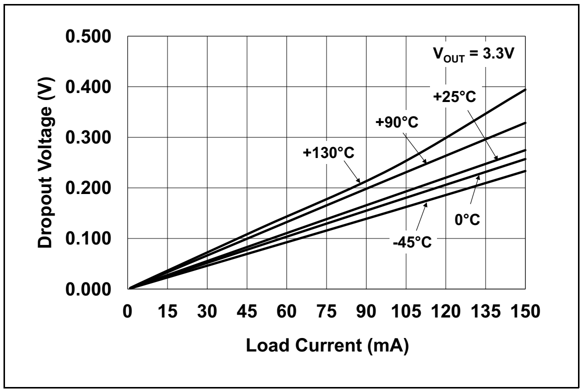


FIGURE 2-13: *Dropout Voltage vs. Load Current.*

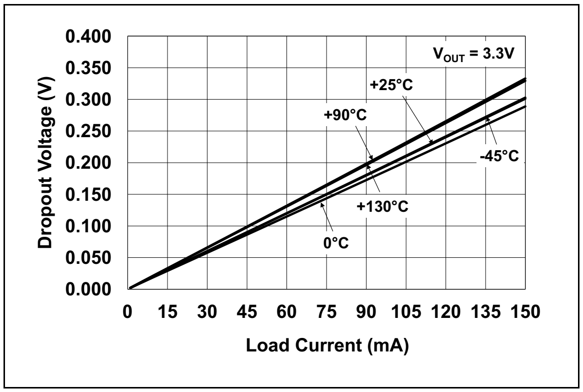


FIGURE 2-14: *Dropout Voltage vs. Load Current.*

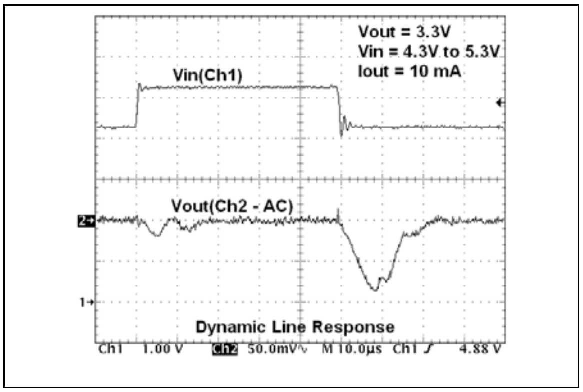


FIGURE 2-15: *Dynamic Line Response.*

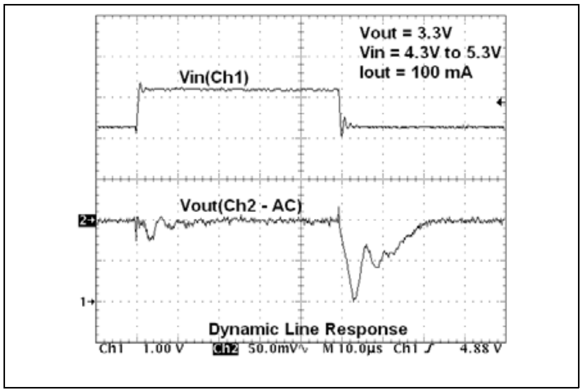


FIGURE 2-16: *Dynamic Line Response.*

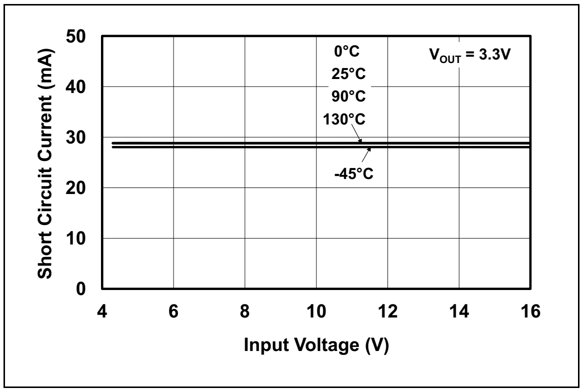


FIGURE 2-17: *Short Circuit Current vs. Input Voltage.*

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25 °C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{\text{SHDN}}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

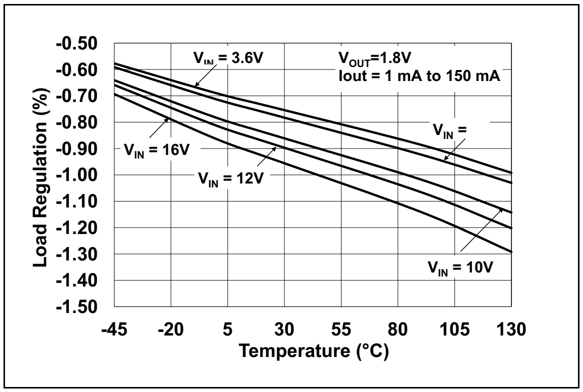


FIGURE 2-18: Load Regulation vs. Temperature.

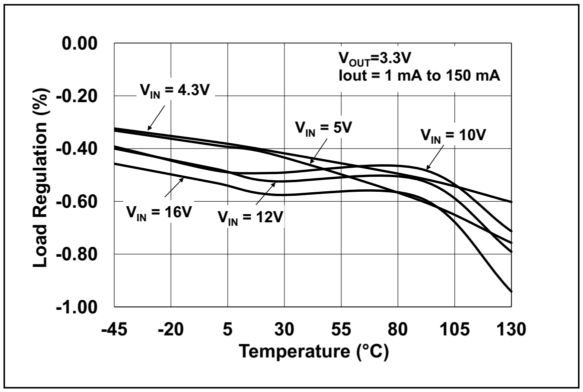


FIGURE 2-19: Load Regulation vs. Temperature.

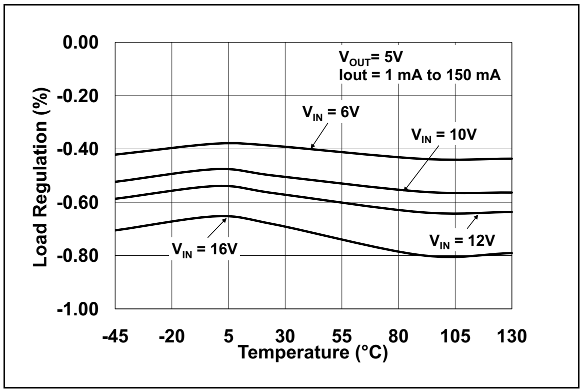


FIGURE 2-20: Load Regulation vs. Temperature.

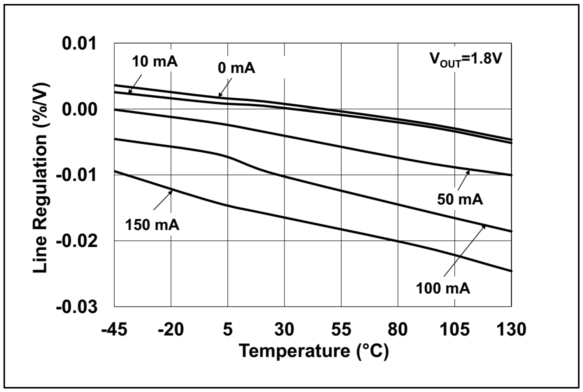


FIGURE 2-21: Line Regulation vs. Temperature.

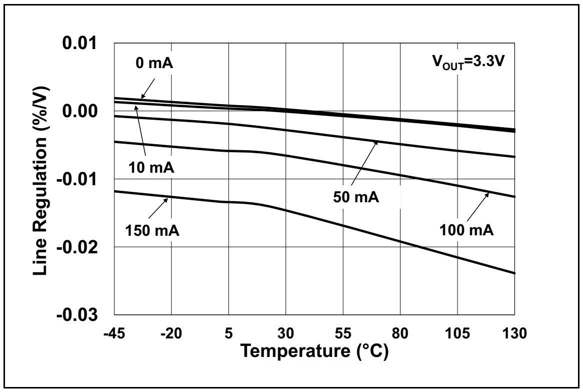


FIGURE 2-22: Line Regulation vs. Temperature.

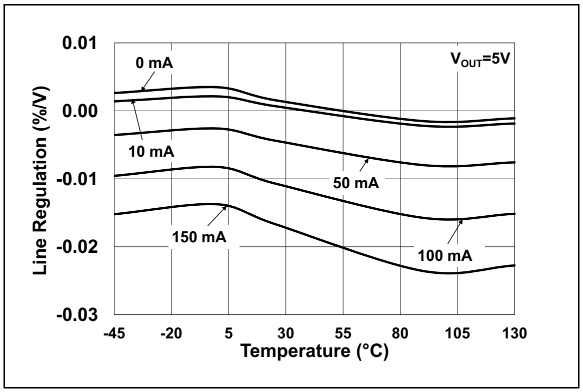


FIGURE 2-23: Line Regulation vs. Temperature.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25 °C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

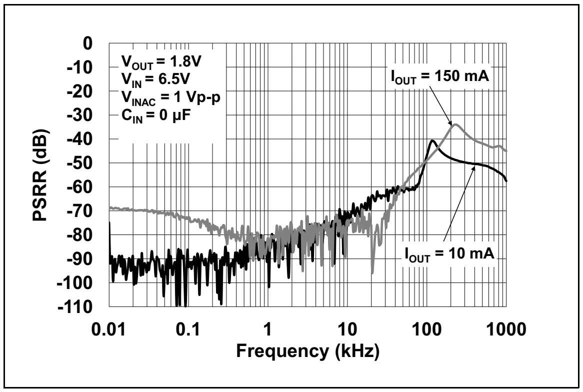


FIGURE 2-24: Power Supply Ripple Rejection vs. Frequency.

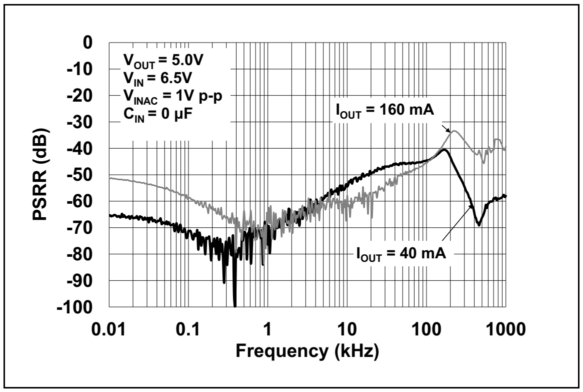


FIGURE 2-25: Power Supply Ripple Rejection vs. Frequency.

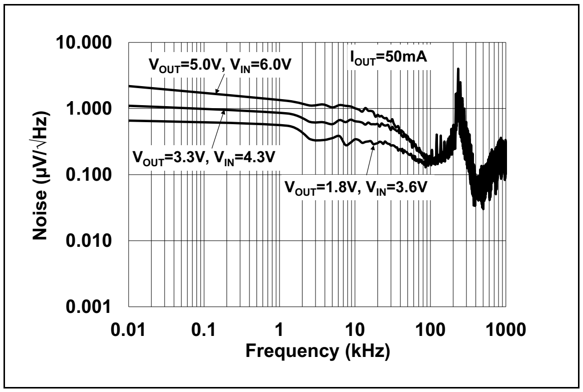


FIGURE 2-26: Output Noise vs. Frequency (3 lines, V_R = 1.2V, 3.3V, 5.0V).

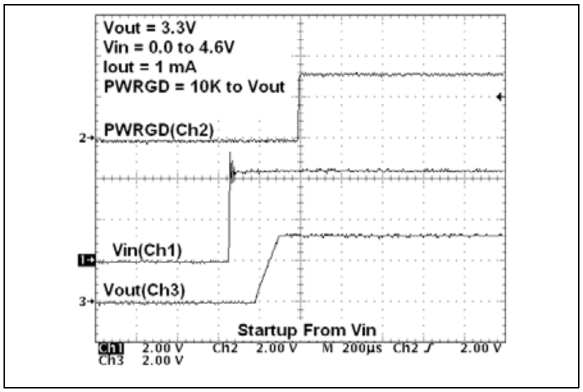


FIGURE 2-27: Power Up Timing.

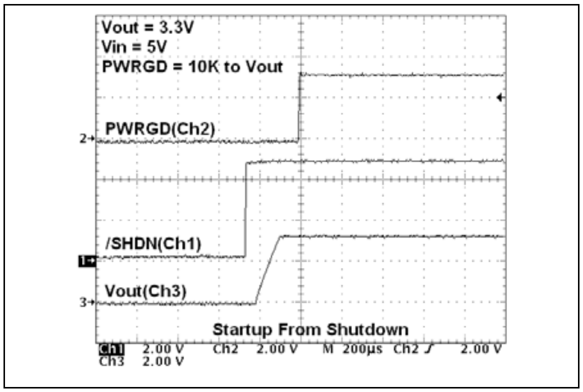


FIGURE 2-28: Startup From Shutdown.

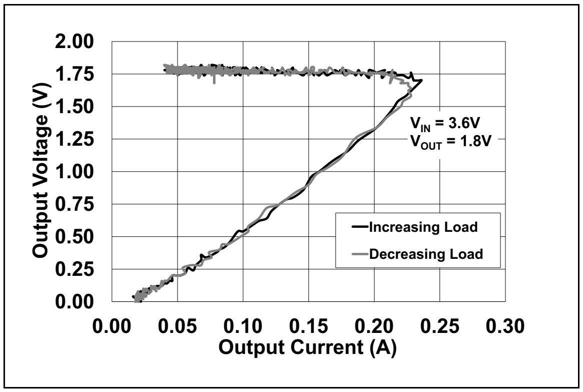


FIGURE 2-29: Short Circuit Current Foldback.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25 °C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

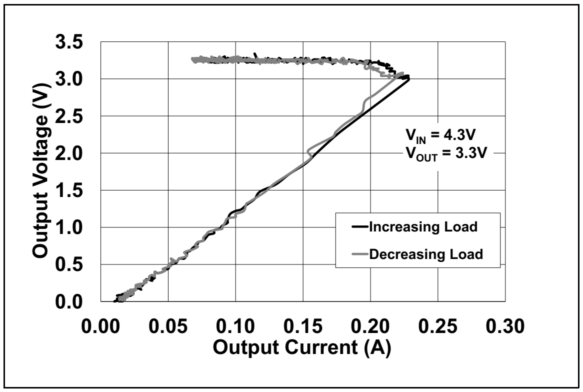


FIGURE 2-30: *Short Circuit Current Foldback.*

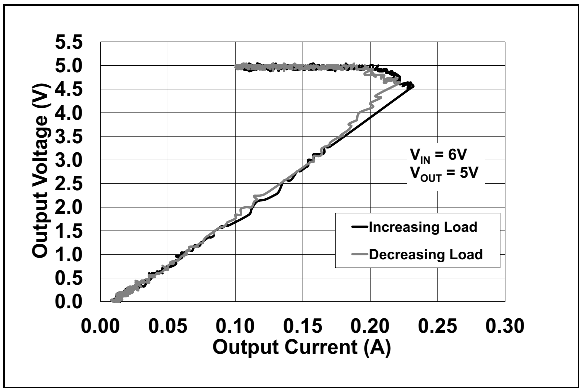


FIGURE 2-31: *Short Circuit Current Foldback.*

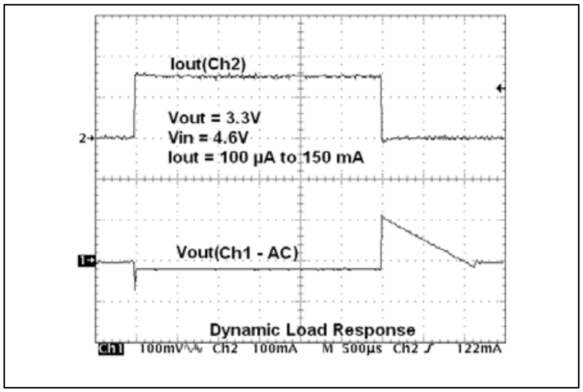


FIGURE 2-32: *Dynamic Load Response.*

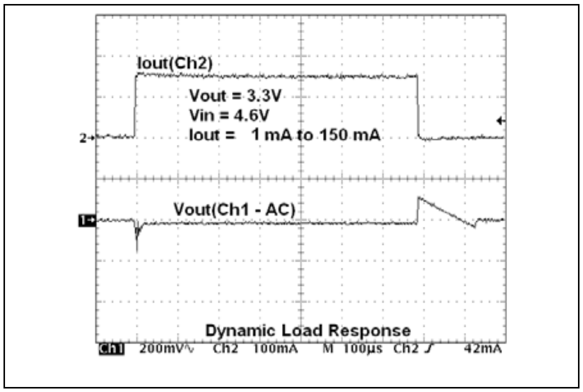


FIGURE 2-33: *Dynamic Load Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

TABLE 3-1: MCP1754 PIN FUNCTION TABLE

Pin No. SOT223-5	Pin No. SOT23-5	Pin No. 2X3 DFN	Name	Function
4	5	1	V_{OUT}	Regulated Voltage Output
5	4	2	PWRGD	Open-Drain Power Good Output
—	—	3,6,7	NC	No Connection
3	2	4	GND	Ground Terminal
1	3	5	$\overline{\text{SHDN}}$	Shutdown Input
2	1	8	V_{IN}	Unregulated Supply Voltage
EP	—	EP	GND	Exposed Pad, Connected to GND

TABLE 3-2: MCP1754S PIN FUNCTION TABLE

Pin No. SOT223-3	Pin No. SOT23A	Pin No. SOT89	Pin No. 2X3 DFN	Name	Function
3	2	3	1	V_{OUT}	Regulated Voltage Output
—	—	—	2,3,5,6,7	NC	No Connection
2	1	2	4	GND	Ground Terminal
1	3	1	8	V_{IN}	Unregulated Supply Voltage
EP	—	EP	EP	GND	Exposed Pad, Connected to GND

3.1 Regulated Output Voltage (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO V_{OUT} pin as is practical. The current flowing out of this pin is equal to the DC load current.

3.2 Power Good Output (PWRGD)

The PWRGD output is an open-drain output used to indicate when the LDO output voltage is within 92% (typically) of its nominal regulation value. The PWRGD threshold has a typical hysteresis value of 2%. The PWRGD output is delayed by 100 µs (typical) from the time the LDO output is within 92% + 2% (typical hysteresis) of the regulated output value on power-up. This delay time is internally fixed. The PWRGD pin may be pulled up to V_{IN} or V_{OUT}. Pulling up to V_{OUT} conserves power when the device is in shutdown ($\overline{\text{SHDN}}$ = 0V) mode.

3.3 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize the voltage drops between this pin and the negative side of the load.

3.4 Shutdown Input ($\overline{\text{SHDN}}$)

The $\overline{\text{SHDN}}$ input is used to turn the LDO output voltage on and off. When the $\overline{\text{SHDN}}$ input is at a logic high level, the LDO output voltage is enabled. When the $\overline{\text{SHDN}}$ input is pulled to a logic low level, the LDO output voltage is disabled. When the $\overline{\text{SHDN}}$ input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state.

3.5 Unregulated Input Voltage (V_{IN})

Connect V_{IN} to the input unregulated source voltage. Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low-source impedance depends on the proximity of the input source capacitors or battery type. For most applications, 1 µF of capacitance ensures stable operation of the LDO circuit. The input capacitor should have a capacitance value equal to or larger than the output capacitor for performance applications. The input capacitor supplies the load current during transients and improves performance. For applications that have load currents below 10 mA, the input capacitance requirement can be lowered. The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic yields better noise and PSRR performance at high frequency.

3.6 Exposed Pad (EP)

Some of the packages have an exposed metal pad on the bottom of the package. The exposed metal pad gives the device better thermal characteristics by providing a good thermal path to either the PCB or heat sink to remove heat from the device. The exposed pad of the package is internally connected to GND.

4.0 DEVICE OVERVIEW

The MCP1754/MCP1754S is a 150 mA output current, Low Dropout (LDO) voltage regulator. The low dropout voltage of 300 mV typical at 150 mA of current makes it ideal for battery-powered applications. The input voltage range is 3.6V to 16.0V. Unlike other high output current LDOs, the MCP1754/MCP1754S typically draws only 150 µA of quiescent current for a 150 mA load. The MCP1754 adds a shutdown control input pin and a power good output pin. The output voltage options are fixed.

4.1 LDO Output Voltage

The MCP1754/MCP1754S LDO has a fixed output voltage. The output voltage range is 1.8V to 5.5V.

4.2 Output Current and Current Limiting

The MCP1754/MCP1754S LDO is tested and ensured to supply a minimum of 150 mA of output current. The MCP1754/MCP1754S has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage to within tolerance.

The MCP1754/MCP1754S also incorporates a true output current foldback. If the output load presents an excessive load due to a low-impedance short circuit condition, the output current and voltage will fold back towards 30 mA and 0V, respectively.

The output voltage and current resume normal levels when the excessive load is removed. If the overload condition is a soft overload, the MCP1754/MCP1754S supplies higher load currents of up to typically 250 mA. This allows for device usage in applications that have pulsed load currents having an average output current value of 150 mA or less.

Output overload conditions may also result in an overtemperature shutdown of the device. If the junction temperature rises above +150°C (typical), the LDO shuts down the output. See **Section 4.8 “Overtemperature Protection”** for more information on overtemperature shutdown.

4.3 Output Capacitor

The MCP1754/MCP1754S requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmentally robust qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The Equivalent Series Resistance (ESR) of the electrolytic output capacitor should be no greater than 2.0Ω. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 milliohms.

Larger LDO output capacitors are used with the MCP1754/MCP1754S to improve dynamic performance and power supply ripple rejection performance. A maximum of 1000 µF is recommended. Aluminum-electrolytic capacitors are not recommended for low temperature applications of <-25°C.

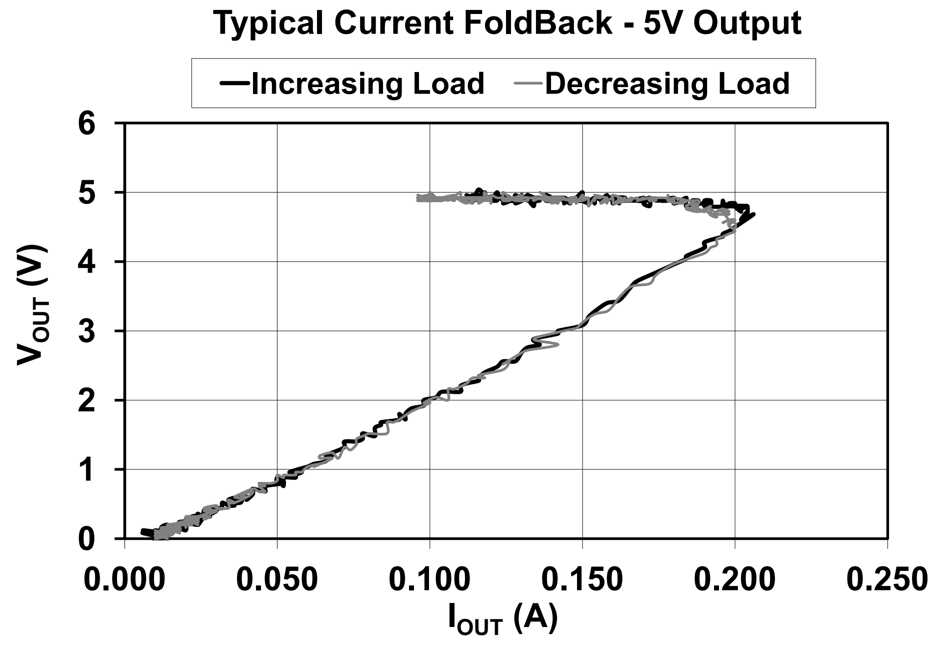


FIGURE 4-1: *Typical Current Foldback.*

4.4 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries or in applications with long lead length (>10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent or higher value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.5 Power Good Output (PWRGD)

The open-drain PWRGD output is used to indicate when the output voltage of the LDO is within 94% (typical value, see **Section 1.0 "Electrical Characteristics"** for minimum and maximum specifications) of its nominal regulation value.

As the output voltage of the LDO rises, the open-drain PWRGD output is actively held low until the output voltage has exceeded the power good threshold plus the hysteresis value. Once this threshold has been exceeded, the power good time delay is started (shown as T_{PG} in the Electrical Characteristics table). The power good time delay is fixed at 100 µs (typical). After the time delay period, the PWRGD open-drain output becomes inactive and may be pulled high by an external pull-up resistor, indicating that the output voltage is stable and within regulation limits. The power good output is typically pulled up to V_{IN} or V_{OUT}. Pulling the signal up to V_{OUT} conserves power during Shutdown mode.

If the output voltage of the LDO falls below the power good threshold, the power good output will transition low. The power good circuitry has a 200 µs delay when detecting a falling output voltage, which helps to increase noise immunity and avoid false triggering of the power good output during fast output transients. See Figure 4-2 for power good timing characteristics.

When the LDO is put into Shutdown mode using the $\overline{\text{SHDN}}$ input, the power good output is pulled low immediately, indicating that the output voltage is out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-3.

The power good output is an open-drain output that can be pulled up to any voltage equal to or less than the LDO input voltage. This output is capable of sinking 5 mA ($V_{PWRGD} < 0.4V$).

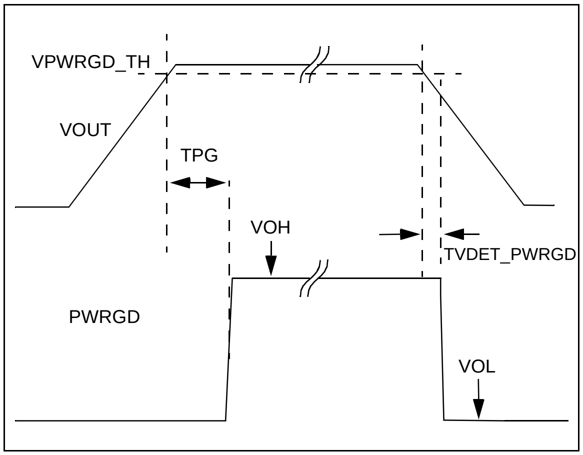


FIGURE 4-2: *Power Good Timing.*

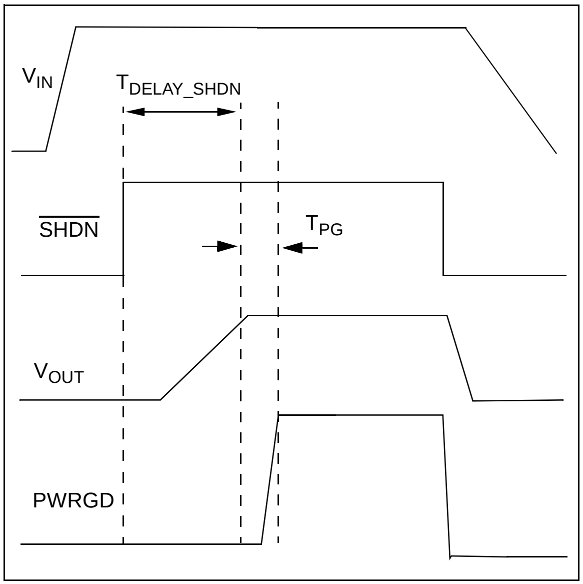


FIGURE 4-3: *Power Good Timing from Shutdown.*

4.6 Shutdown Input ($\overline{\text{SHDN}}$)

The $\overline{\text{SHDN}}$ input is an active-low input signal that turns the LDO on and off. The $\overline{\text{SHDN}}$ threshold is a fixed voltage level. The minimum value of this shutdown threshold required to turn the output ON is 2.4V. The maximum value required to turn the output OFF is 0.8V.

The $\overline{\text{SHDN}}$ input ignores low going pulses (pulses meant to shut down the LDO) that are up to 400 ns in pulse width. If the shutdown input is pulled low for more than 400 ns, the LDO enters Shutdown mode. This small bit of filtering helps to reject any system noise spikes on the shutdown input signal.

On the rising edge of the $\overline{\text{SHDN}}$ input, the shutdown circuitry has a 70 µs delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{\text{SHDN}}$ input signal. After the 70 µs delay, the LDO output enters its soft-start period as it rises from 0V to its final regulation value. If the $\overline{\text{SHDN}}$ input signal is pulled low during the 70 µs delay period, the timer resets and the delay time starts over again on the next rising edge of the $\overline{\text{SHDN}}$ input. The total time from the $\overline{\text{SHDN}}$ input going high (turn-on) to the LDO output being in regulation is typically 160 µs. See Figure 4-4 for a timing diagram of the $\overline{\text{SHDN}}$ input.

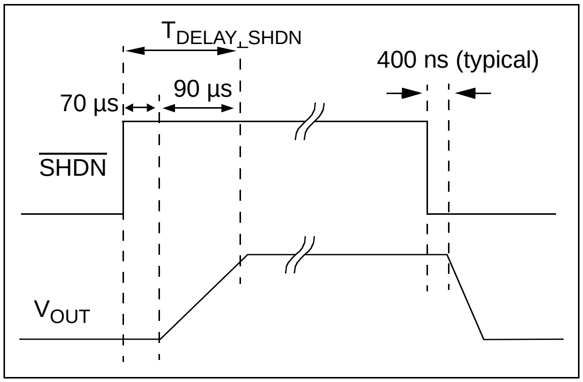


FIGURE 4-4: Shutdown Input Timing Diagram.

4.7 Dropout Voltage and Undervoltage Lockout

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a V_R + 1.0V differential applied. The MCP1754/MCP1754S LDO has a very low dropout voltage specification of 300 mV (typical) at 150 mA of output current. See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

The MCP1754/MCP1754S LDO operates across an input voltage range of 3.6V to 16.0V and incorporates input Undervoltage Lockout (UVLO) circuitry that keeps the LDO output voltage off until the input voltage reaches a minimum of 2.95V (typical) on the rising edge of the input voltage. As the input voltage falls, the LDO output remains on until the input voltage level reaches 2.70V (typical).

For high-current applications, voltage drops across the PCB traces must be taken into account. The trace resistances can cause significant voltage drops between the input voltage source and the LDO. For applications with input voltages near 3.0V, these PCB trace voltage drops can sometimes lower the input voltage enough to trigger a shutdown due to undervoltage lockout.

4.8 Overtemperature Protection

The MCP1754/MCP1754S LDO has temperature-sensing circuitry to prevent the junction temperature from exceeding approximately +150°C. If the LDO junction temperature does reach +150°C, the LDO output is turned off until the junction temperature cools to approximately +137°C, at which point the LDO output automatically resumes normal operation. If the internal power dissipation continues to be excessive, the device will again shut off. The junction temperature of the die is a function of power dissipation, ambient temperature and package thermal resistance. See **Section 5.0 "Application Circuits and Issues"** for more information on LDO power dissipation and junction temperature.

NOTES:

5.0 APPLICATION CIRCUITS AND ISSUES

5.1 Typical Application

The MCP1754/MCP1754S is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage make it ideal for many battery-powered applications.

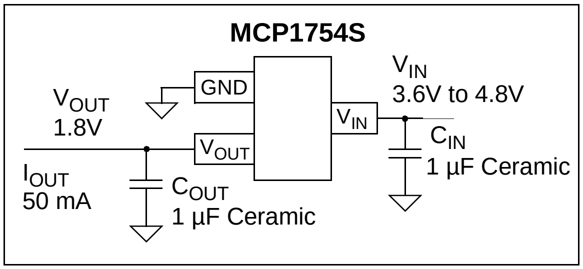


FIGURE 5-1: *Typical Application Circuit.*

5.1.1 APPLICATION INPUT CONDITIONS

Package Type = SOT23
Input Voltage Range = 3.6V to 4.8V
V_{IN} maximum = 4.8V
V_{OUT} typical = 1.8V
I_{OUT} = 50 mA maximum

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1754/MCP1754S is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low that it is insignificant (56.0 µA x V_{IN}). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

P_{LDO} = LDO Pass device internal power dissipation
$V_{IN(MAX)}$ = Maximum input voltage
$V_{OUT(MIN)}$ = LDO minimum output voltage

The maximum continuous operating junction temperature specified for the MCP1754/MCP1754S is +150°C. To estimate the internal junction temperature of the MCP1754/MCP1754S, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT23A pin package is estimated at 336 °C/W.

EQUATION

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{A(MAX)}$$

$T_{J(MAX)}$ = Maximum continuous junction temperature
P_{TOTAL} = Total device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction to ambient
$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability of a package is calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
$T_{J(MAX)}$ = Maximum continuous junction temperature
$T_{A(MAX)}$ = Maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
$P_{D(MAX}$ = Maximum device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction Temperature
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
T_A = Ambient temperature

5.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = SOT-23

Input Voltage

V_{IN} = 3.6V to 4.8V

LDO Output Voltages and Currents

V_{OUT} = 1.8V

I_{OUT} = 50 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation

Internal Power dissipation is the product of the LDO output current multiplied by the voltage across the LDO (V_{IN} to V_{OUT}).

$$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

$$P_{LDO} = (4.8V - (0.97 \times 1.8V)) \times 50\text{ mA}$$

$$P_{LDO} = 152.7\text{ milliwatts}$$

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC® standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, *“High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages”*. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, *“A Method to Determine How Much Power a SOT23 Can Dissipate in an Application”* (DS00792), for more information regarding this subject.

$$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$$

$$T_{J(RISE)} = 152.7\text{ milliwatts} \times 336.0^\circ\text{C/Watt}$$

$$T_{J(RISE)} = 51.3^\circ\text{C}$$

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated as follows:

$$T_J = T_{J(RISE)} + T_{A(MAX)}$$

$$T_J = 91.3^\circ\text{C}$$

Maximum Package Power Dissipation Examples at +40°C Ambient Temperature

SOT-23 (336.0°C/Watt = $R\theta_{JA}$)

$$P_{D(MAX)} = (125^\circ\text{C} - 40^\circ\text{C})/336^\circ\text{C/W}$$

$$P_{D(MAX)} = 253\text{ milliwatts}$$

SOT-89 (153.3°C/Watt = $R\theta_{JA}$)

$$P_{D(MAX)} = (125^\circ\text{C} - 40^\circ\text{C})/153.3^\circ\text{C/W}$$

$$P_{D(MAX)} = 554\text{ milliwatts}$$

5.4 Voltage Reference

The MCP1754/MCP1754S can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1754/MCP1754S LDO. The low-cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1754/MCP1754S as a voltage reference.

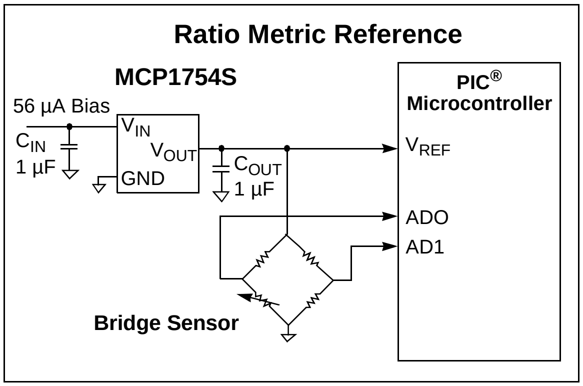


FIGURE 5-2: *Using the MCP1754/MCP1754S as a Voltage Reference.*

5.5 Pulsed Load Applications

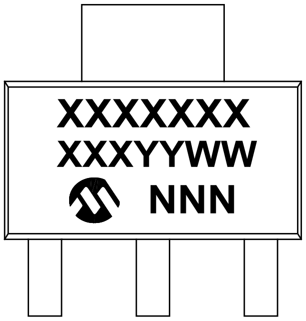
For some applications, there are pulsed load current events that may exceed the specified 150 mA maximum specification of the MCP1754/MCP1754S. The internal current limit of the MCP1754/MCP1754S prevents high peak load demands from causing non-recoverable damage. The 150 mA rating is a maximum average continuous rating. As long as the average current does not exceed 150 mA, pulsed higher load currents can be applied to the MCP1754/MCP1754S. The typical current limit for the MCP1754/MCP1754S is 250 mA (T_A +25°C).

NOTES:

6.0 PACKAGING INFORMATION

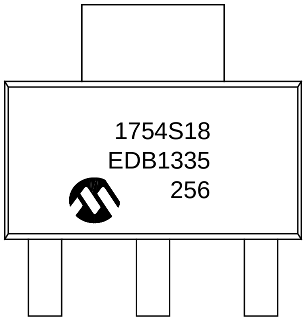
6.1 Package Marking Information

3-Lead SOT-223 **(MCP1754S only)**

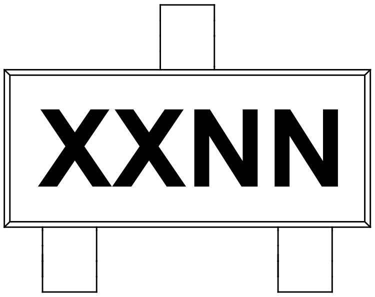


Part Number	Code
MCP1754S-1802E/DB	1754S18
MCP1754ST-1802E/DB	1754S18
MCP1754S-3302E/DB	1754S33
MCP1754ST-3302E/DB	1754S33
MCP1754S-5002E/DB	1754S50
MCP1754ST-5002E/DB	1754S50

Example:

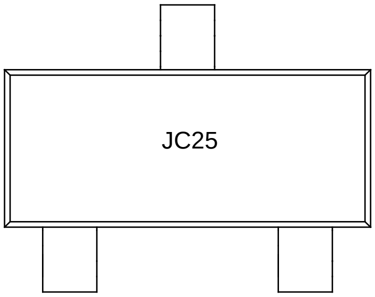


3-Lead SOT-23A **(MCP1754S only)**

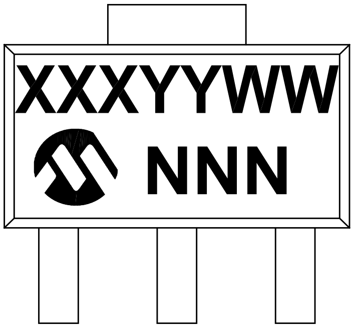


Part Number	Code
MCP1754ST-1802E/CB	JCNN
MCP1754ST-3302E/CB	JDNN
MCP1754ST-5002E/CB	JENN

Example:

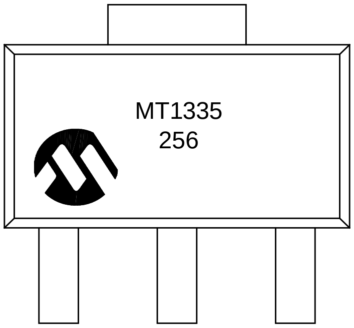


3-Lead SOT-89 **(MCP1754S only)**



Part Number	Code
MCP1754ST-1802E/MB	MTYYWW
MCP1754ST-3302E/MB	MUYYWW
MCP1754ST-5002E/MB	MVYYWW

Example:

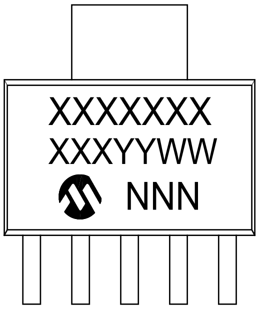


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

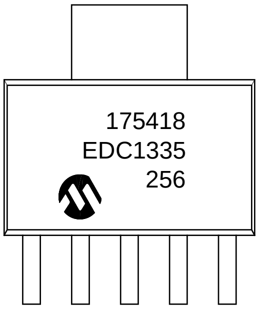
Package Marking Information (Continued)

5-Lead SOT-223 **(MCP1754 only)**

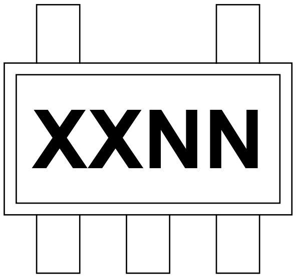


Part Number	Code
MCP1754T-1802E/DC	175418
MCP1754T-3302E/DC	175433
MCP1754T-5002E/DC	175450

Example:

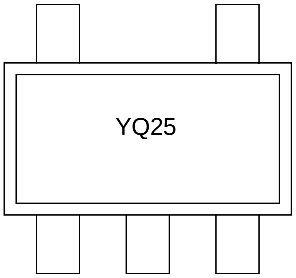


5-Lead SOT-23A (2x3) **(MCP1754 only)**

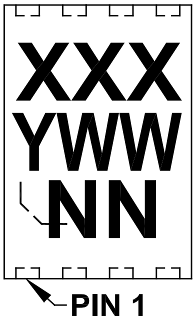


Part Number	Code
MCP1754T-1802E/OT	YQNN
MCP1754T-3302E/OT	YRNN
MCP1754T-5002E/OT	YSNN

Example:

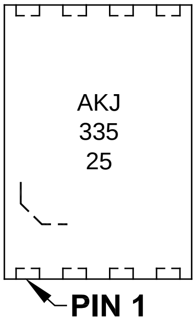


8-Lead DFN (2x3)



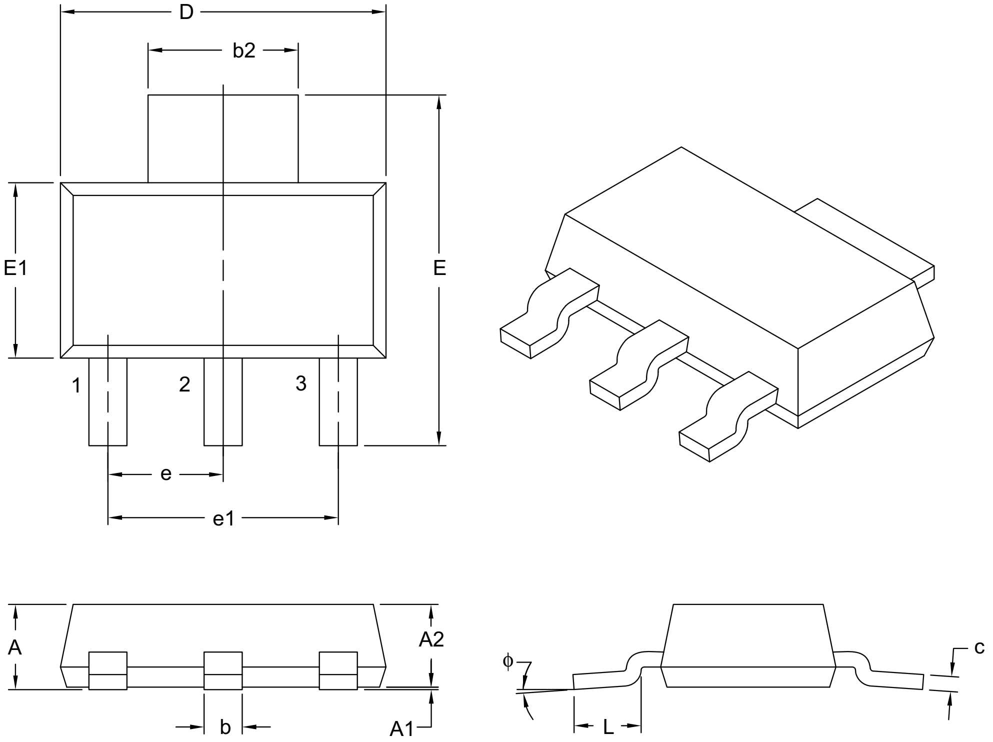
Part Number	Code	Part Number	Code
MCP1754-1802E/MC	AKG	MCP1754S-1802E/MC	ALN
MCP1754-3302E/MC	AKH	MCP1754S-3302E/MC	ALM
MCP1754-5002E/MC	AKJ	MCP1754S-5002E/MC	ALL
MCP1754T-1802E/MC	AKG	MCP1754ST-1802E/MC	ALN
MCP1754T-3302E/MC	AKH	MCP1754ST-3302E/MC	ALM
MCP1754T-5002E/MC	AKJ	MCP1754ST-5002E/MC	ALL

Example:



3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N	3		
Lead Pitch	e	2.30 BSC		
Outside Lead Pitch	e1	4.60 BSC		
Overall Height	A	–	–	1.80
Standoff	A1	0.02	–	0.10
Molded Package Height	A2	1.50	1.60	1.70
Overall Width	E	6.70	7.00	7.30
Molded Package Width	E1	3.30	3.50	3.70
Overall Length	D	6.30	6.50	6.70
Lead Thickness	c	0.23	0.30	0.35
Lead Width	b	0.60	0.76	0.84
Tab Lead Width	b2	2.90	3.00	3.10
Foot Length	L	0.75	–	–
Lead Angle	ϕ	0°	–	10°

Notes:

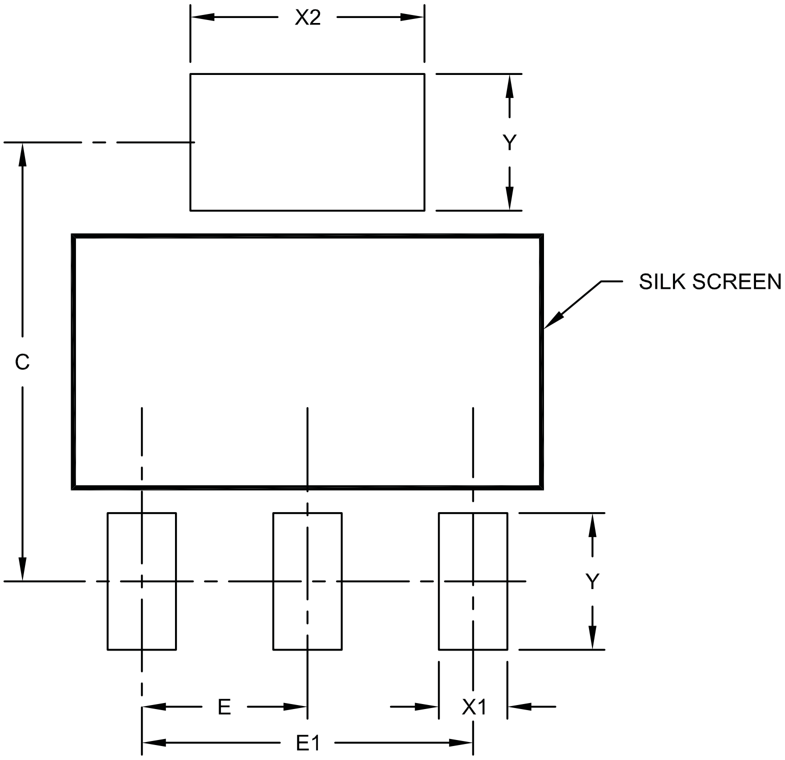
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.30 BSC		
Overall Pitch	E1	4.60 BSC		
Contact Pad Spacing	C		6.10	
Contact Pad Width	X1			0.95
Contact Pad Width	X2			3.25
Contact Pad Length	Y			1.90

Notes:

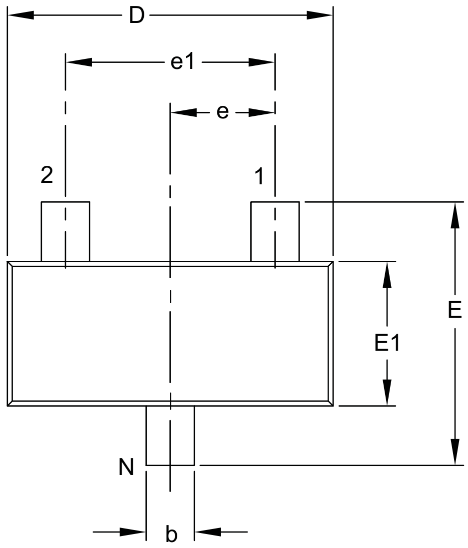
1. Dimensioning and tolerancing per ASME Y14.5M

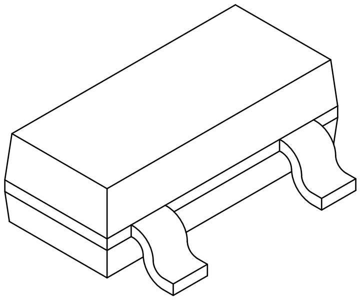
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

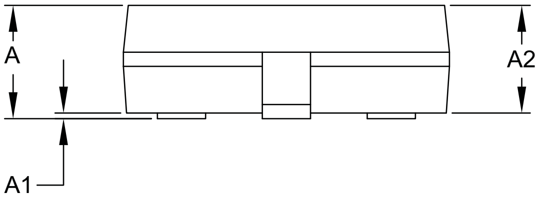
Microchip Technology Drawing No. C04-2032A

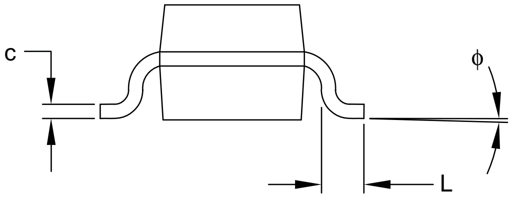
3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	3		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.89	–	1.45
Molded Package Thickness	A2	0.90	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.10	–	3.00
Molded Package Width	E1	1.20	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.15	–	0.60
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.09	–	0.26
Lead Width	b	0.30	–	0.51

Notes:

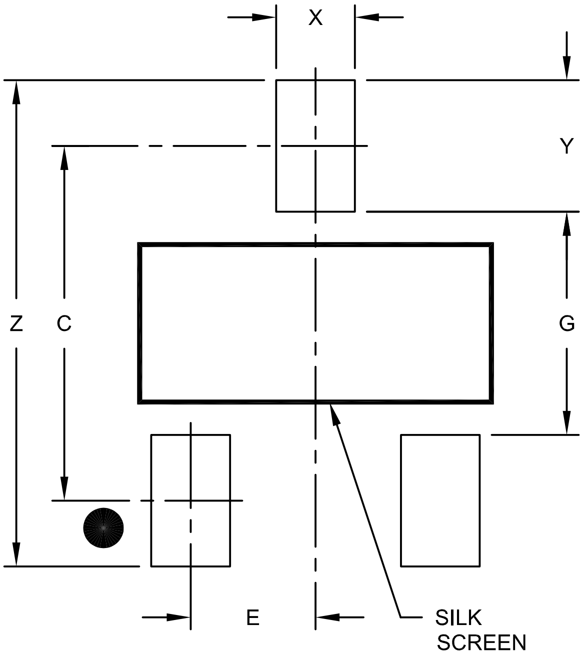
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-130B

3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.70	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.00
Distance Between Pads	G	1.70		
Overall Width	Z			3.70

Notes:

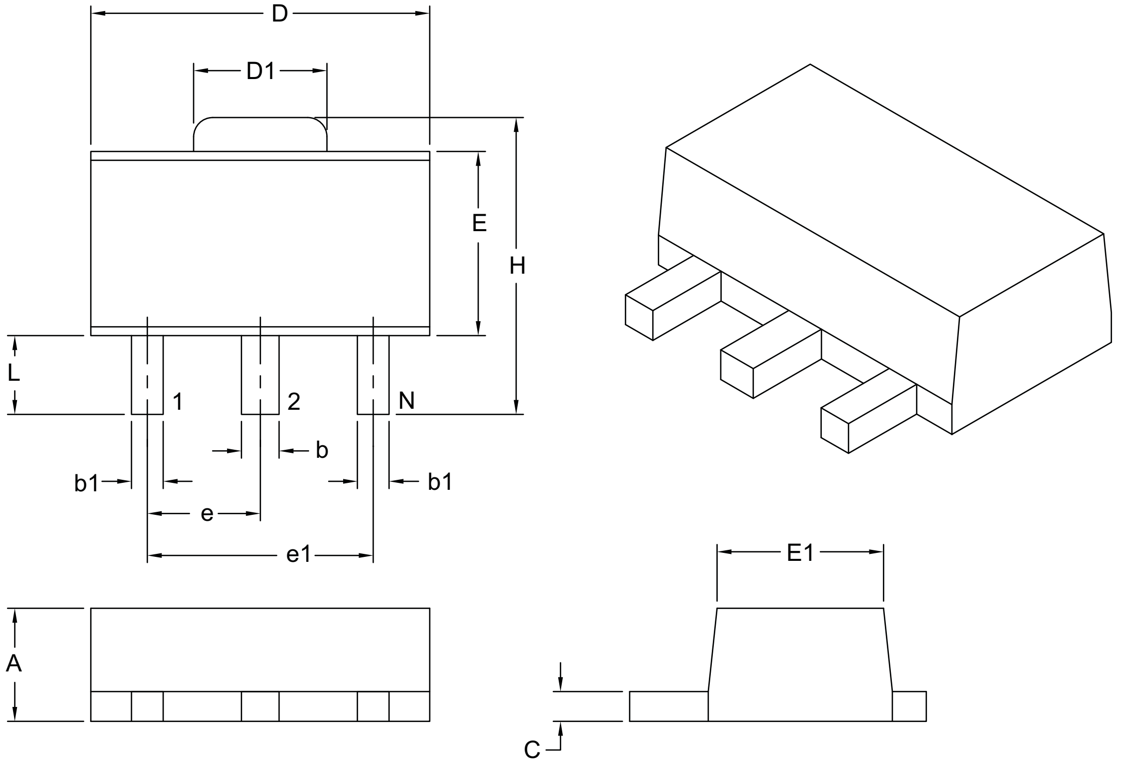
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2130A

3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS	
Dimension Limits		MIN	MAX
Number of Leads	N	3	
Pitch	e	1.50 BSC	
Outside Lead Pitch	e1	3.00 BSC	
Overall Height	A	1.40	1.60
Overall Width	H	3.94	4.25
Molded Package Width at Base	E	2.29	2.60
Molded Package Width at Top	E1	2.13	2.29
Overall Length	D	4.39	4.60
Tab Length	D1	1.40	1.83
Foot Length	L	0.79	1.20
Lead Thickness	c	0.35	0.44
Lead 2 Width	b	0.41	0.56
Leads 1 & 3 Width	b1	0.36	0.48

Notes:

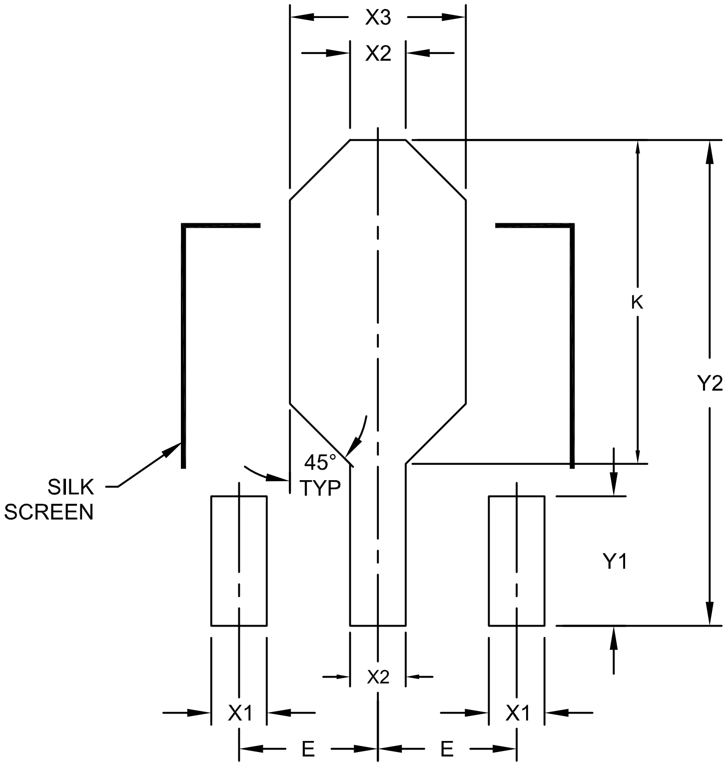
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029B

3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.50 BSC		
Contact Pads 1 & 3 Width	X1			0.48
Contact Pad 2 Width	X2			0.56
Heat Slug Pad Width	X3			1.20
Contact Pads 1 & 3 Length	Y1		1.40	
Contact 2 Pad Length	Y2			4.25
-	K	2.60		2.85

Notes:

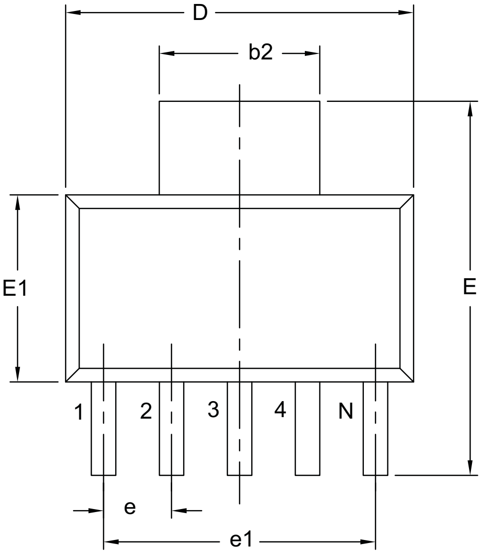
1. Dimensioning and tolerancing per ASME Y14.5M

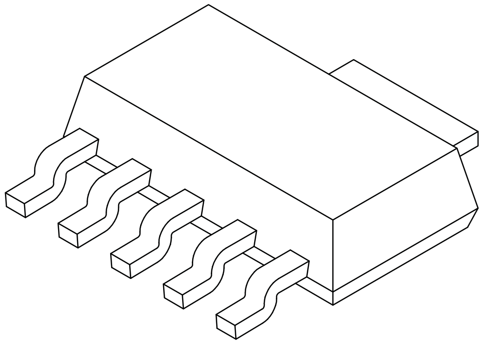
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

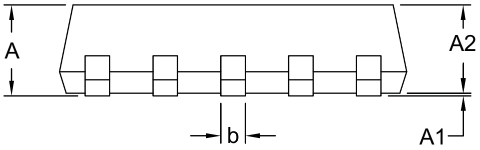
Microchip Technology Drawing No. C04-2029A

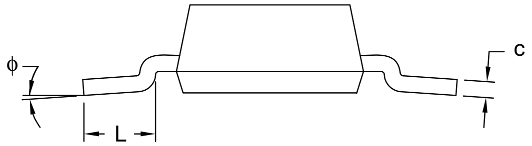
5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	5		
Lead Pitch	e	1.27 BSC		
Outside Lead Pitch	e1	5.08 BSC		
Overall Height	A	–	–	1.80
Standoff	A1	0.02	0.06	0.10
Molded Package Height	A2	1.55	1.60	1.65
Overall Width	E	6.86	7.00	7.26
Molded Package Width	E1	3.45	3.50	3.55
Overall Length	D	6.45	6.50	6.55
Lead Thickness	c	0.24	0.28	0.32
Lead Width	b	0.41	0.457	0.51
Tab Lead Width	b2	2.95	3.00	3.05
Foot Length	L	0.91	–	1.14
Lead Angle	ϕ	0°	4°	8°

Notes:

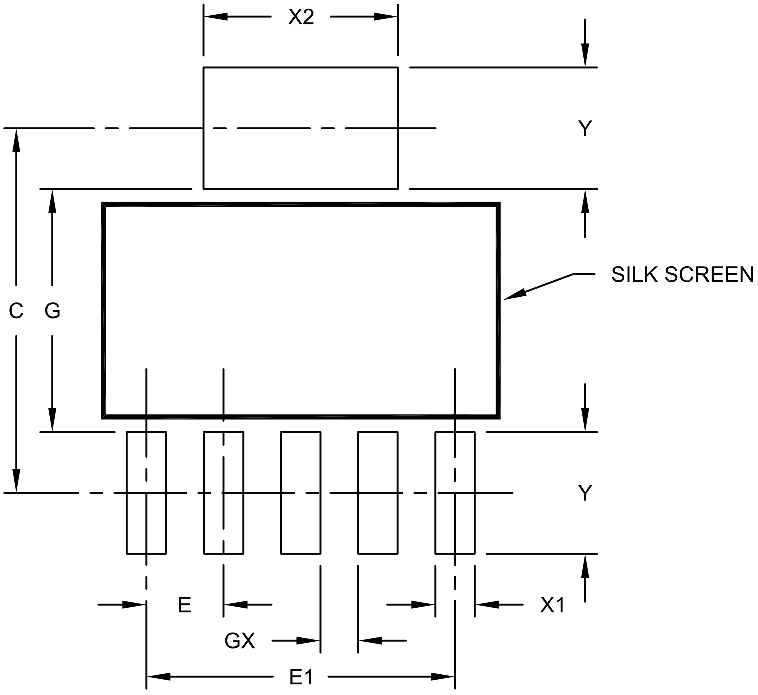
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-137B

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Pad Pitch	E		1.27 BSC	
Overall Pad Pitch	E1		5.08 BSC	
Pad Spacing	C		6.00	
Pad Width	X1			0.65
Pad Width	X2			3.20
Pad Length	Y			2.00
Distance Between Pads	G	4.00		
Distance Between Pads	GX	0.62		

Notes:

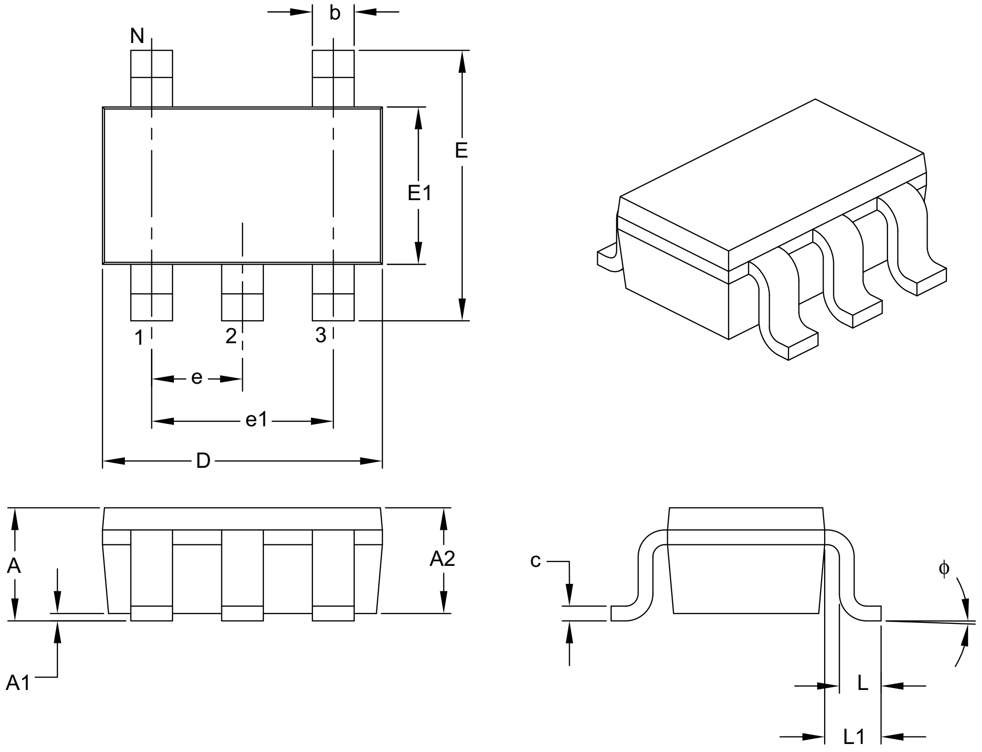
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2137A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

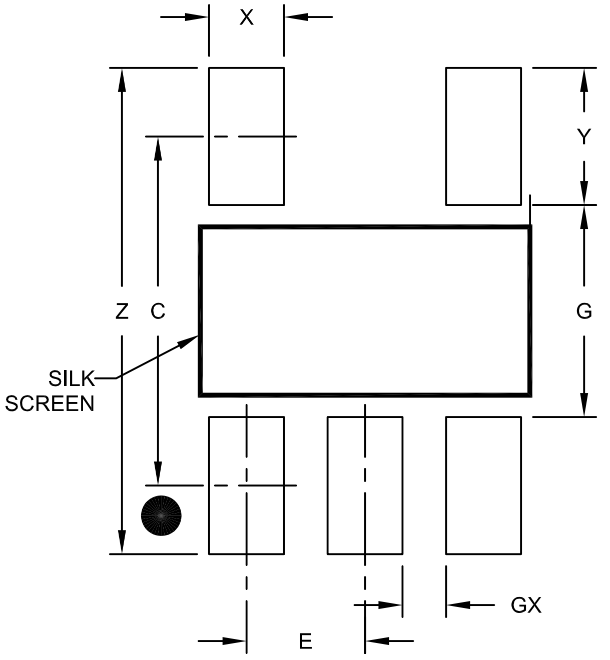
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

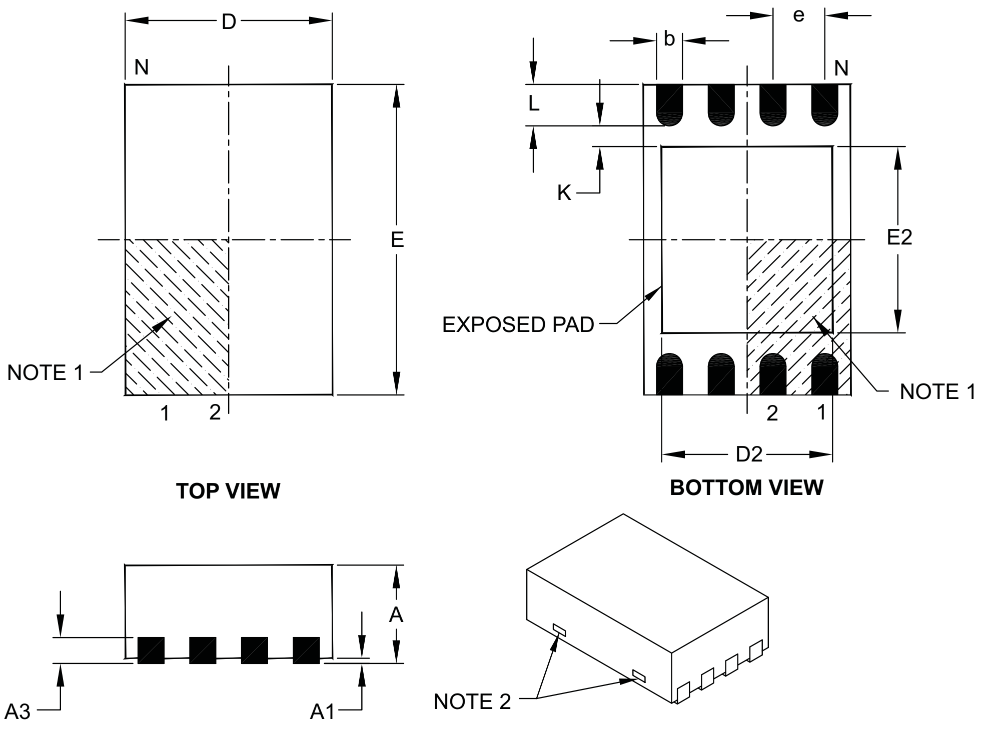
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

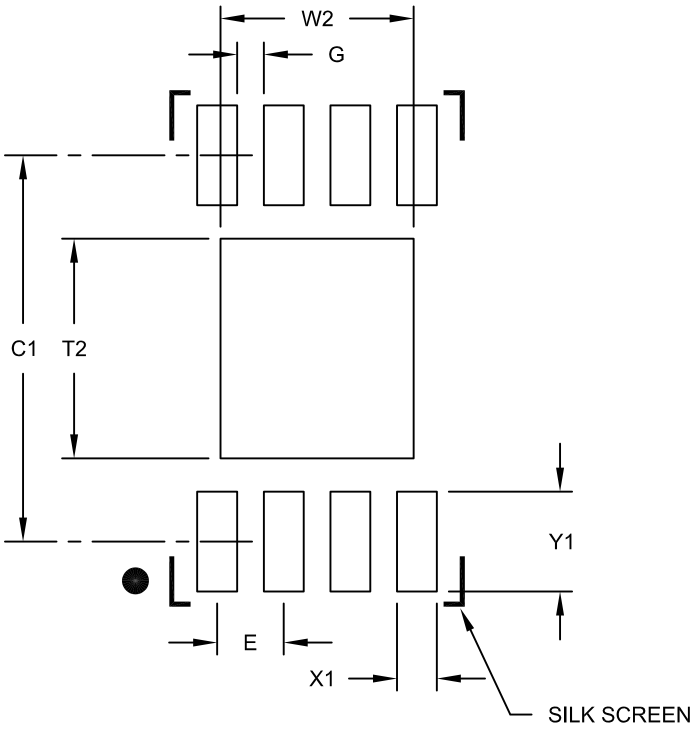
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

APPENDIX A: REVISION HISTORY

Revision C (September 2013)

The following is the list of modifications:

1. Corrected Product Identification System examples.
2. Minor editorial corrections.

Revision B (April 2013)

The following is the list of modifications:

1. Updated Note 5 in the AC/DC Characteristics table.
2. Updated Figure 2-20.
3. Minor grammatical and spelling corrections.

Revision A (August 2011)

4. Original data sheet for the MCP1754/MCP1754S family of devices.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	XX	X	X	X/	XX
Device	Tape and Reel	Output Voltage	Feature Code	Tolerance	Temp.	Package

Device:	MCP1754:	150 mA, 16V High-Performance LDO
	MCP1754T:	150 mA, 16V High-Performance LDO (Tape and Reel) (SOT)
	MCP1754S:	150 mA, 16V High-Performance LDO
	MCP1754ST:	150 mA, 16V High-Performance LDO (Tape and Reel) (SOT)
Tape and Reel:	T	= Tape and Reel
Output Voltage*:	18	= 1.8V “Standard”
	33	= 3.3V “Standard”
	50	= 5.0V “Standard”
	*Contact factory for other voltage options	
Extra Feature Code:	0	= Fixed
Tolerance:	2	= 2% (Standard)
Temperature Range:	E	= -40°C to +125°C
Package:	CB	= Plastic Small Outline, (SOT-23A), 3-lead
	DB*	= Plastic Small Outline, (SOT-223), 3-lead
	DC	= Plastic Small Outline, (SOT223), 5-lead
	MB	= Plastic Small Outline, (SOT-89), 3-lead
	MC	= Plastic Dual Flat, No Lead, (2x3 DFN), 8-lead
	OT	= Plastic Small Outline, (SOT-23), 5-lead
	*Note: The 3-lead SOT-223 (DB) is not a standard package for output voltages below 3.0V	

Examples:

a) MCP1754T-1802E/DC: 1.8V, 5LD SOT-223, Tape and Reel
b) MCP1754T-3302E/DC: 3.3V, 5LD SOT-223, Tape and Reel
c) MCP1754T-5002E/DC: 5.0V, 5LD SOT-223, Tape and Reel

a) MCP1754T-1802E/OT: 1.8V, 5LD SOT-23, Tape and Reel
b) MCP1754T-3302E/OT: 3.3V, 5LD SOT-23, Tape and Reel
c) MCP1754T-5002E/OT: 5.0V, 5LD SOT-23, Tape and Reel

a) MCP1754T-1802E/MC: 1.8V, 8LD DFN, Tape and Reel
b) MCP1754T-3302E/MC: 3.3V, 8LD DFN, Tape and Reel
c) MCP1754T-5002E/MC: 5.0V, 8LD DFN, Tape and Reel

a) MCP1754ST-3302E/DB: 3.3V, 3LD SOT-223, Tape and Reel
b) MCP1754ST-5002E/DB: 5.0V, 3LD SOT-223, Tape and Reel

a) MCP1754ST-1802E/CB: 1.8V, 3LD SOT-23A, Tape and Reel
b) MCP1754ST-3302E/CB: 3.3V, 3LD SOT-23A, Tape and Reel
c) MCP1754ST-5002E/CB: 5.0V, 3LD SOT-23A, Tape and Reel

a) MCP1754ST-1802E/MB: 1.8V, 3LD SOT-89, Tape and Reel
b) MCP1754ST-3302E/MB: 3.3V, 3LD SOT-89, Tape and Reel
c) MCP1754ST-5002E/MB: 5.0V, 3LD SOT-89, Tape and Reel

a) MCP1754ST-1802E/MC: 1.8V, 8LD DFN, Tape and Reel
b) MCP1754ST-3302E/MC: 3.3V, 8LD DFN, Tape and Reel
c) MCP1754ST-5002E/MC: 5.0V, 8LD DFN, Tape and Reel

NOTES:

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