
HAF2011(L),HAF2011(S)

Silicon N Channel MOS FET Series
Power Switching

HITACHI

ADE-208-738 (Z)
Target specification
1st. Edition
Jan. 1999

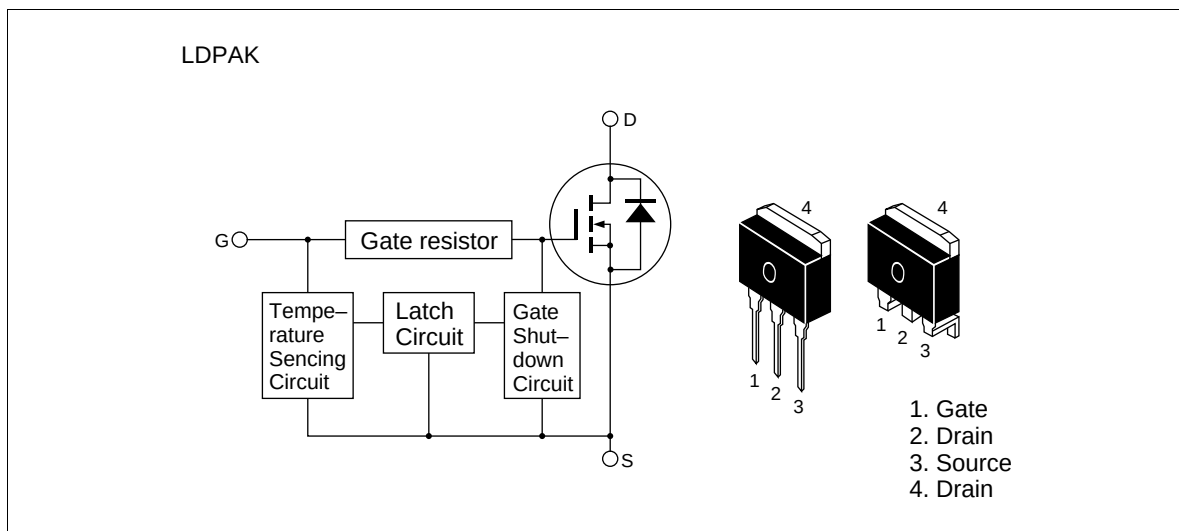
Features

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut-down operation (Need 0 voltage recovery)

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Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	16	V
Gate to source voltage	V_{GSS}	-2.5	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}^{*1}$	80	A
Body-drain diode reverse drain current	I_{DR}	40	A
Channel dissipation	P_{ch}^{*2}	50	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. Value at Ta = 25°C

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Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current	I_{IH1}	—	—	100	μA	$V_i = 8V, V_{DS} = 0$
(Gate non shut down)	I_{IH2}	—	—	50	μA	$V_i = 3.5V, V_{DS} = 0$
	I_{IL}	—	—	1	μA	$V_i = 1.2V, V_{DS} = 0$
Input current	$I_{IH(sd)1}$	—	0.8	—	mA	$V_i = 8V, V_{DS} = 0$
(Gate non shut down)	$I_{IH(sd)2}$	—	0.35	—	mA	$V_i = 3.5V, V_{DS} = 0$
Shut down temperature	T_{sd}	—	175	—	$^{\circ}C$	Channel temperature
Gate operation voltage	V_{OP}	3.5	—	12	V	

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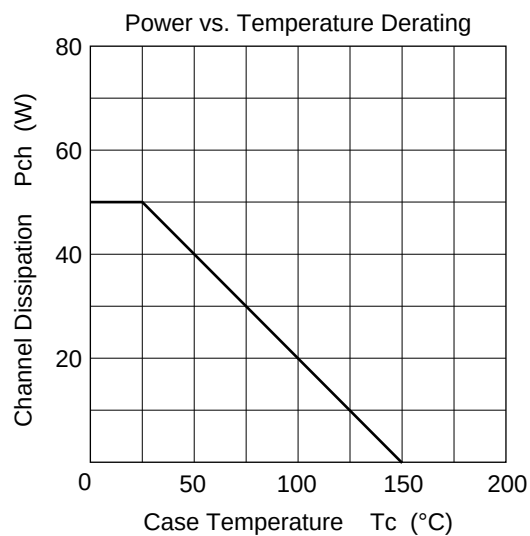
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	(25)	—	—	A	$V_{GS} = 3.5V, V_{DS} = 2V$
Drain current	I_{D2}	—	—	10	mA	$V_{GS} = 1.2V, V_{DS} = 2V$
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10mA, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	(16)	—	—	V	$I_G = (300\mu A), V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	(-2.5)	—	—	V	$I_G = (-100\mu A), V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	100	μA	$V_{GS} = 8V, V_{DS} = 0$
	I_{GSS2}	—	—	50	μA	$V_{GS} = 3.5V, V_{DS} = 0$
	I_{GSS3}	—	—	1	μA	$V_{GS} = 1.2V, V_{DS} = 0$
	I_{GSS4}	—	—	-100	μA	$V_{GS} = -2.4V, V_{DS} = 0$
Input current (shut down)	$I_{GS(op)1}$	—	0.8	—	mA	$V_{GS} = 8V, V_{DS} = 0$
	$I_{GS(op)2}$	—	0.35	—	mA	$V_{GS} = 3.5V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	$V_{DS} = 50V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	$I_D = 1mA, V_{DS} = 10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	25	33	m Ω	$I_D = 20A, V_{GS} = 4V^{*3}$
Static drain to source on state resistance	$R_{DS(on)}$	—	15	20	m Ω	$I_D = 20A, V_{GS} = 10V^{*3}$
Forward transfer admittance	$ y_{fs} $	25	50	—	S	$I_D = 20A, V_{DS} = 10V^{*3}$
Output capacitance	C_{oss}	—	940	—	pF	$V_{DS} = 10V, V_{GS} = 0$ $f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	(7.8)	—	μs	$I_D = 5A, V_{GS} = 5V$
Rise time	t_r	—	(64)	—	μs	$R_L = 6\Omega$
Turn-off delay time	$t_{d(off)}$	—	(19)	—	μs	
Fall time	t_f	—	(30)	—	μs	
Body-drain diode forward voltage	V_{DF}	—	(0.85)	—	V	$I_F = 40A, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	()	—	ns	$I_F = 40A, V_{GS} = 0$ $diF/dt = 50A/\mu s$
Over load shut down	t_{os1}	—	()	—	ms	$V_{GS} = 5V, V_{DD} = 12V$
operation time ^{*4}	t_{os2}	—	()	—	ms	$V_{GS} = 5V, V_{DD} = 24V$

Note: 3. Pulse test

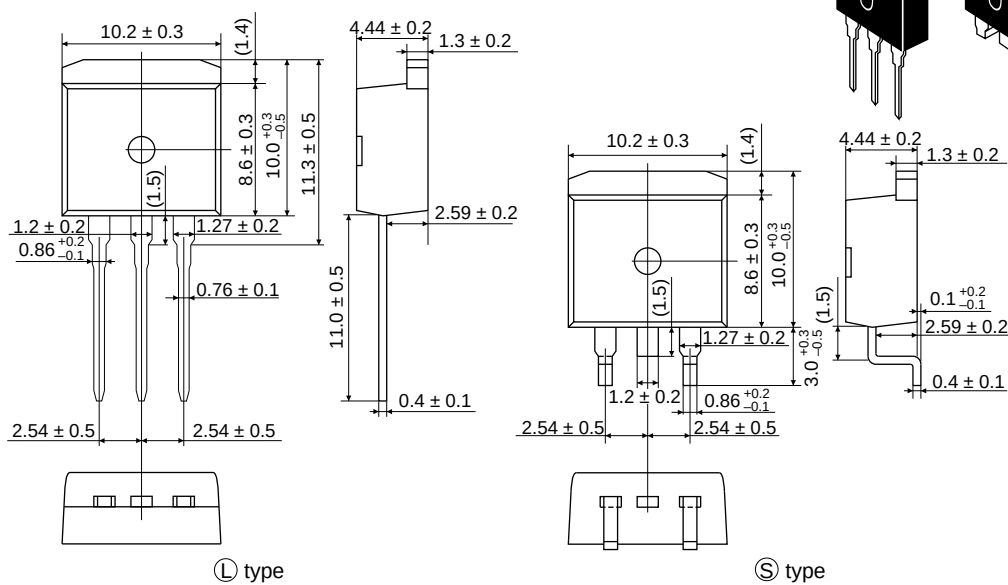
4. Include the time shift based on increasing of channel temperature when operate under over load condition.

Main Characteristics



Package Dimensions

Unit: mm



Hitachi Code	LDPAK
EIAJ	—
JEDEC	—

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