HMC1044LP3E

PROGRAMMABLE HARMONIC LOW PASS FILTER 1 - 3 GHz 3 dB BANDWIDTH

Typical Applications

The HMC1044LP3E is ideal for wideband transceiver harmonic filtering applications including:

- Filtering LO Harmonics to Reduce Modulator Sideband Rejection & Demodulator Image Rejection
- Amplifier Harmonic Filtering
- RF Filtering

Features

Programmable Bandwidth: 1 to 3 GHz

Compatible with Narrowband & Wideband:
- PLLs with Integrated VCOs
- Modulators
- Demodulators

LO Harmonic Rejection: ~20 dB

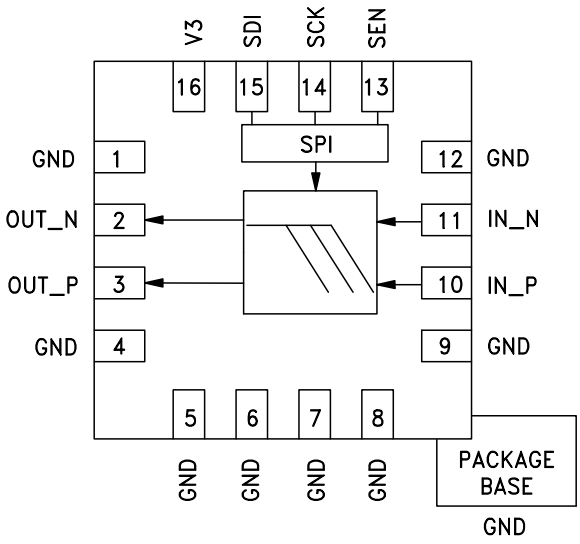
Improves Modulator/Demodulator Sideband/Image Rejection Performance: 20 dB Typical

Single-Ended or Differential Options

Footprint up to 90% Smaller than Current Discrete Fixed Bandwidth Solutions

16 Lead 3x3 mm SMT Package

Functional Diagram



General Description

The HMC1044LP3E is a programmable bandwidth LPF (Low Pass Filter) targeted at all applications that use quadrature modulators and/or demodulators. The HMC1044LP3E filters out LO harmonics and ensures little or no LO contribution to modulator sideband rejection or demodulator image rejection performance.

Although targeted at LO filtering applications, the HMC1044LP3E can be used to filter all RF harmonics such as the ones generated by amplifiers.

The HMC1044LP3E offers a choice of 16 programmable bands, optimized for high and low cellular bands ranging from 1 to 3 GHz, making the HMC1044LP3E a truly wideband part compatible with wideband PLLs with Integrated VCOs and wideband quadrature modulators and demodulators. It enables wideband multi-standard, multi-carrier designs that are field configurable on-the-fly for each individual application.

The HMC1044LP3E is packaged in a compact 3x3 mm QFN leadless package.

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Electrical Specifications, T_A = +25 °C, V3 = 3.3 V (3 V to 3.5 V)

Parameter	Min.	Typ.	Max.	Units
Single-Ended				
Passband[1]	250		3060	MHz
ƒcutoff[2] Tuning Range (3 dB Loss)	1025		3060	MHz
Passband Flatness		2.5		dB
Passband Insertion Loss		3	5	dB
Return Loss		10		dB
Input/Output Impedance		50		Ω
Input IP3 (inband)		43		dBm
Differential				
Passband[1]	250		3400	MHz
ƒcutoff[2] Tuning Range (3 dB Loss)	970		3400	MHz
Passband Flatness		2.5		dB
Passband Insertion Loss		3	5	dB
Return Loss		10		dB
Input/Output Impedance		100		Ω
Input IP3 (inband)		43		dBm
Supplies				
DC Supply	3	3.3	3.5	V
Supply Current		1		uA
Digital Inputs				
Digital Input Low Level (VIL)			0.4	V
Digital Input High Level (VIH)	1.5			V

[1] Minimum frequency is limited by external DC blocking capacitor. Displayed value corresponds to default evaluation board configuration of 100 pF.

[2] ƒcutoff defined as the point at which the insertion loss is 3 dB below the passband insertion loss @ 500 MHz.

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Figure 1. Single-Ended Insertion Loss [1]

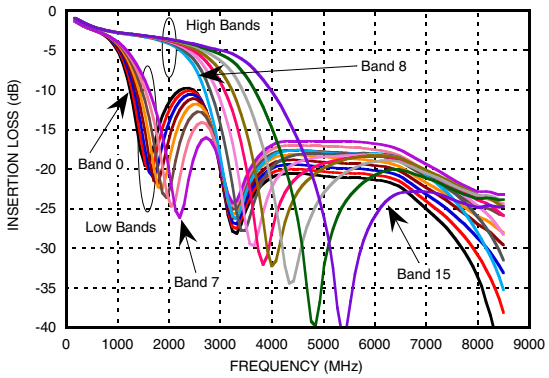


Figure 2. Differential Insertion Loss [1]

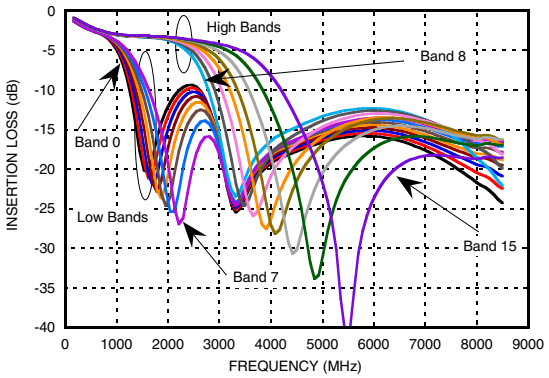


Figure 3. Single-Ended Insertion Loss Over Supply Voltage [1]

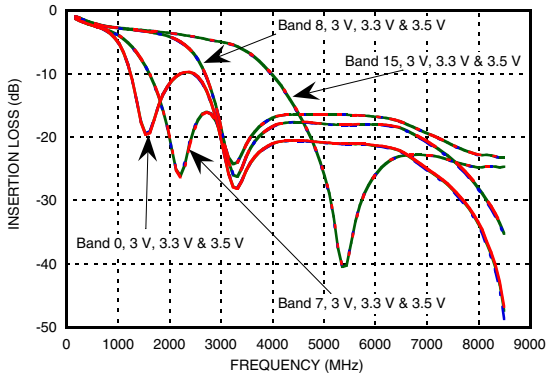


Figure 4. Single-Ended Insertion Loss Over Temperature [1]

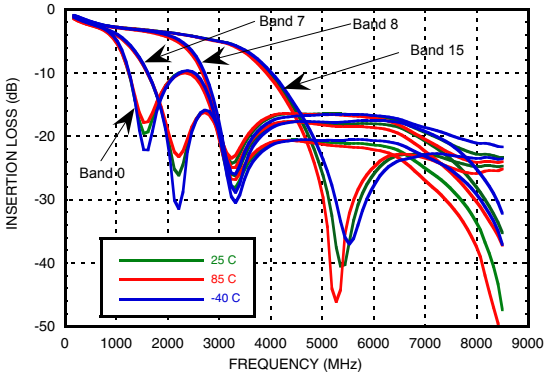


Figure 5. Single-Ended Return Loss [1]

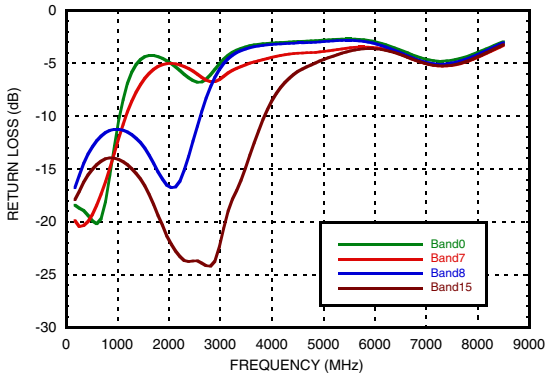
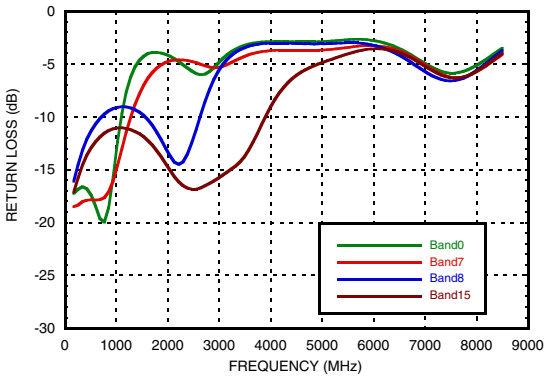


Figure 6. Differential Return Loss [1]



[1] Low frequency performance limited by external DC blocking capacitors at RF input and output.

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Figure 7. Single-Ended Return Loss vs. V3[1]

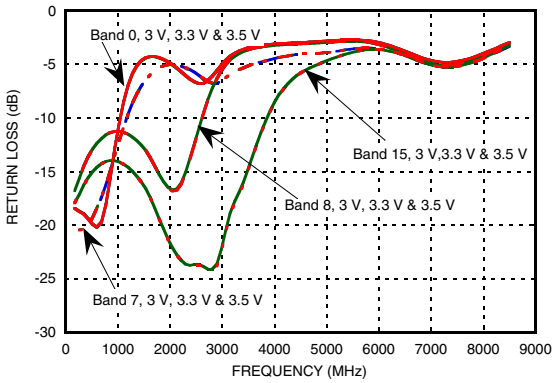


Figure 8. Single-Ended Return Loss vs. Temperature[1]

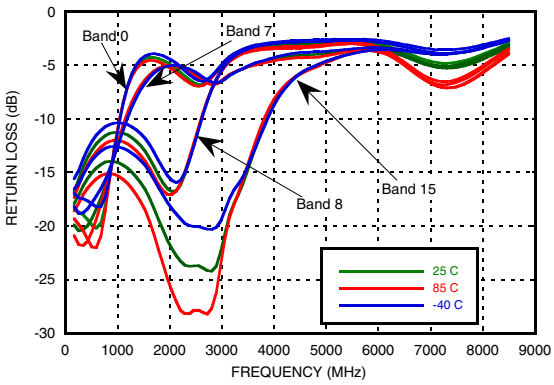
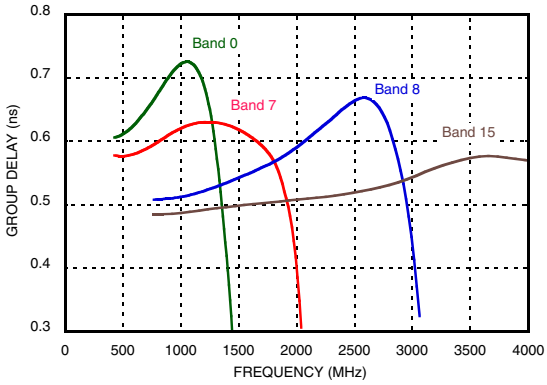


Figure 9. Single-Ended Filter Group Delay[1]



[1] Low frequency performance limited by external DC blocking capacitors at RF input and output.

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HMC1044LP3E Frequency Bands

HMC1044LP3E Band Setting	Typical 3 dB Cutoff Frequency Relative to 500 MHz	
	Single-Ended	Differential
0	1025	970
1	1050	1000
2	1075	1030
3	1105	1055
4	1130	1085
5	1160	1120
6	1195	1155
7	1225	1195
8	2230	2335
9	2300	2430
10	2380	2530
11	2465	2655
12	2550	2770
13	2675	2940
14	2805	3145
15	3060	3400

PROGRAMMABLE HARMONIC LOW PASS FILTER 1 - 3 GHz 3 dB BANDWIDTH

Absolute Maximum Ratings

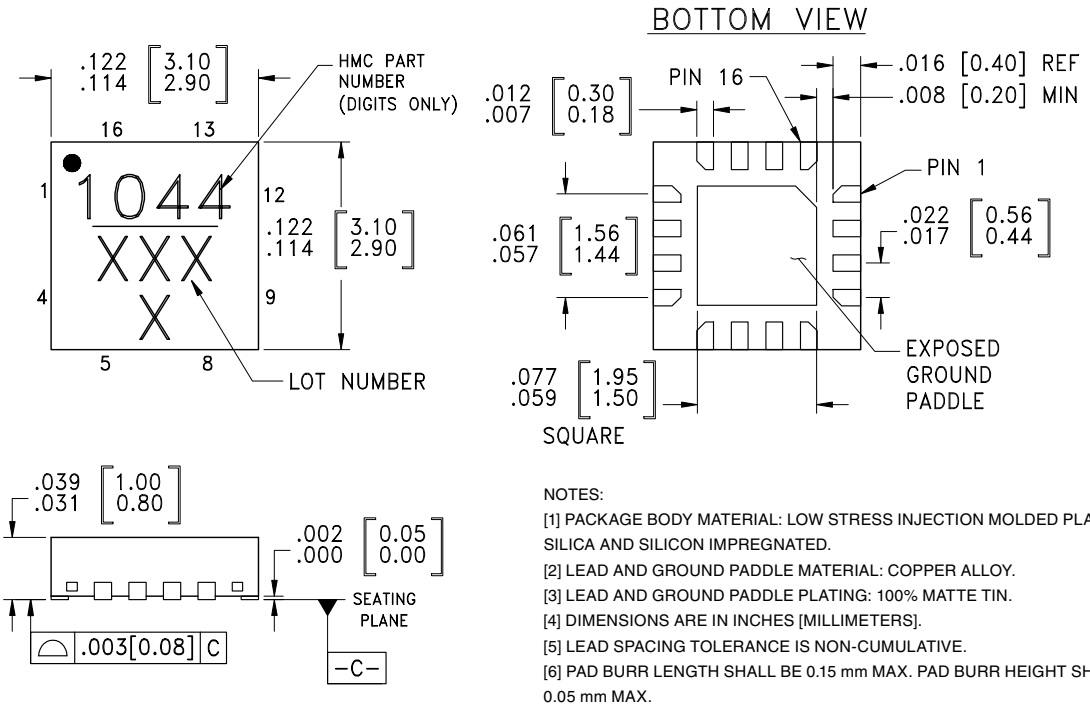
Parameter	Rating
V3	-0.3 to +3.6 V
RF Power Input	18 dBm
Digital Input Voltage Range	-0.3 to +3.6 V
Storage Temperature	-65 to +150 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec

Reliability Information

Maximum Junction Temperature	125 °C
Operating Temperature	-40 to +85 °C
ESD Rating (HBM)	Class 2
Thermal Resistance	90 °C/W

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



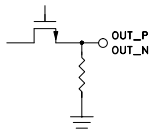
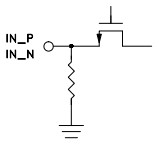
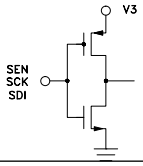
NOTES:
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15 mm MAX. PAD BURR HEIGHT SHALL BE 0.05 mm MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05 mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1044LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	1044 XXXX

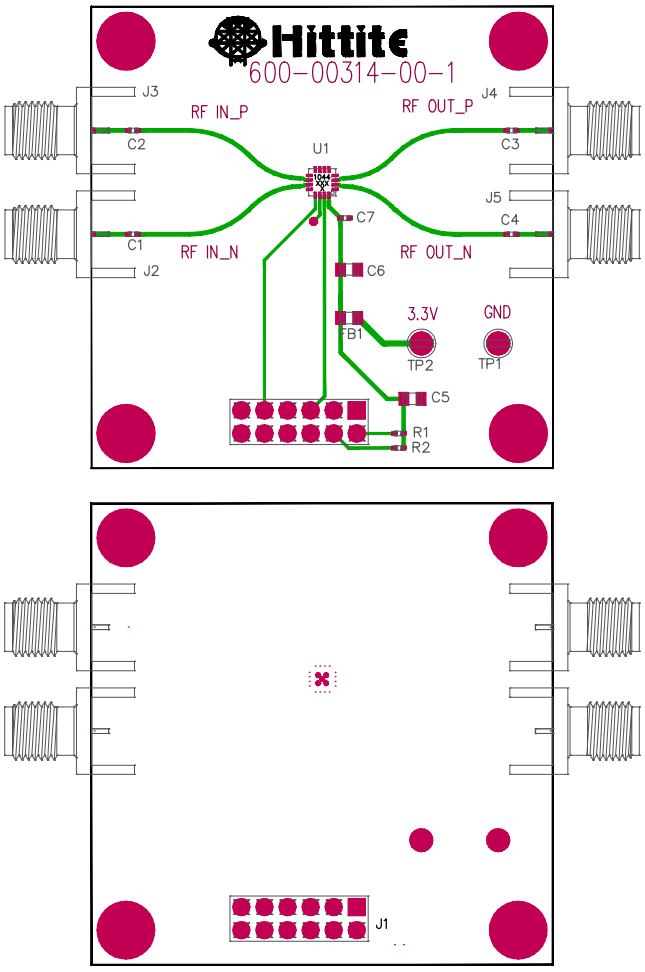
[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 6, 7, 8, 9, 12	GND	These pins and exposed paddle must be connected to RF/DC ground.	
2	OUT_N	This pin is DC coupled and matched to 50 Ohms. External voltage must not be applied to this pin. [1]	
3	OUT_P	This pin is DC coupled and matched to 50 Ohms. External voltage must not be applied to this pin. [1]	
10	IN_P	This pin is DC coupled and matched to 50 Ohms. External voltage must not be applied to this pin. [1]	
11	IN_N	This pin is DC coupled and matched to 50 Ohms. External voltage must not be applied to this pin. [1]	
13	SEN	Serial Port Enable (CMOS) Logic Input	
14	SCK	Serial Port Clock (CMOS) Logic Input	
15	SDI	Serial Port Data (CMOS) Logic Input	
16	V3	DC Power Supply	

[1] Although the pins are DC coupled they require external AC coupling for proper operation. Please refer to *Evaluation PCB Schematic* for more information.

Evaluation PCB



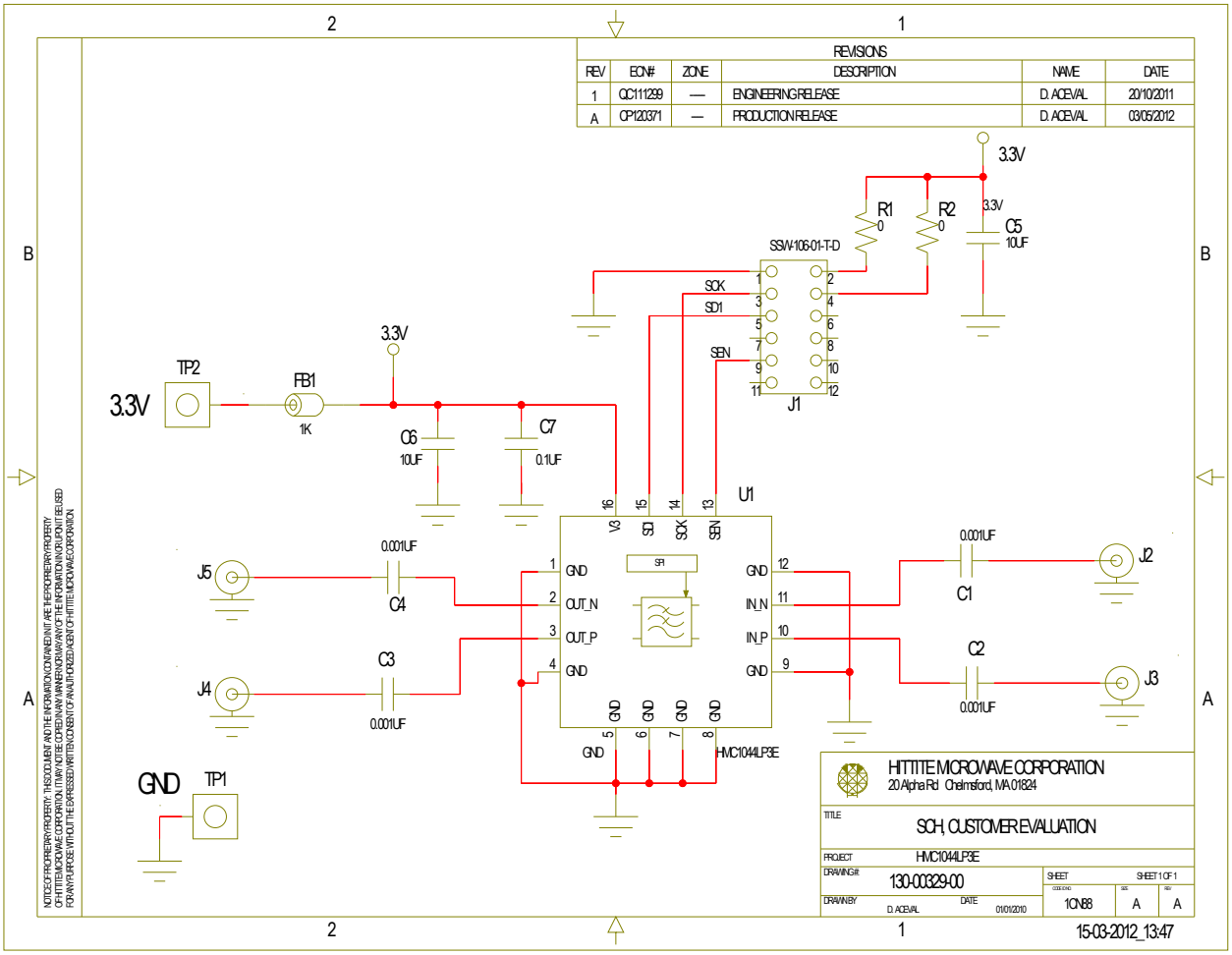
The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1044LP3E Evaluation PCB	EVAL01-HMC1044LP3E
Evaluation Kit	HMC1044LP3E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software)	EKIT01-HMC1044LP3E

PROGRAMMABLE HARMONIC LOW PASS FILTER 1 - 3 GHz 3 dB BANDWIDTH

Evaluation PCB Schematic



HMC1044LP3E Application Information

The HMC1044LP3E is an ideal LO harmonic filter for wideband applications featuring quadrature modulators and/or demodulators. The HMC1044LP3E's 16 user programmable bands enable the user to optimally attenuate 2nd and/or 3rd LO harmonics in order to maximize quadrature modulator/demodulator sideband/image rejection performance. Typical diagrams with the HMC1044LP3E are shown in *Figure 10* and *Figure 11*.

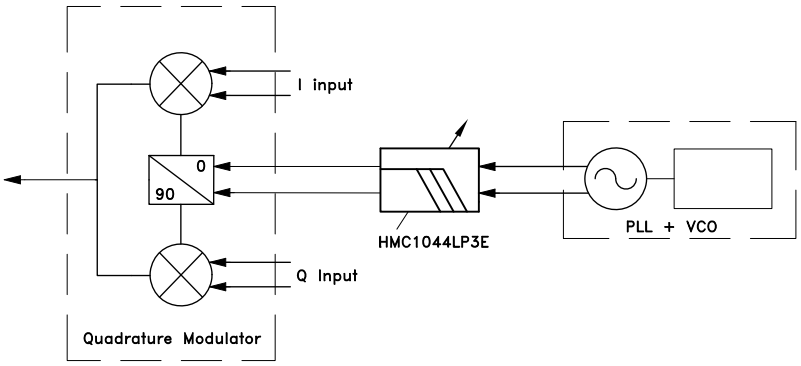


Figure 10. Typical HMC1044LP3E transmitter application

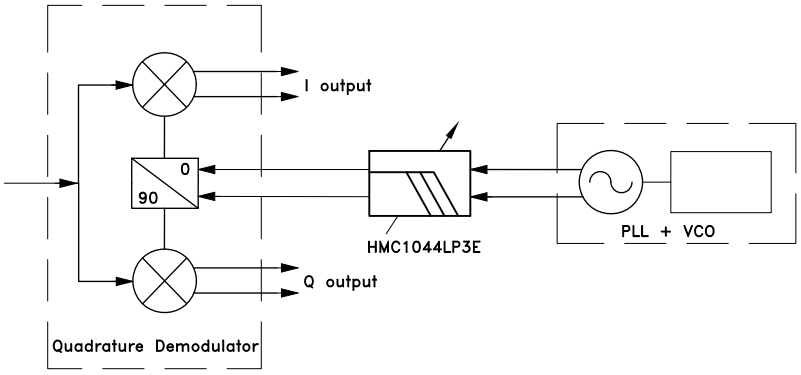


Figure 11. Typical HMC1044LP3E receiver application

Background, LO Harmonics and Modulator/Demodulator Sideband/Image Rejection

Most wideband quadrature modulators/demodulators in the market use some form of a filter to create the required in-phase and quadrature LO components at the fundamental frequency of the LO (1xLO). Others, less common modulators/demodulators accept LO input at 2xLO frequency and are not based upon filters. The 1xLO types are particularly sensitive to LO 3rd harmonic levels, while the 2xLO types are more sensitive to 2nd harmonic levels.

Harmonics are normally present in all VCOs and especially in RFICs with integrated VCOs. High LO harmonic content causes amplitude and phase mismatches, and ultimately performance degradation in modulator sideband rejection and demodulator image rejection, as shown in *Figure 12*.

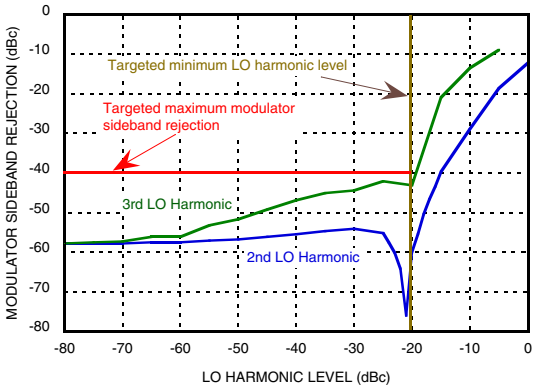


Figure 12. Typical impact of 2nd and 3rd LO harmonic on modulator sideband rejection.[1]

Figure 12 shows a typical modulator with 1xLO input, where both the 2nd and 3rd LO harmonics affect the modulator sideband rejection performance at levels > -20 dBc relative to the LO signal power. It also shows that the 3rd LO harmonic has greater impact on modulator sideband rejection performance than the 2nd, and that there is little effect of the 2nd LO harmonic on modulator sideband rejection once the 2nd LO harmonic is below -20 dBc levels, relative to the LO signal level.

The HMC1044LP3E is designed to ensure that the 2nd and the 3rd LO harmonics are below -20 dBc relative to the LO signal level across the entire operating range of Hittite's wideband PLLs with integrated VCOs. Thereby ensuring little or no LO contribution is added to modulator/demodulator sideband/image rejection performance degradation.

Using the HMC1044LP3E

Modulator/demodulator sideband/image rejection performance is specific to each individual modulator/demodulator, and depends on a number of other variables including: type (1xLO or 2xLO input), balance (amplitude and phase matching), signal path matching and interface to other components, board layout, input signal bandwidth, and LO harmonics.

Figure 12 shows that typically the LO harmonics stop being a dominant contributor to modulator/demodulator sideband/image rejection performance degradation once they are below approximately -20 dBc relative to the LO signal level. However, the exact level at which harmonics cease being the dominant contributor to sideband/image rejection performance depends on each individual modulator/demodulator and each individual design. Hence, the optimal band selection of the HMC1044LP3E may be different for different designs.

Figure 13 shows optimal 3rd harmonic attenuation achieved with the HMC1044LP3E without optimizing the 2nd harmonic, when the HMC830LP6GE PLL with Integrated VCO is used as an LO to drive the HMC697LP4E quadrature modulator. The corresponding HMC1044LP3E band selections are shown in Figure 14.

[1] Measured with HMC697LP4E direct modulator at 2 GHz, with LO input power = 0 dBm, 1xLO type.

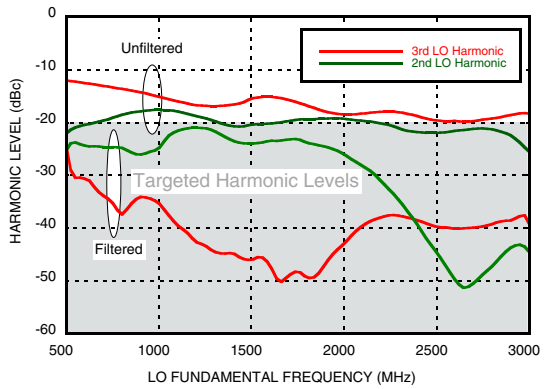


Figure 13. Maximum HMC1044LP3E attenuation of 3rd harmonic of the LO[2]

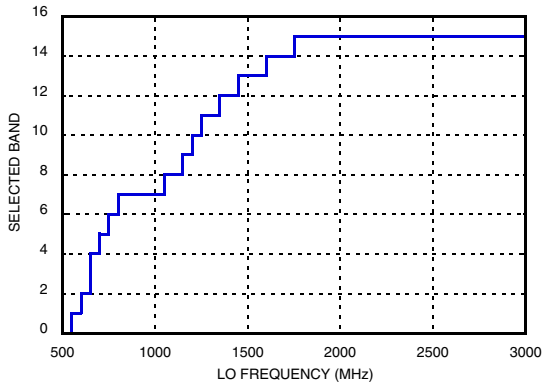


Figure 14. HMC1044LP3E band selection corresponding to Figure 13

Observing the results shown in Figure 13 in the context of targeted performance in Figure 12; It is apparent that the HMC1044LP3E attenuates both the 3rd and the 2nd LO harmonics to well below the targeted maximum LO harmonic level shown in Figure 12, ensuring that the targeted modulator sideband rejection performance is achieved.

Figure 15 shows the optimal 2nd harmonic attenuation achieved with the HMC1044LP3E, when the HMC830LP6GE PLL with Integrated VCO is used as an LO to drive the HMC697LP4E quadrature modulator. The corresponding HMC1044LP3E band selection is shown in Figure 16.

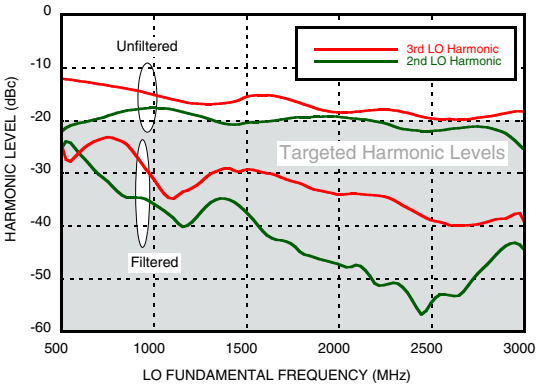


Figure 15. Maximum HMC1044LP3E attenuation of 2nd harmonic of the LO [2]

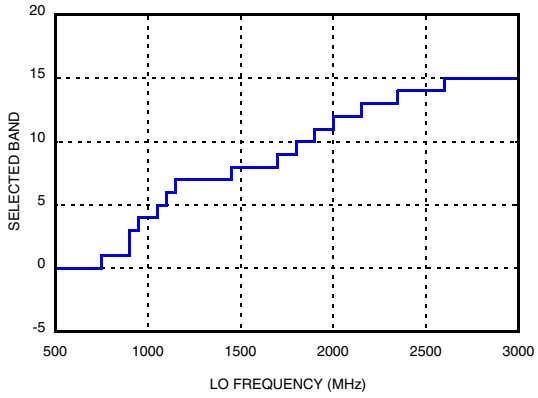


Figure 16. HMC1044LP3E band selection corresponding to Figure 15

Observing the results shown in Figure 15 in the context of the targeted performance in Figure 12; it is apparent that the HMC1044LP3E attenuates both the 3rd and the 2nd LO harmonics to well below the targeted maximum LO harmonic level shown in Figure 12, ensuring that the targeted modulator sideband rejection performance shown in Figure 12 is achieved.

Using the relationship between sideband/image rejection vs. LO harmonic distortion in Figure 12 as a reference, it can be observed that both approaches (maximizing 2nd harmonic attenuation in Figure 13, and maximizing 3rd harmonic attenuation in Figure 14) achieve sideband/image rejection performance improvement, and effectively remove any LO contribution to sideband/image rejection performance degradation. However, Figure 12 suggests that, when using a 1xLO type modulator, more emphasis should be placed on attenuating the 3rd harmonic than the second because the 2nd harmonic ceases to be a contributor at levels ~<-20 dBc, while the 3rd harmonic continues contributing to sideband/image rejection, albeit at a smaller rate for the particular design characterized in Figure 12.

[2] Measured with HMC830LP6GE as an LO and HMC697LP4E modulator. The HMC830LP6GE was used in single-ended output configuration.

Figure 17 shows the maximum sideband rejection achieved without calibrating the modulator, both with and without the HMC1044LP3E. It is generated by selecting the HMC1044LP3E band that achieves maximum uncalibrated sideband rejection for each particular frequency accross a very wide bandwidth. The corresponding HMC1044LP3E band settings are shown in Figure 18.

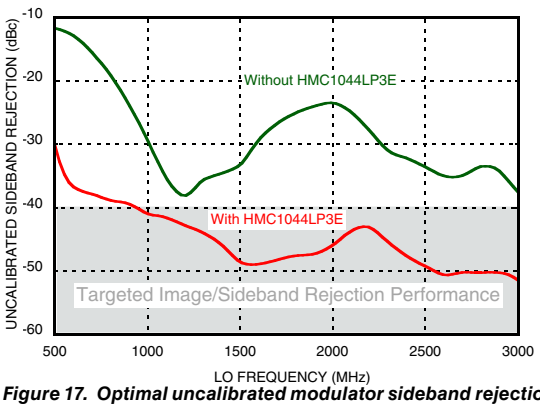


Figure 17. Optimal uncalibrated modulator sideband rejection with and and without HMC1044LP3E, single-ended LO configuration[3]

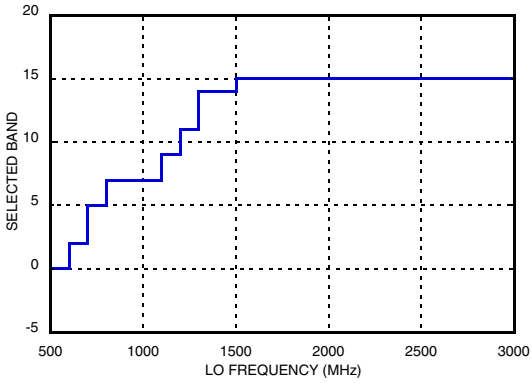


Figure 18. HMC1044LP3E band selection corresponding to Figure 17

Results shown in Figure 17 confirm that the HMC1044LP3E improves modulator sideband rejection ~20 dB across the wideband operation of the modulator and PLL with integrated VCO. Sideband rejection performance improvements less than ~20 dB occur at those frequencies where the LO harmonics are not a dominant contributor to sideband rejection, ie. where sideband rejection performance is already good.

The corresponding HMC1044LP3E band selections shown in Figure 18 are closer to those shown in Figure 14, than those from Figure 16. This confirms the data shown in Figure 12, and the postulation that the 3rd LO harmonic is a greater contributor to modulator sideband rejection degradation than the 2nd for 1xLO type modulators/demodulators.

Another variable that should be considered is the insertion loss of the HMC1044LP3E which can vary ~2.5 dB across the pass band of the selected band setting as shown in Figure 1 and Figure 2. The selected HMC1044LP3E band that results in optimal sideband/image rejection performance also depends on the LO input power at the modulator/demodulator, which is specific to each individual design. It depends on the output power of the PLL with integrated VCO (that is used as an LO) at each frequency, insertion loss of the HMC1044LP3E at the selected band setting, LO frequency, and the required modulator/demodulator LO input power. The harmonic attenuation and sideband rejection graphs in this section were generated by maintaining the minimum LO input power into the HMC697LP4E at ≥ -3 dBm across all frequencies, which falls well into the required LO input power specification in the HMC697LP4E data sheet of greater than -6 dBm and less than 6 dBm.

For applications that require a flat output power response, over a wide bandwidth, it should be noted that it is possible to build a low harmonic source with flat output power over a wideband using a leveling loop based upon the HMC830LP6GE wideband PLL with integrated VCO, the HMC1044LP3E variable LPF, and the HMC993LP5E AGC.

[3] Measured with HMC830LP6GE as an LO and HMC697LP4E modulator. The HMC830LP6GE was used in single-ended output configuration.

Serial Port Interface (SPI)

The HMC1044LP3E SPI has only write and no read capability. It features a three wire serial port for simple communication with the host controller. The HMC1044LP3E has a 3-bit chip address which is fixed as 6b.

Serial Port WRITE Operation

Main SPI Timing Characteristics

V3 = 3.3 V (3 V to 3.5 V), GND = 0V

Parameter	Conditions	Min	Typ	Max	Units
t_1	SDI to SCK Setup Time	8			nsec
t_2	SDI to SCK Hold Time	8			nsec
t_3	SCK High Duration	10			nsec
t_4	SCK Low Duration	10			nsec
t_5	SEN Low Duration	20			nsec
t_6	SEN High Duration	20			nsec
t_7	SCK to SEN [a]	8			nsec

a. SEN must rise after the 16th falling edge of SCK but before the next rising SCK edge. If SCK is shared amongst several devices this timing must be respected.

A typical write cycle is shown in *Figure 19*.

1. The Master asserts SEN (active low Serial Port Enable) followed by a rising edge of SCK.
2. The HMC1044LP3E reads SDI (the MSB) on the 1st rising edge of SCK after SEN active low.
3. The HMC1044LP3E registers the data bits in the next 8 rising edges of SCK (for a total of 9 data bits).
4. The host places 4 register address bits on the next 4 falling edges of SCK (MSB to LSB) while the HMC1044LP3E reads the address bits on the corresponding rising edge of SCK.
5. The host places 3 chip address bits on the next 3 falling edges of SCK (MSB to LSB). Note the HMC1044LP3E chip address is fixed as '6d' or '110'b.

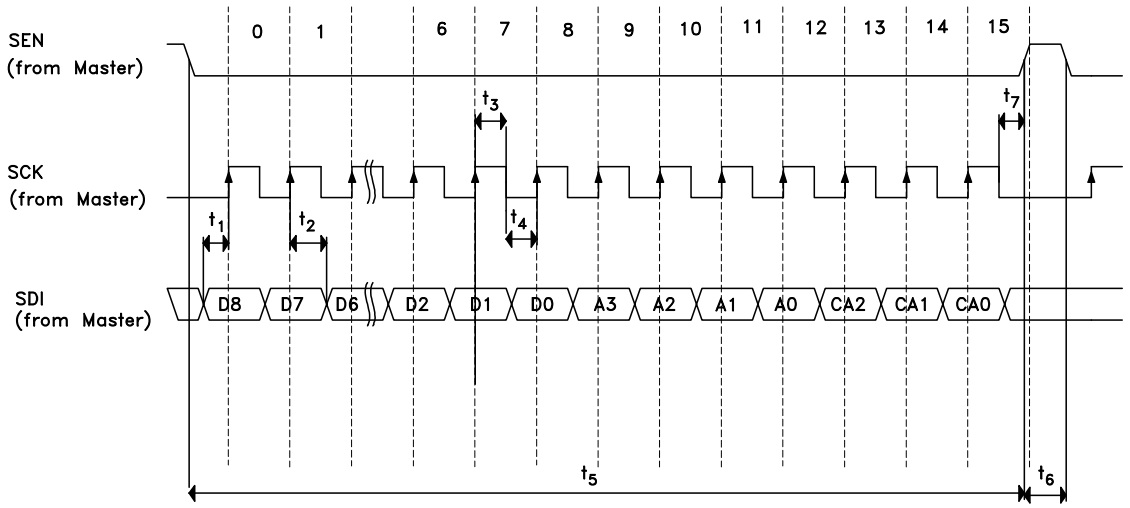


Figure 19. Serial port write timing diagram

PROGRAMMABLE HARMONIC LOW PASS FILTER 1 - 3 GHz 3 dB BANDWIDTH

Register Map

Reg 01h - Autotune

Bit	Name	Width	Default	Description
[15:0]	Autotune	4	15	Band setting 0 - lowest band 15 - highest band

PROGRAMMABLE HARMONIC LOW PASS FILTER 1 - 3 GHz 3 dB BANDWIDTH

NOTES: