SC1185 & SC1185A

Programmable Synchronous DC/DC Converter, Dual LDO Controller

Description

The SC1185 combines a synchronous voltage mode controller with two low-dropout linear regulators providing most of the circuitry necessary to implement three DC/DC converters for powering advanced microprocessors such as Pentium® II .

The SC1185 switching section features an integrated 5 bit D/A converter, pulse by pulse current limiting, integrated power good signaling, and logic compatible shutdown. The SC1185 switching section operates at a fixed frequency of 140kHz, providing an optimum compromise between size, efficiency and cost in the intended application areas. The integrated D/A converter provides programmability of output voltage from 2.0V to 3.5V in 100mV increments and 1.30V to 2.05V in 50mV increments with no external components.

The SC1185 linear sections are low dropout regulators supplying 1.5V for GTL bus and 2.5V for non-GTL I/O. The Reference voltage is made available for external linear regulators.

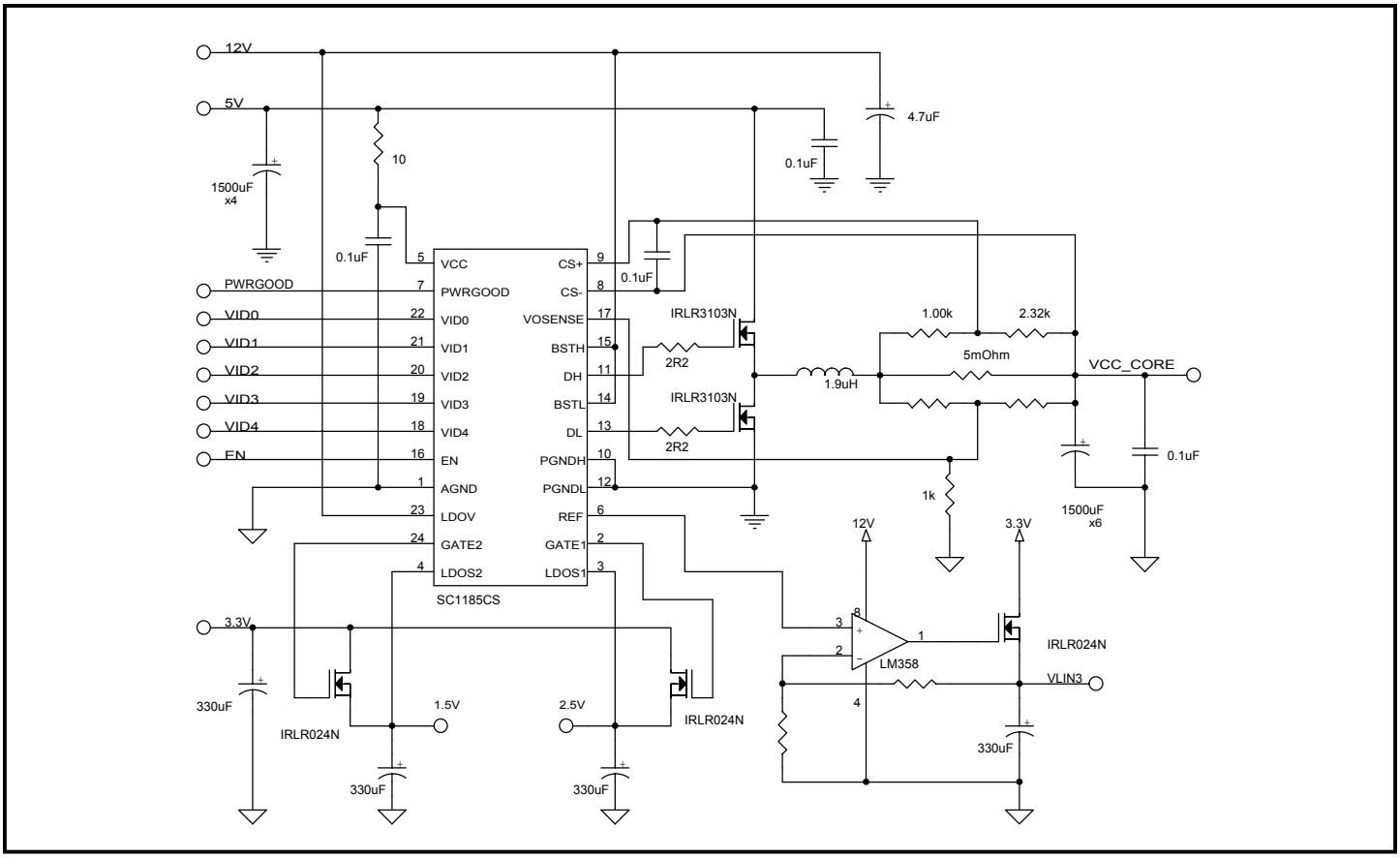
Features

- Synchronous design, enables no heatsink solution
- 95% efficiency (switching section)
- 5 bit DAC for output programmability
- On chip power good function
- Designed for Intel Pentium® II requirements
- 1.5V, 2.5V @ 1.25% for linear section
- 1.265V ± 1.5% Reference available
- 24-lead SO package. Lead free option available. Lead free product is fully WEEE and RoHS compliant.

Applications

- Pentium® II microprocessor supplies
- Flexible motherboards
- 1.3V to 3.5V microprocessor supplies
- Programmable triple power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
VCC to GND	V_{IN}	-0.3 to +7	V
PGND to GND		+1	V
BST to GND		-0.3 to +15	V
Operating Temperature Range	T_A	0 to +70	°C
Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_L	300	°C
Thermal Impedance Junction to Ambient	θ_{JA}	80	°C/W
Thermal Impedance Junction to Case	θ_{JC}	25	°C/W

Electrical Characteristics

Unless specified: V_{CC} = 4.75V to 5.25V; GND = P_{GND} = 0V; V_{OSENSE} = V_O; 0mV < (CS+-CS-) < 60mV; LDOV = 11.4V to 12.6V; T_A = 0 to 70°C

Parameter	Conditions	Min	Typ	Max	Units
Switching Section					
Output Voltage	I_O = 2A in Application Circuit	See Output Voltage Table			
Supply Voltage	VCC	4.5		7	V
Supply Current	VCC = 5.0V		8	15	mA
Load Regulation	I_O = 0.8A to 15A		1		%
Line Regulation			+0.15		%
Current Limit Voltage		60	70	85	mV
Oscillator Frequency		125	140	160	kHz
Oscillator Max Duty Cycle		90	95		%
Peak DH Sink/Source Current	BSTH - DH = 4.5V, DH - PGNDH = 3.1V DH - PGNDH = 1.5v	1 100			A mA
Peak DL Sink/Source Current	BSTL - DL = 4.5V, DL - PGNDL = 3.1V DL - PGNDL = 1.5V	1 100			A mA
Gain (A_{OL})	V_{OSENSE} to V_O		35		dB
VID Source Current	VIDx < 2.4V	1	10		µA
VID Leakage	VIDx < 2.4V			10	µA
Power good threshold voltage		88	100	112	%
Dead time		40	100		ns

Electrical Characteristics (Cont.)

Unless specified: V_{CC} = 4.75V to 5.25V; GND = P_{GND} = 0V; V_{OSENSE} = V_O; 0mV < (CS+-CS-) < 60mV; LDOV = 11.4V to 12.6V; T_A = 0 to 70°C

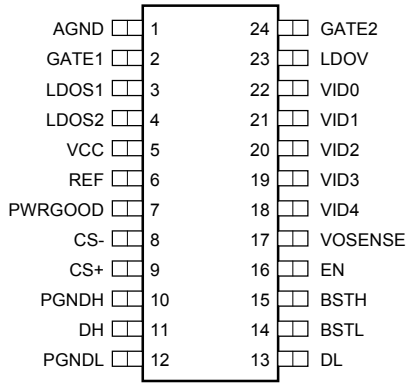
Parameter	Conditions	Min	Typ	Max	Units
Linear Sections					
Quiescent current	LDOV = 12V			5	mA
Output Voltage LDO1		2.469	2.500	2.531	V
Output Voltage LDO2		1.481	1.500	1.519	V
Reference Voltage	Iref < 100µA	1.246	1.265	1.284	V
Gain (A_{OL})	LDOS (1, 2) to GATE (1, 2)		90		dB
Load Regulation	I_O = 0 to 8A			0.3	%
Line Regulation				0.3	%
Output Impedance	VGATE = 6.5V		1	1.5	Ω
Gate Pulldown Impedance	GATE (1,2)-AGND; VCC=LDOV=OV	80	300	750	kΩ
VOSENSE Impedance		10			kΩ

NOTE:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

POWER MANAGEMENT

Pin Configuration

TOP VIEW



(24 Pin SOIC)

Ordering Information

Part Number	Package (1)	Linear Voltage	Temp Range (T_J)
SC1185CSW.TR	SO-24	1.5V2.5V	0° to 125°C
SC1185CSW.TRT(3)			
SC1185ACSW.TR	SO-24	1.5V2.5V	0° to 125°C
SC1185ACSW.TRT(3)			

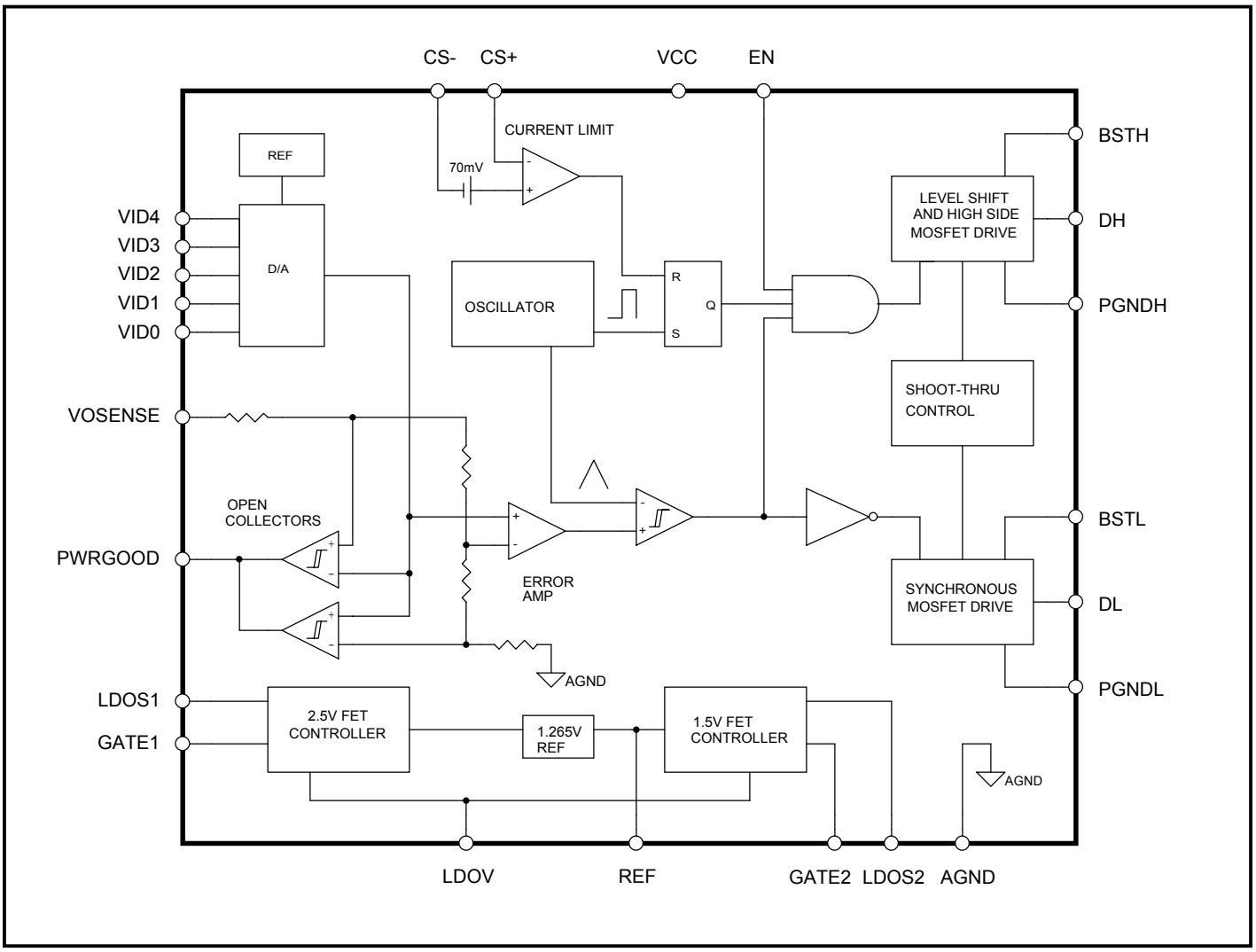
Notes:
(1) Only available in tape and reel packaging. A reel contains 1000 devices.
(2) SC1185A provides improved output tolerance. See Output Voltage Table.
(3). Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	AGND	Small Signal Analog and Digital Ground
2	GATE1	Gate Drive Output LDO1
3	LDOS1	Sense Input for LDO1
4	LSOS2	Sense Input for LDO2
5	VCC	Input Voltage
6	REF	Buffered Reference Voltge output
7	PWRGOOD(1)	Open collector logic output, high if V_O within 10% of setpoint
8	CS-	Current Sense Input (negative)
9	CS+	Current Sense Input (positive)
10	PGNDH	Power Ground for High Side Switch
11	DH	High Side Driver Output
12	PGNDL	Power Ground for Low Side Swtch
13	DL	Low side Driver Output
14	BSTL	Supply for Low Side Driver
15	BSTH	Supply for High Side Driver
16	EN (1)	Logic low shuts down the converter. High or open for normal operation.
17	VOSENSE	Top end of internal feedback chain
18	VID4 (1)	Programming Input (MSB)
19	VID3 (1)	Programming Input
20	VID2 (1)	Programming Input
21	VID1 (1)	Programming Input
22	VID0 (1)	Programming Input (LSB)
23	LDOV	+12V for LDO section
24	GATE2	Gate Drive Output LDO2

Note:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Output Voltage Table

Unless specified: 4.75V < VCC < 5.25V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+-CS-) < 60mV; = 0°C < T_j < 85°C

Parameter		Standard			"A" Version			
	Vid 43210	Min	Typ	Max	Min	Typ	Max	Units
Output Voltage	01111	1.277	1.300	1.323	1.287	1.300	1.313	V
	01110	1.326	1.350	1.374	1.337	1.350	1.364	
	01101	1.375	1.400	1.425	1.386	1.400	1.414	
	01100	1.424	1.450	1.476	1.436	1.450	1.465	
	01011	1.478	1.500	1.523	1.485	1.500	1.515	
	01010	1.527	1.550	1.573	1.535	1.550	1.566	
	01001	1.576	1.600	1.624	1.584	1.600	1.616	
	01000	1.625	1.650	1.675	1.634	1.650	1.667	
	00111	1.675	1.700	1.726	1.683	1.700	1.717	
	00110	1.724	1.750	1.818	1.733	1.750	1.768	
	00101	1.782	1.800	1.869	1.782	1.800	1.818	
	00100	1.832	1.850	1.919	1.832	1.850	1.869	
	00011	1.881	1.900	1.970	1.881	1.900	1.919	
	00010	1.931	1.950	2.020	1.931	1.950	1.970	
	00001	1.980	2.000	2.020	1.980	2.000	2.020	
	00000	2.030	2.050	2.071	2.030	2.050	2.071	
	11111	1.970	2.000	2.030	1.970	2.000	2.030	
	11110	2.069	2.100	2.132	2.069	2.100	2.132	
	11101	2.167	2.200	2.233	2.167	2.200	2.233	
	11100	2.266	2.300	2.335	2.266	2.300	2.335	
	11011	2.364	2.400	2.436	2.364	2.400	2.436	
	11010	2.463	2.500	2.538	2.463	2.500	2.538	
	11001	2.561	2.600	2.639	2.561	2.600	2.639	
	11000	2.660	2.700	2.741	2.660	2.700	2.741	
	10111	2.758	2.800	2.842	2.758	2.800	2.842	
	10110	2.842	2.900	58	2.842	2.900	2.958	
	10101	2.940	3.000	3.060	2.940	3.000	3.060	
	10100	3.038	3.100	3.162	3.038	3.100	3.162	
	10011	3.136	3.200	3.264	3.136	3.200	3.264	
	10010	3.234	3.300	3.366	3.234	3.300	3.366	
	10001	3.332	3.400	3.468	3.332	3.400	3.468	
	10000	3.430	3.500	3.570	3.430	3.500	3.570	

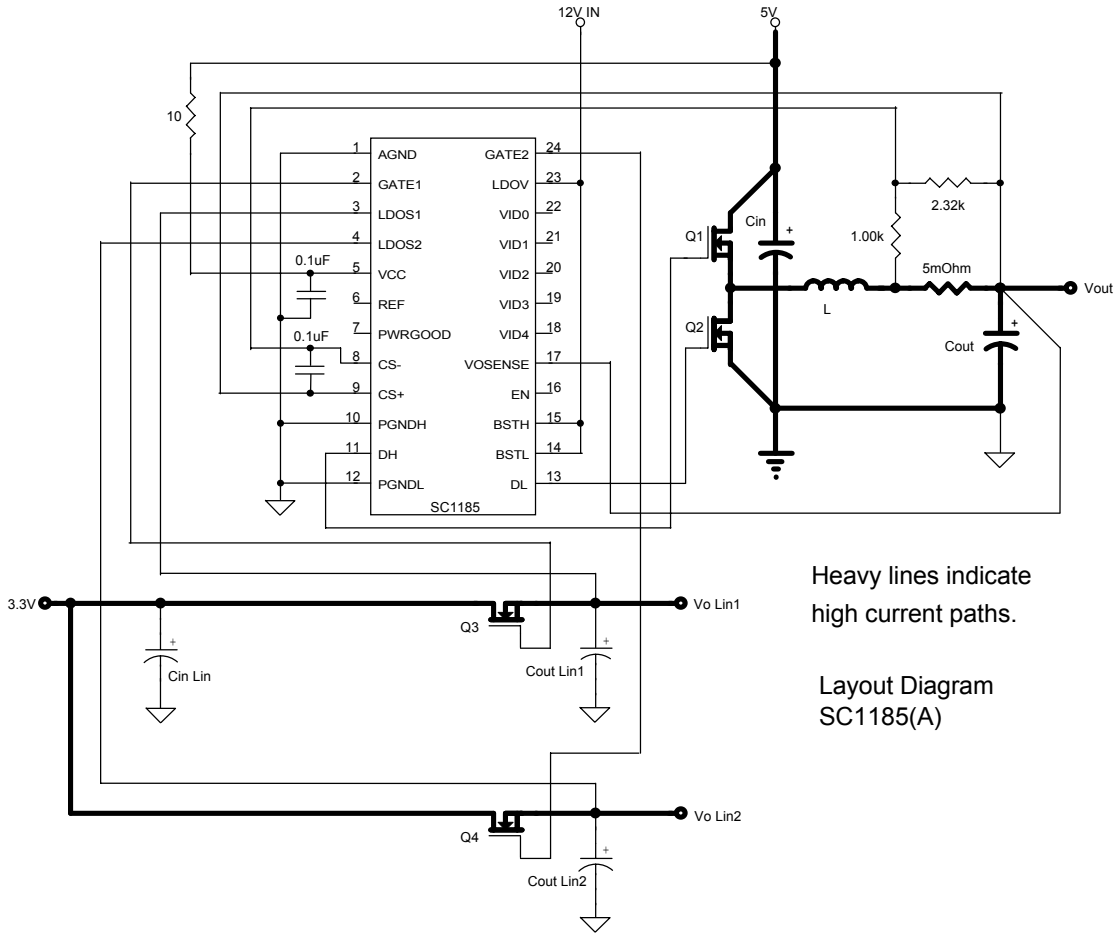
Layout Guidelines

Careful attention to layout requirements are necessary for successful implementation of the SC1185 PWM controller. High currents switching at 140kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.



Layout Guidelines

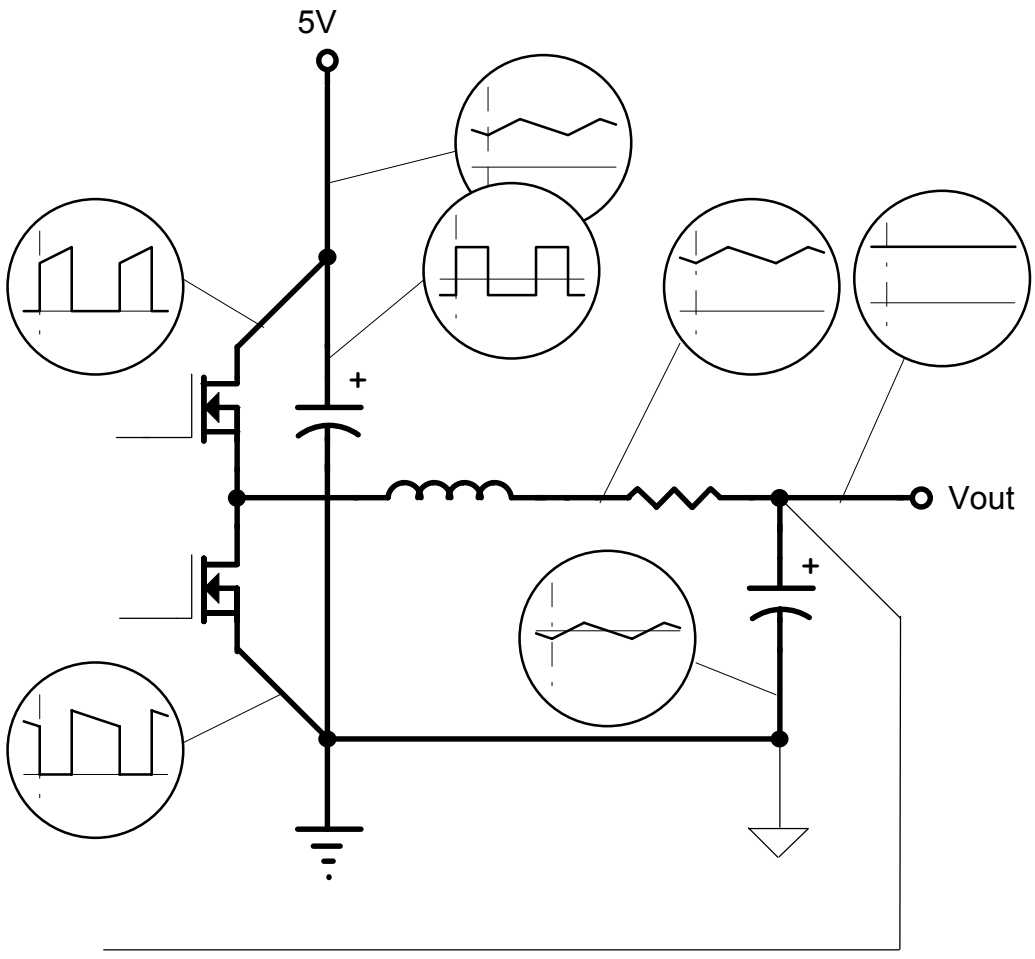
4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1185 is best placed over a quiet ground plane area, avoid pulse currents in the Cin, Q1, Q2 loop flowing in this area. PGNDH and PGNDL should be returned to the ground plane close to the package. The AGND pin should be connected to the ground side of (one of) the output capacitor(s). If this is not possible, the AGND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should AGND be returned to a ground inside the Cin, Q1, Q2 loop.

6) Vcc for the SC1185 should be supplied from the 5V supply through a 10Ω resistor, the Vcc pin should be decoupled directly to AGND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS+ and CS- on the SC1185 should run parallel and close to each other. The 0.1µF capacitor should be mounted as close to the CS+ and CS- pins as possible.

8) Ideally, the grounds for the two LDO sections should be returned to the ground side of (one of) the output capacitor(s).



Currents in various parts of the power section

Layout Guidelines

COMPONENT SELECTION

SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \le \frac{V_t}{I_t}$$

Where

V_t = Maximum transient voltage excursion

I_t = Transient current step

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Cap.		Qty. Rqd.	Total	
	C (µF)	ESR (mΩ)		C (µF)	ESR (mΩ)
Low ESR Tantalum	330	60	6	2000	10
OS-CON	330	25	3	990	8.3
Low ESR Aluminum	1500	44	5	7500	8.3

The choice of which to use is simply a cost/performance issue, with Low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above.

The maximum inductor value may be calculated from:

$$L \le \frac{R_{ESR}\, C}{I_t} \cdot V_A$$

where V_A is the lesser of V_O or $(V_{IN} - V_O)$

The calculated maximum inductor value assumes 100% and 0% duty cycle, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions.

We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L_{RIPPLE}} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot \delta$$

where

$$\delta = \text{duty cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, if we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot 10^{-2}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{4}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

To a first order approximation, it is convenient to only con-

sider conduction losses to determine FET suitability. For a 5V in; 2.8V out at 14.2A requirement, typical FET losses would be: Using 1.5X Room temp $R_{DS(ON)}$ to allow for temperature rise.

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
IRL34025	15	1.69	D^2Pak
IRL2203	10.5	1.19	D^2Pak
Si4410	20	2.26	S0-8

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it, resulting in low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1-\delta)$$

For the example above:

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
IRL34025	15	1.33	D^2Pak
IRL2203	10.5	0.93	D^2Pak
Si4410	20	1.77	S0-8

Each of the package types has a characteristic thermal impedance, for the TO-220 package, thermal impedance is mostly determined by the heatsink used. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D^2PAK and 80°C/W for the SO-8 are readily achievable. The corresponding temperature rise is detailed below:

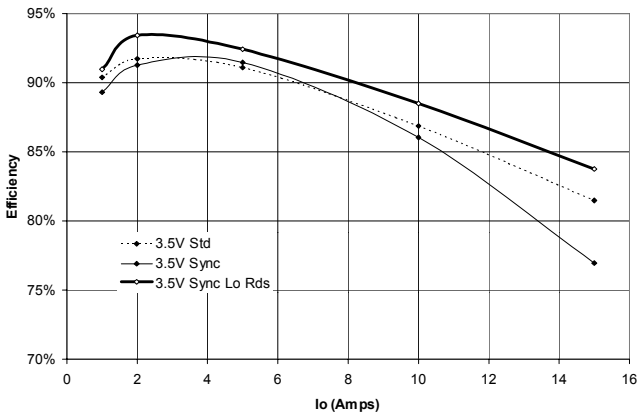
	Temperature rise (°C)	
FET type	Top FET	Bottom FET
IRL34025	67.6	53.2
IRL2203	47.6	37.2
Si4410	180.8	141.6

It is apparent that single SO-8 Si4410 are not adequate for this application, but by using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

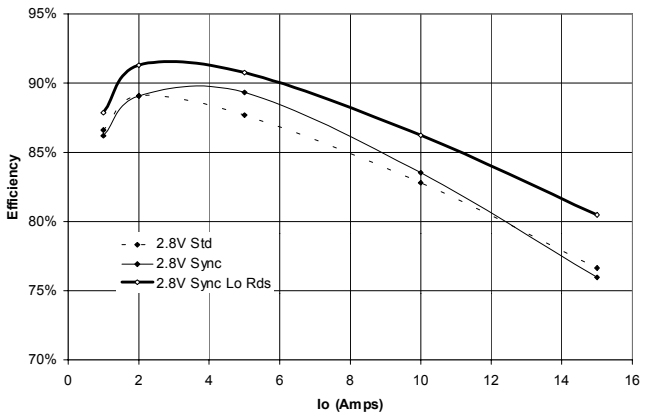
INPUT CAPACITORS - since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

Typical Characteristics

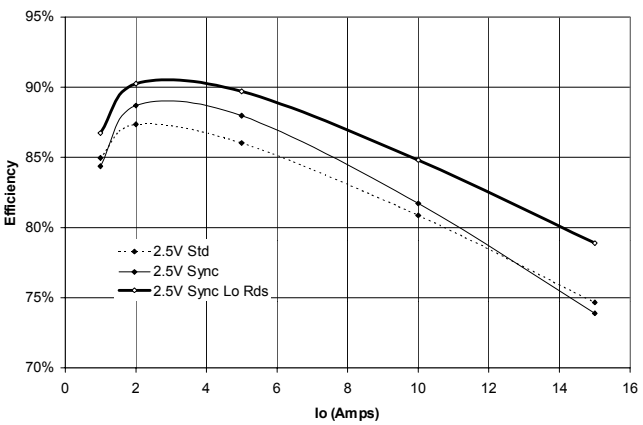
Typical Efficiency at Vo=3.5V



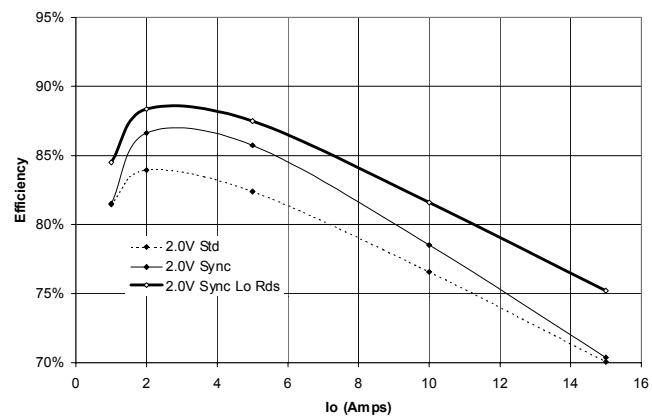
Typical Efficiency at Vo=2.8V



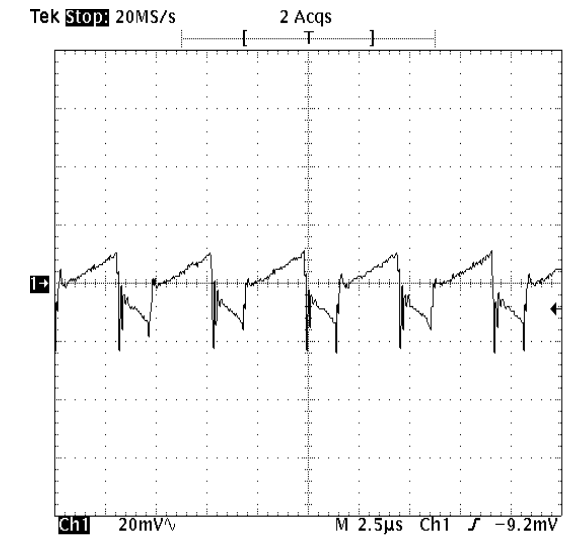
Typical Efficiency at Vo=2.5V



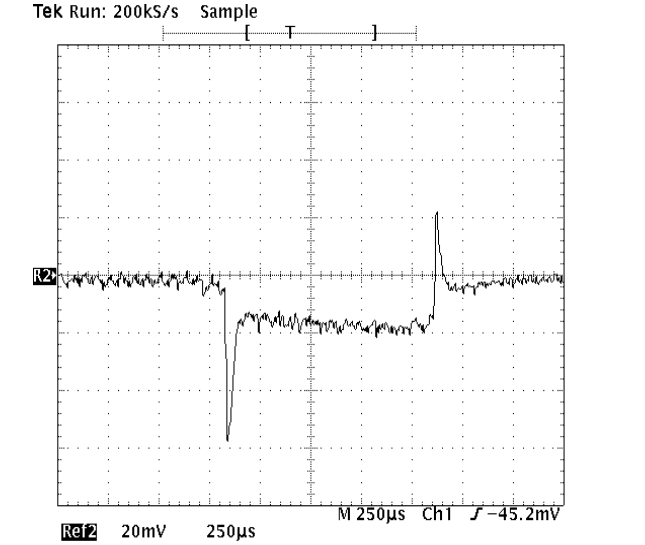
Typical Efficiency at Vo=2.0V



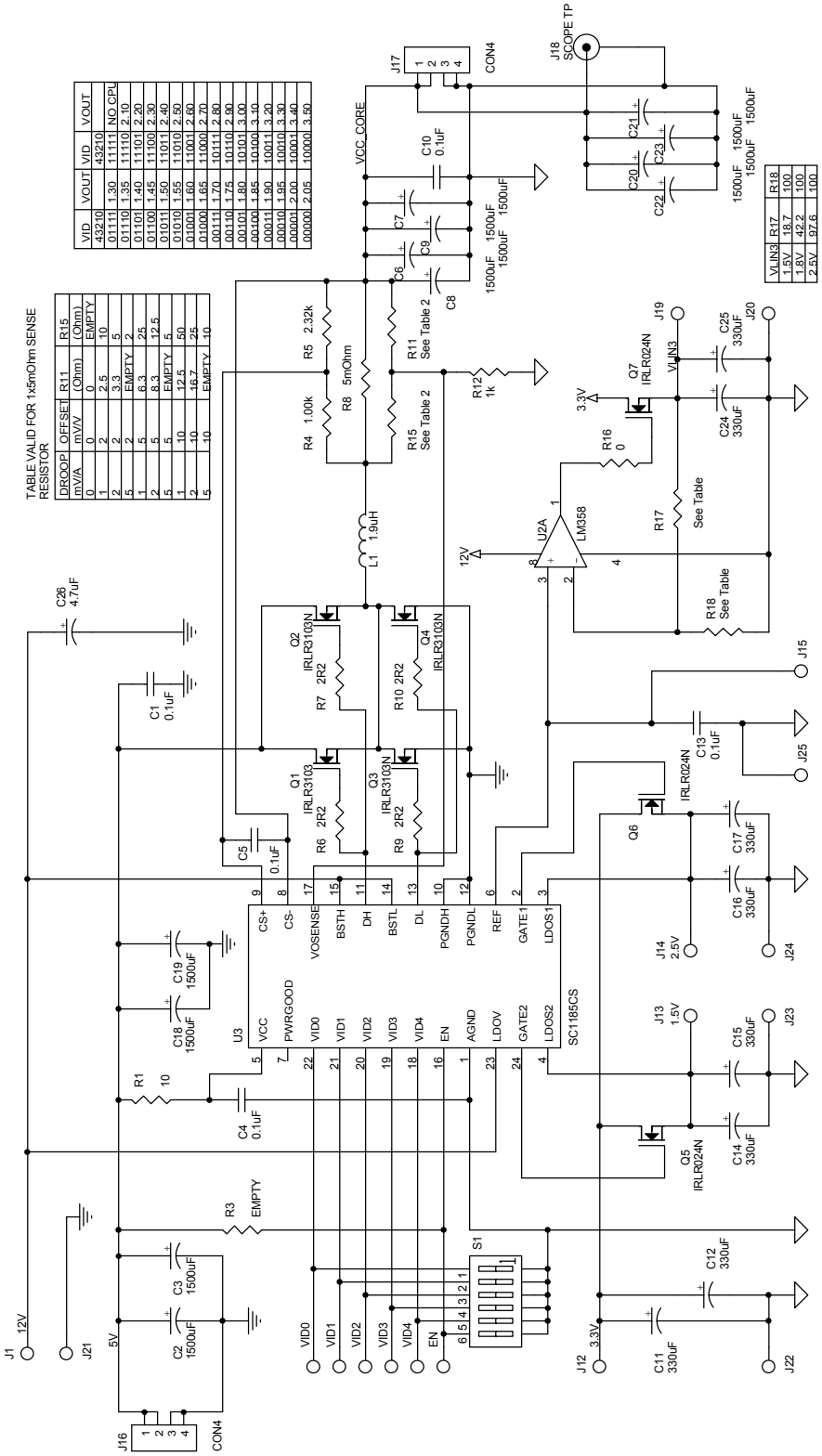
Typical Ripple, Vo=2.8V, Io=10A



Transient Response Vo=2.8V, Io=300mA to 10A



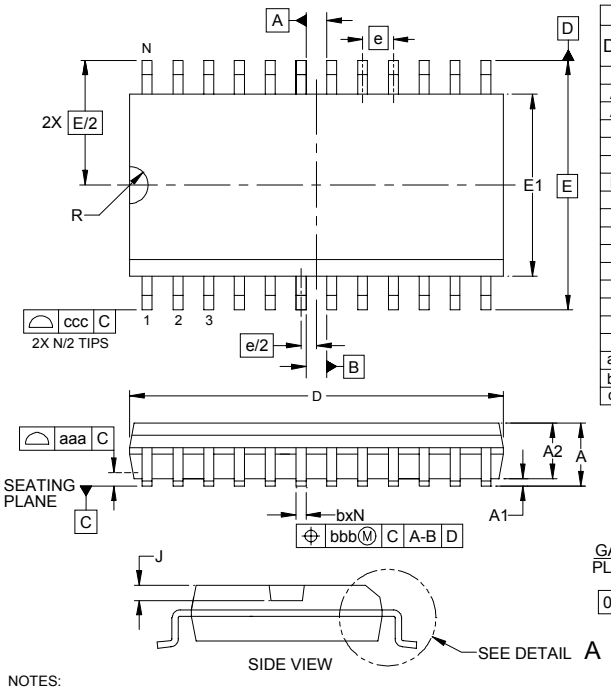
Typical Application Circuit



Materials List

Item	Qty.	Reference	Value	Notes
1	5	C1, C4, C5, C10, C13	0.1uF Ceramic	
2	12	C2, C3, C6, C7, C8, C9, C18, C19, C20, C21, C22, C23	1500uF	Sanyo MV-GX or equiv. Low ESR
3	8	C11, C12, C14, C15, C16, C17, C24, C25	330uF	
4	1	C26	4.7uF	
5	1	L1	1.9uH	6 Turns 16AWG on MICROMETALS T50-52D core
6	4	Q1, Q2, Q3, Q4	IRLR3103N	
7	3	Q5, Q6, Q7	IRLR024N	
8	1	R1	10	
9	1	R3	EMPTY	
10	1	R4	1.00k	
11	1	R5	2.32k	
12	4	R6, R7, R9, R10	2R2	
13	1	R8	5mOhm	IRC OAR-1 Series
14	2	R15, R11	See Table	
15	1	R12	1k	
16	1	R16	0	
17	2	R17, R18	See Table	
18	1	U2	LM358	
19	1	U3	SC1185CS	SEMTECH

Outline Drawing - SO - 24

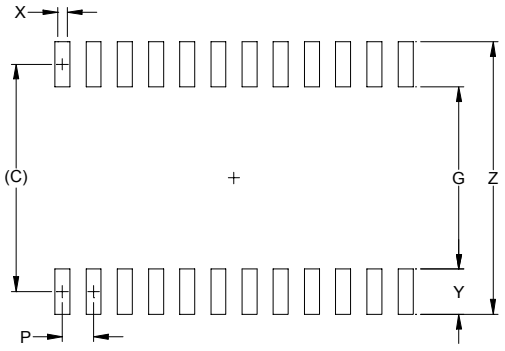


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.093	-	.104	2.35	-	2.65
A1	.004	-	.012	0.10	-	0.30
A2	.081	-	.100	2.05	-	2.55
b	.012	-	.020	0.31	-	0.51
c	.008	-	.013	0.20	-	0.33
D	.602	.606	.610	15.30	15.40	15.50
E1	.291	.295	.299	7.40	7.50	7.60
E	.406 BSC			10.30 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.030	0.25	-	0.75
J	.020	-	.030	0.50	-	0.75
L	.016	-	.041	0.40	-	1.04
L1	(.041)			(1.04)		
N	24			24		
R	.024	-	.035	0.60	-	0.90
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.013			0.33		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-013, VARIATION AD.

Land Pattern - SO - 24



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.362)	(9.20)
G	.276	7.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.449	11.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 307A.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012-8790
Phone: (805)498-2111 FAX (805)498-3804