TC8521AP, TC8521AM

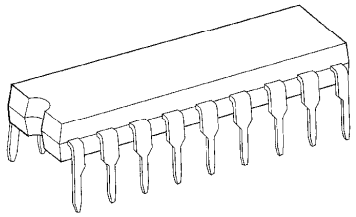
(Real Time Clock II)

1. GENERAL DESCRIPTION

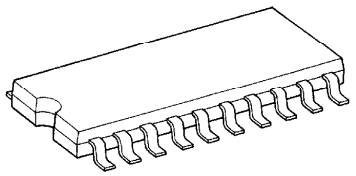
The TC8521AP/AM is an 1-chip C-MOS LSI to be used for the real time clock fabricated as the peripheral IC of the microcomputer.

The TC8521AP/AM has the crystal oscillation circuit of 32768Hz, the counter for clock and calendar, the alarm function, and the 26×4-bit RAM.

Since the package is of 18-pin DIP, 20-pin SOP and the battery back-up is possible, the time counting system provided with the non-volatile RAM can be fabricated with the crystal and the battery.



DIP18-P-300-2.54A



SIO20-P-300-1.27

PIN NO.	I/O	PIN NAME
1 (1)	I	-CS
2 (2)	I	CS
3 (3)	I	ADJUST
4 (4)	I	A0
5 (5)	I	A1
6 (6)	I	A2
7		NC
8 (7)	I	A3
9 (8)	I	-RD
10 (9)	G	GND
11 (10)	I	-WR
12 (11)	IO	D0
13 (12)	IO	D1
14 (13)	IO	D2
15 (14)	IO	D3
16 (15)	O	-ALARM
17		NC
18 (16)	I	XIN
19 (17)	O	XOUT
20 (18)	V	VCC

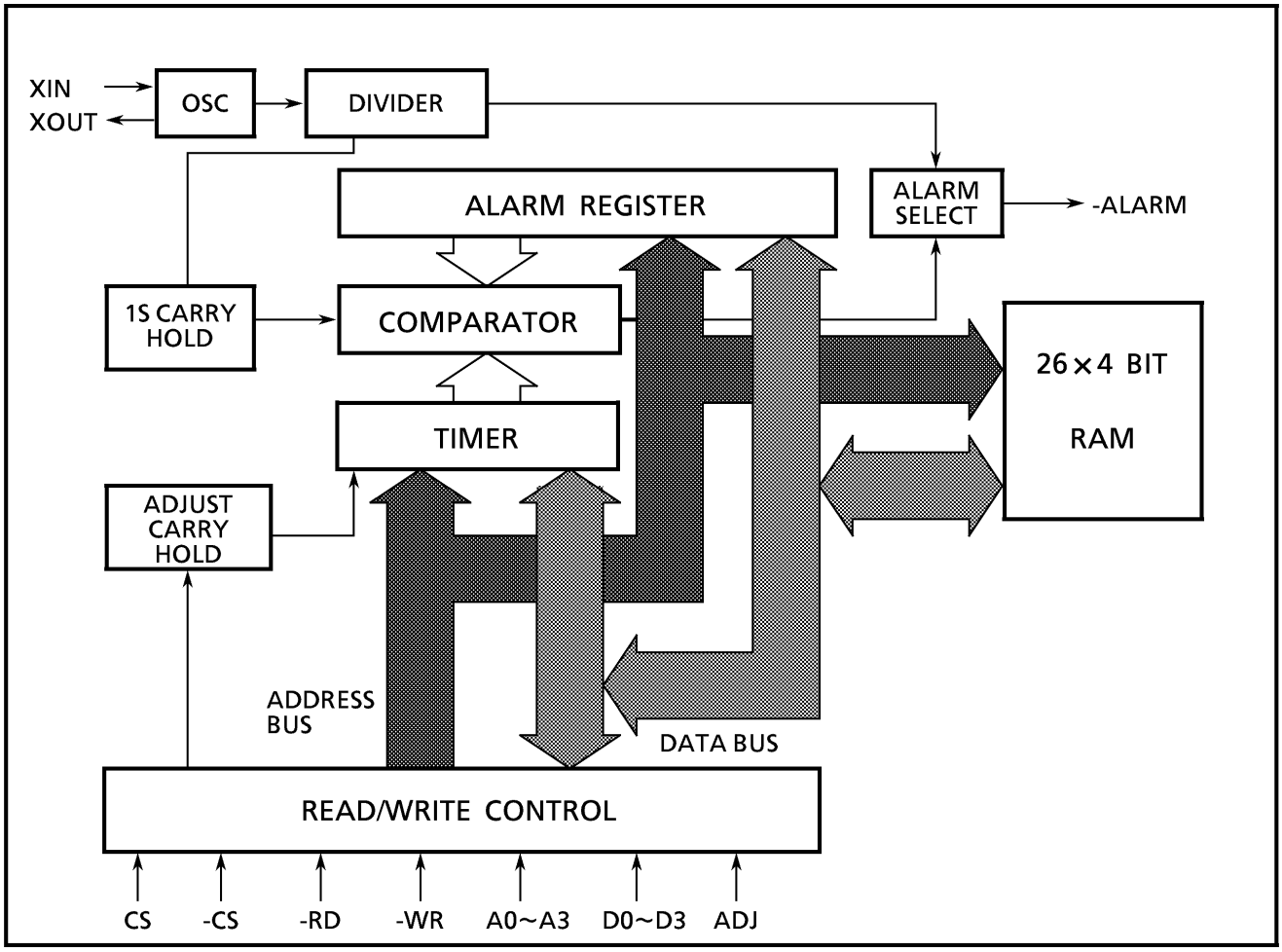
note) (1)~(18) are PIN number of DIP.

2. FEATURES

- ☐ Low power dissipation realized by Si-gate CMOS technology
- ☐ Clock function (hr, min, sec, date, day of week, year and leap year) Auto-calendar
- ☐ Clock system of 24-hour or 12-hour (AM/PM) is selectable.
- ☐ ±30-sec correction function, Alarm signal, or pulse of 16Hz or 1Hz can be output.
- ☐ Built-in 26×4-bit RAM
- ☐ Directly connectable with CPU bus.
- ☐ 4-bit bidirectional data bus
- ☐ 4-bit address input
- ☐ Capable of battery backup

3. TC8521AP/AM and APPLICATION SYSTEM

3.1 INTERNAL BLOCK DIAGRAM



The comparator compares the contents of the timer and the alarm register to output the coincident signal. The signal ORed with the output of the comparator and 16Hz or 1Hz signal which is generated from the divider is output to the alarm terminal through the ALARM SELECT circuit. Each of these three signals can select the output ENABLE or the output DISABLE independently. The 1S CARRY HOLD circuit holds one second carry signal generated from the divider during the TIMER DISABLE for one time, and output it to the TIMER after the TIMER ENABLE state is selected. The ADJUST CARRY HOLD circuit also holds the carry signal made by the ADJUST.

3.2 SYSTEM CONFIGURATION

The RTC can be backed up by the battery.

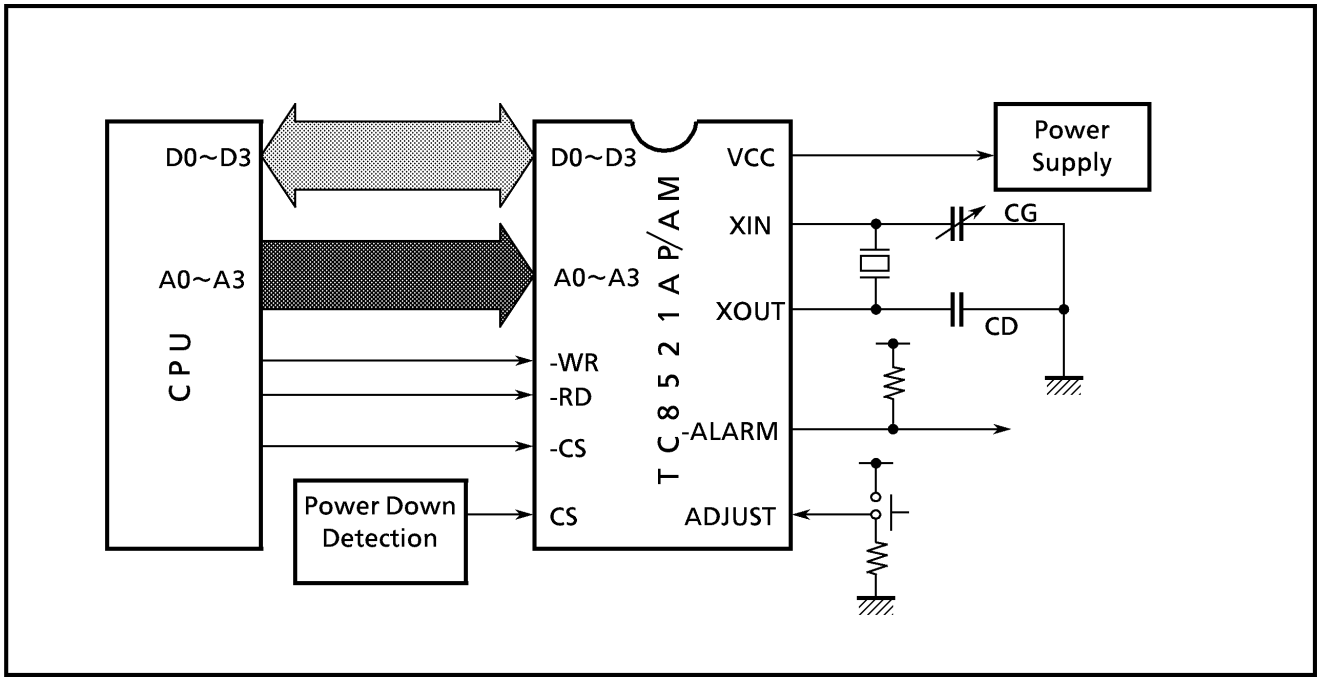


FIG.3.2 SYSTEM CONFIGURATION

Even if the input terminal to be interfaced with the CPU and the data bus come into the state of floating, this IC does not operate abnormally when the input is set to "0" (Low level).

* Output stabling resistance (about 250kΩ) is built in oscillation circuit.
* CG = 10pF to 30pF
* CD = 10pF to 30pF

4. PIN DESCRIPTION

note) (1)~(18) are PIN number of DIP.

NO.	PIN NAME	I/O	FUNCTION
1 (1)	-CS	I	When -CS is "0" and CS is "1", RTC is selected making read and write operations possible.
2 (2)	CS	I	-CS is connected to CPU to be used. CS is connected to POWER DOWN DETECTION CIRCUIT of peripheral circuit power supply to be used.
3 (3)	ADJUST	I	Second adjustment is made by this signal. Set this signal at "High" level when second indication is 0 to 29, and the indication becomes 0. When the second indication is 30 to 59, the minute indication is carried up and the second indication is made 0.
4 (4)	A0	I	Address input for selecting RTC register. Connected to address bus of CPU side.
5 (5)	A1	I	
6 (6)	A2	I	
8 (7)	A3	I	
9 (8)	-RD	I	Set this terminal at "0" during the state the chip is selected, and CPU can read the contents of RTC register.
10 (9)	GND	G	Ground of IC. Connected to ground of system.
11 (10)	-WR	I	Set this terminal at "0" during the chip is selected, and CPU can write data into RTC register.
12 (11)	D0	I/O	Bidirectional data bus (4 bits) for exchanging the data to and from CPU side.
13 (12)	D1	I/O	
14 (13)	D2	I/O	
15 (14)	D3	I/O	
16 (15)	-ALARM	O	Alarm signal and clock pulse of 16Hz and 1Hz are output. Open drain output.
18 (16)	XIN	I	Crystal oscillator connecting terminal.
19 (17)	XOUT	O	
20 (18)	VDD	V	+ 5V of IC plus power supply is supplied.

5. FUNCTIONAL SPECIFICATION

5.1 FUNCTIONAL DESCRIPTION

5.1.1 DESCRIPTION of ADDRESS

PAGE 0 (TIMER)

ADDRESS CONTENTS				16 HEXA-DECIMAL	DATA BUS CONTENTS				REMARKS
A3	A2	A1	A0		D3	D2	D1	D0	
0	0	0	0	0	8 secs	4 secs	2 secs	1 sec	1-sec digit
0	0	0	1	1	– (*1)	40 secs	20 secs	10 secs	10-sec digit
0	0	1	0	2	8 mins	4 mins	2 mins	1 min	1-min digit
0	0	1	1	3	–	40 mins	20 mins	10 mins	10-min digit
0	1	0	0	4	8 hrs	4 hrs	2 hrs	1 hr	1-hr digit
0	1	0	1	5	–	–	20 hrs (PM/AM)	10 hrs	10-hr digit
0	1	1	0	6	–	W2	W1	W0	Week digit (*2)
0	1	1	1	7	8 days	4 days	2 days	1 day	1-day digit
1	0	0	0	8	–	–	20 days	10 days	10-day digit
1	0	0	1	9	8 months	4 months	2 months	1 month	1-month digit
1	0	1	0	A	–	–	–	10 months	10-month digit
1	0	1	1	B	8 years	4 years	2 years	1 year	1-year digit
1	1	0	0	C	80 years	40 years	20 years	10 years	10-year digit
1	1	0	1	D	TIMER ENABLE	ALARM ENABLE	PA1	PA0	PAGE register (*3)
1	1	1	0	E	TEST 3	TEST 2	TEST 1	TEST 0	TEST register (*4)
1	1	1	1	F	1Hz ENABLE	16Hz ENABLE	TIMER RESET	ALARM RESET	RESET register (*5)

PAGE 1 (ALARM)

ADDRESS CONTENTS				16 HEXA-DECIMAL	DATA BUS CONTENTS				REMARKS
A3	A2	A1	A0		D3	D2	D1	D0	
0	0	0	0	0	–	–	–	– (*1)	
0	0	0	1	1	–	–	–	–	
0	0	1	0	2	8 mins	4 mins	2 mins	1 min	ALARM 1-min digit
0	0	1	1	3	–	40 mins	20 mins	10 mins	ALARM 10-min digit
0	1	0	0	4	8 hrs	4 hrs	2 hrs	1 hr	ALARM 10-hr digit
0	1	0	1	5	–	–	20 hrs (PM/AM)	10 hrs	ALARM 10-hr digit
0	1	1	0	6	–	W2	W1	W0	ALARM week digit (*2)
0	1	1	1	7	8 days	4 days	2 days	1 day	ALARM 1-day digit
1	0	0	0	8	–	–	20 days	10 days	ALARM 10-day digit
1	0	0	1	9	–	–	–	–	
1	0	1	0	A	–	–	–	24/12	24-hr select bit (*6)
1	0	1	1	B			U1	U0	Leap year digit (*7)
1	1	0	0	C	–	–	–	–	
1	1	0	1	D	TIMER ENABLE	ALARM ENABLE	PA1	PA0	PAGE register (*3)
1	1	1	0	E	TEST 3	TEST 2	TEST 1	TEST 0	TEST register (*4)
1	1	1	1	F	1Hz ENABLE	16Hz ENABLE	TIMER RESET	ALARM RESET	RESET register (*5)

PAGE 3, 4 (RAM)

PAGE address 10 and 11 are RAMs of 13×4 bits

Notes :

- □ Address 0_{16} to D_{16} Read and write are enabled.
- □ Address E_{16} to F_{16} Only write is enabled.
- □ Address D_{16} to F_{16} Unrelated to MODE.

(*1) "—" is neglected at writing and turned into "0" at reading.

(*2) Day of week is a numeral from 0 to 6.

(*3) PAGE register

TIMER ENABLE Timer starts at "1", and stops counting the time follows second at"0"

ALARM ENABLE ALARM ENABLE at "1". Signals of 16Hz and 1Hz are output even at "0" without any relation to ENABLE and DISABLE states of alarm.

PA1 or PA0 bit of PAGE register is selected as shown in the table below.

PA1	PA0		FUNCTION
0	0	PAGE 0	Setting and reading of time.
0	1	PAGE 1	Setting and reading of ALARM, 12-hr/24-hr and leap year.
1	0	PAGE 2	Writing and reading of RAM.
1	1	PAGE 3	Writing and reading of RAM.

(*4) TEST register

Since this is the register for high-speed test at shipping, set all the contents of the register at "0". As no normal operation can be expected when the data other than "0" is input, care must be taken.

(*5) RESET register

D0 = "1" Alarm register is reset.
D1 = "1" Timer is reset
D2 = "0" 16Hz clock is output to ALARM.
D3 = "0" 1Hz clock is output to ALARM.

(*6) 24 hour select bit

When D0 = "1", 24-hr system, and when D0 = "0", 12-hr system is selected.
In 12 hour, when D1 of 10-hr digit = "1", PM, and when D1 = "0", AM is selected

(*7) Leap year digit

When both U1 and U0 are "0", leap year is selected. The year carry is made simultaneously with that of 1-year digit to this leap year digit U1, U0.

At setting, caution must be exercised for inputting the correct years elapsed after the leap year. If this year is the year after the "leap year", input U1 = "0" and U0 = "1", and if this year is the year two years after the "leap year", input U1 = "1" and U0 = "0". At the time three years after the "leap year", input "1" both to U1 and U0.

This is used to facilitate the setting of a leap year, using the fact that in general, a leap year occurs once every four years. However, note that a leap year is not necessarily once every four years. The year 2000 is a leap year but the years 1900 and 2100 are not. Thus, if the user sets the incorrect data in the leap year digit, operation is not guaranteed.

(*8) Year 2000

This product only has lower two digits to set the year. Therefore, the year after the year 99 is the year 00. In the user system where the product is used, the user must control the digits for hundred years and thousand years.

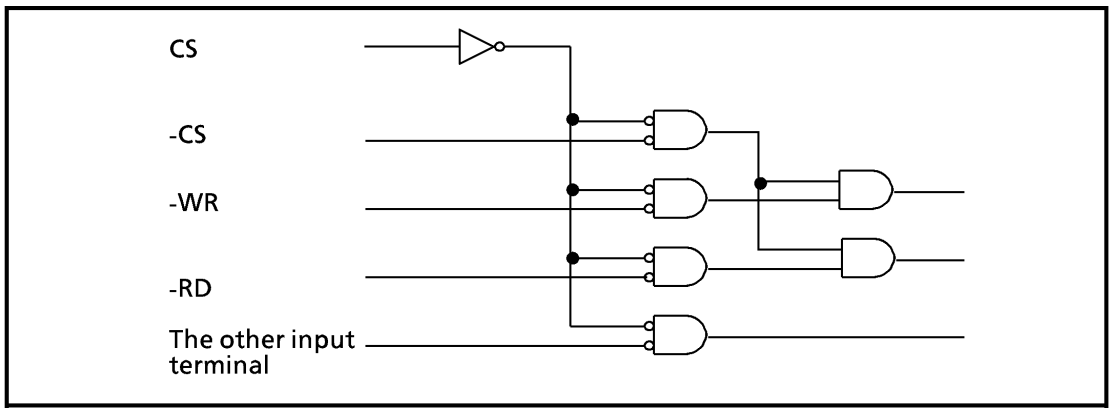
If the user system uses four-digit years, take care during changeover from the year 99 to 00 that the system does not revert to the previous century; for example, from 1999 to 1900 instead of 2000.

5.2 APPLICATION METHOD

5.2.1 DESCRIPTION of CS and -CS

When the terminals of CS and -CS are respectively "1" and "0", the following circumstances are turned out.

* -WR and -RD signals from outside become ENABLE.
* If the CS terminal is at "0". All the inputs become disabled, and even if the input terminal is in the floating state, the through current does not flow. However, the input voltage of the CS terminal is required to be at VCC level or GND level.
* The output of the power-down detection circuit is usually connected to the CS terminal. By means of connecting this circuit, the CS terminal is fixed at low level, the erroneous operation of the RTC is prevented and the data is maintained undestroyed.

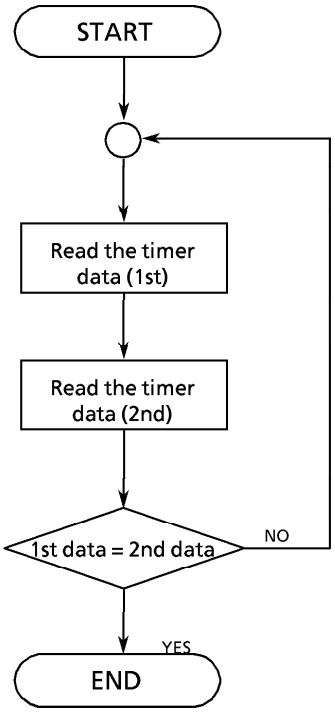


5.2.2 READING of DATA

Caution must be exercised because the erroneous data is possibly be read if the carry signal is input during the series of reading operations. The data is correctly read through the procedures below.

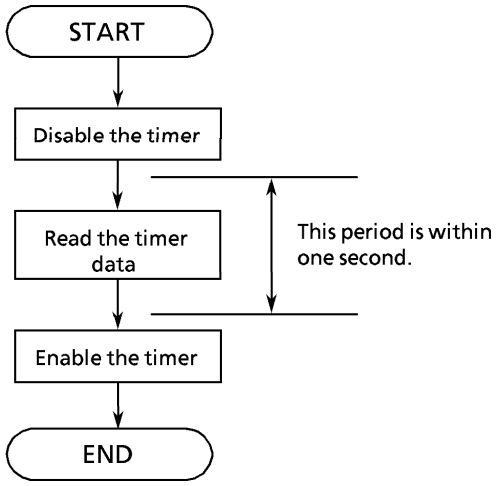
1. READ TWICE

Read the timer data twice and compare the contents to confirm the carry. If the contents are found different to each other during the data comparison, read the data twice again because this means that the carry has been made.



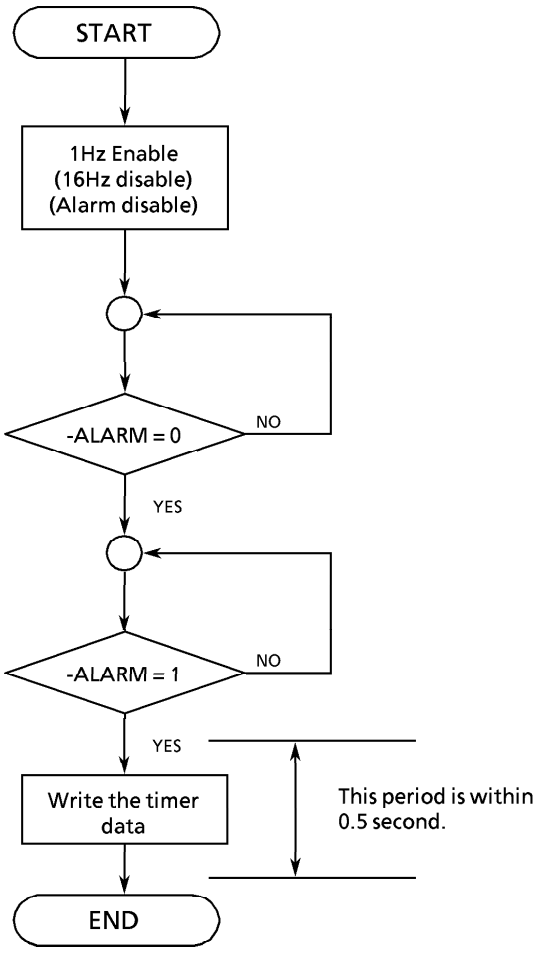
2. DISABLE THE TIMER

When "0" is written to D3 of the address "D", the timer is made DISABLE, the carry is inhibited and the erroneous operation can be prevented by the CLOCK HOLD circuit. The CLOCK HOLD circuit holds one second carry from the divider preceding to second counter during the DISABLE state, and the held carry will regenerate after the timer is made ENABLE so as to adjust the time. However, when the ENABLE state of the timer continues over one second, the timer becomes delayed. At this time, care must be taken because the system power supply sometimes goes down during the DISABLE state of the timer (the timer is left stopped and the time indication begins to lose). Therefore, when the power-down is detected during the timer DISABLE state, it is necessary to set CS to "0" after restoring the timer ENABLE state.



3. USE 1HZ OUTPUT OF ALARM

Use 1Hz signal which is output from the ALARM terminal to read the data at its leading edge.

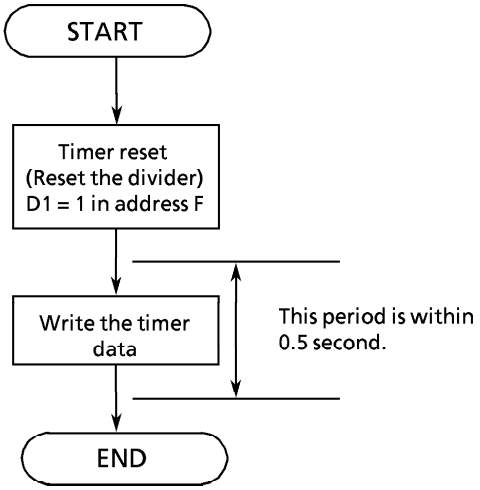


5.2.3 WRITING of DATA

The expected data can not be written if the carry signal is input during the series of writing operations. The data is correctly written through the procedures below.

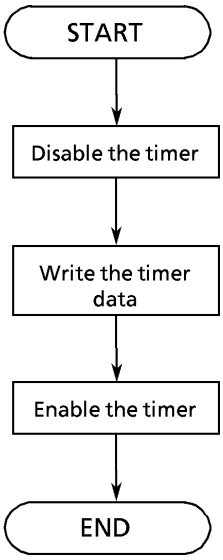
1. RESET THE DIVIDER

The 15-stage divider for generating 1Hz signal from 32.768KHz is built in the RTC. When this divider is reset, the timer carry is not coming out for a second and during which time, the data can be written safely.



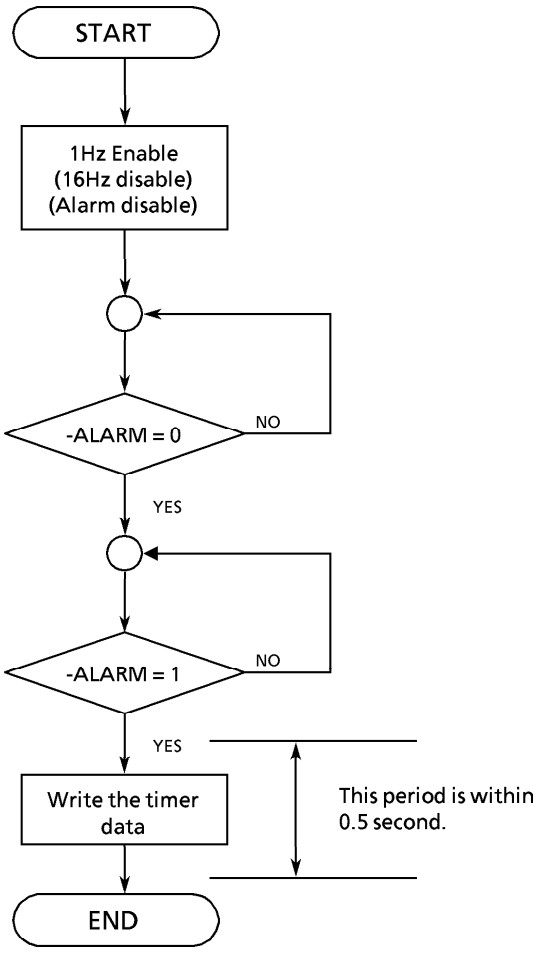
2. DISABLE THE TIMER

The same procedure as that of "Reading the data".



3. USE 1Hz OUTPUT OF ALARM

The same procedure as that of "Reading the data".



In the RTC, the 12-hr or the 24-hr system can be selected as the time digit. This selection is simultaneously made at the timer data writing.

The 12-hr system is turned out when D0 = "0" in the address "A", AM when D1 = "1". The 24-hr system is turned out when D0 = "1".

The data such as "A" and "B" (hexadecimal) can be written as the contents of the timer data, however, if the data other than the data of 0 to 9 is written, the correct timer operation can not be guaranteed.

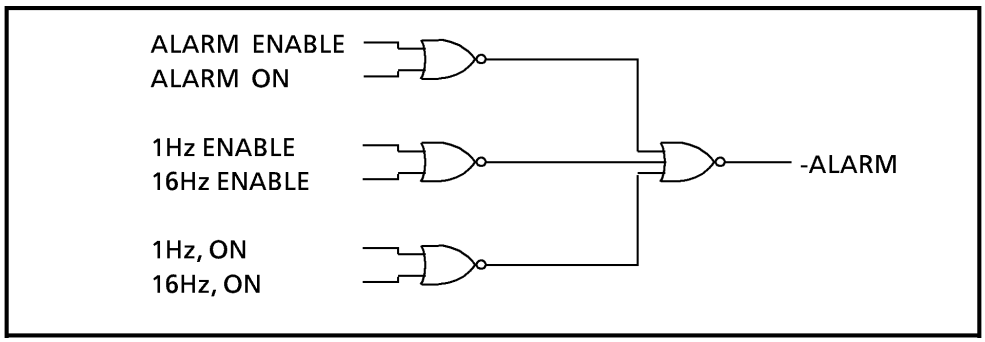
5.2.4 DESCRIPTION of ALARM

When the contents of the timer and the alarm register coincide in the four items, minute, hour, day of week and day in the ALARM ENABLE state, "0" is output at the -ALARM. On this coincidence condition, the items not written at all after the alarm reset are considered to be coincident regardless of the timer contents.

Therefore, when the alarm is required to be output at the same time every day, it is enough only to set the hour and the minute after the alarm reset. When the alarm reset is made, all the contents of the alarm register are cleared to "0". However, when "0" is required to be compared (when "0" is necessary to be individually set at the digits of hour and the minute for example at setting just noon), be sure to write "0".

Caution must be paid for the alarm reset, because when the reset is made in the ALARM ENABLE state, all the items become don't care and the alarm is output until the alarm is set.

Therefore, alarm reset is necessary to be made after the alarm DISABLE is performed.



6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	− 0.5 ~ + 7.0	V
Input Voltage	V_I	− 0.5 ~ VCC + 0.5	V
Operating Temperature	T_{OPR}	− 40 ~ + 85	°C
Storage Temperature	T_{STG}	− 65 ~ + 125	°C

Note1)
The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note2)
The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC and DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

6.2 DC CHARACTERISTICS

(VCC = 5V ± 10%, Ta = − 40 to + 85°C)

PARAMETER	SYMBOL	CONDITIONS	STANDARD VALUE		UNIT
			MIN.	MAX.	
High Level Input Voltage	V_{IH1}	XIN, ADJUST excluded.	2.0	VCC + 0.3	V
Low Level Input Voltage	V_{IL1}	XIN, ADJUST excluded.	− 0.3	0.8	V
High Level Input Voltage	V_{IH2}	ADJUST only	2.2	VCC + 0.3	V
Low Level Input Voltage	V_{IL2}	ADJUST only	− 0.3	0.6	V
High Level Output Current	I_{OH}	VOH = VCC − 0.4[V]		− 0.5	mA
Low Level Output Current	I_{OL}	VOL = 0.4 [V]	2		mA
Input Leak Current	I_{IL}	VIH = 0 to VCC	− 10	+ 10	μA
Consumption Current at BACK UP	I_{CC1}	fo = 32.786KHz VCC = 2.0V		5	μA
Operating Consumption Current	I_{CC2}	RD, WR cycle 100KHz		250	μA
Operating Minimum Voltage of Timer	V_{Cmin}	Ta = 25°C		2.0	V

(VCC = 3V, Ta = − 40 to + 85°C)

PARAMETER	SYMBOL	CONDITIONS	STANDARD VALUE		UNIT
			MIN.	MAX.	
High Level Output Current	I_{OH}	VOH = VCC − 0.4 [V]		− 0.3	mA
Low Level Output Current	I_{OL}	VOL = 0.4 [V]	1		mA
Operating Consumption Current	I_{CC2}	RD, WR cycle 100KHz		60	μA
		RD, WR cycle 32KHz		25	μA

6.3 AC CHARACTERISTICS

WRITE TIMING

(VCC = 5V ± 10%, Ta = −40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	STANDARD VALUE		UNIT
			MIN.	MAX.	
Address Setup Time	t_{AW}		50		ns
-WR Pulse Width	t_{WW}		120		ns
Address Hold TIme	t_{WA}		10		ns
Data Setup Time	t_{DW}		100		ns
Data Hold Time	t_{WD}		20		ns

(VCC = 3V, Ta = −40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	STANDARD VALUE		UNIT
			MIN.	MAX.	
Address Setup Time	t_{AW}		50		ns
-WR Pulse Width	t_{WW}		200		ns
Address Hold TIme	t_{WA}		10		ns
Data Setup Time	t_{DW}		100		ns
Data Hold Time	t_{WD}		40		ns

READ TIMING

(VCC = 5V ± 10%, Ta = −40 to +85°C)

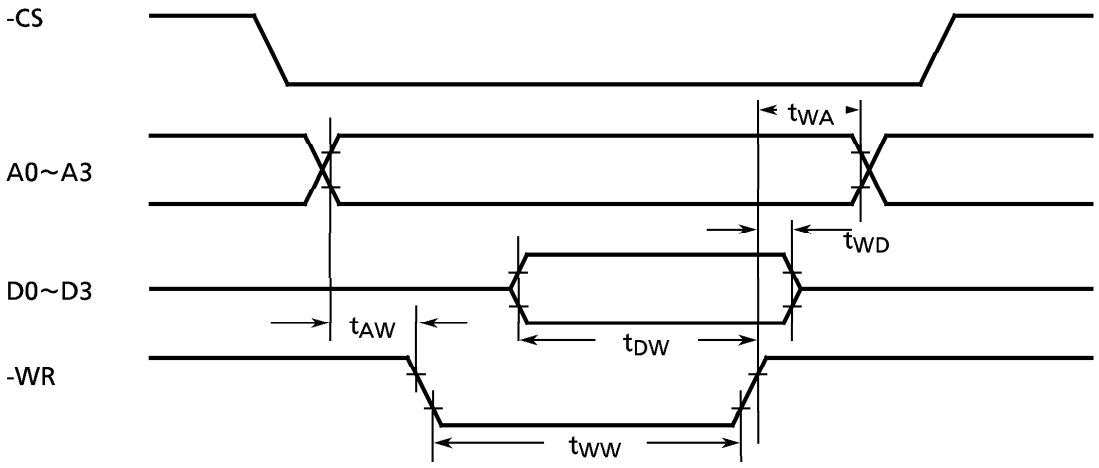
PARAMETER	SYMBOL	CONDITIONS	STANDARD VALUE		UNIT
			MIN.	MAX.	
Address Setup Time	t_{AR}		50		ns
-RD Pulse Width	t_{RR}		250		ns
Address Hold TIme	t_{RA}		10		ns
Data Delay Time	t_{RD}	100pF Load		240	ns
Data Hold Time	t_{DH}		10		ns

(VCC = 3V, Ta = −40 to +85°C)

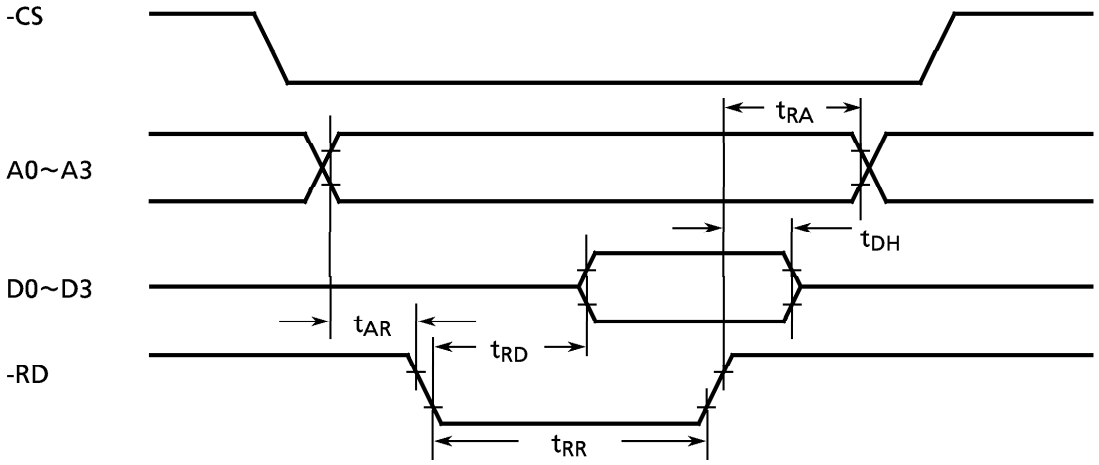
PARAMETER	SYMBOL	CONDITIONS	STANDARD VALUE		UNIT
			MIN.	MAX.	
Address Setup Time	t_{AR}		50		ns
-RD Pulse Width	t_{RR}		480		ns
Address Hold TIme	t_{RA}		10		ns
Data Delay Time	t_{RD}	100pF Load		470	ns
Data Hold Time	t_{DH}		10		ns

6.4 TIMING CHART

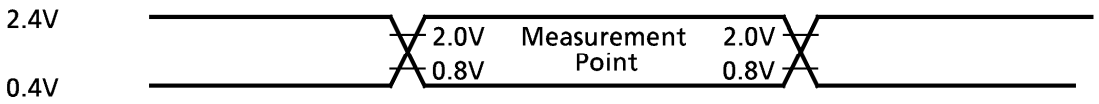
6.4.1 WRITE OPERATION (CS = "H")



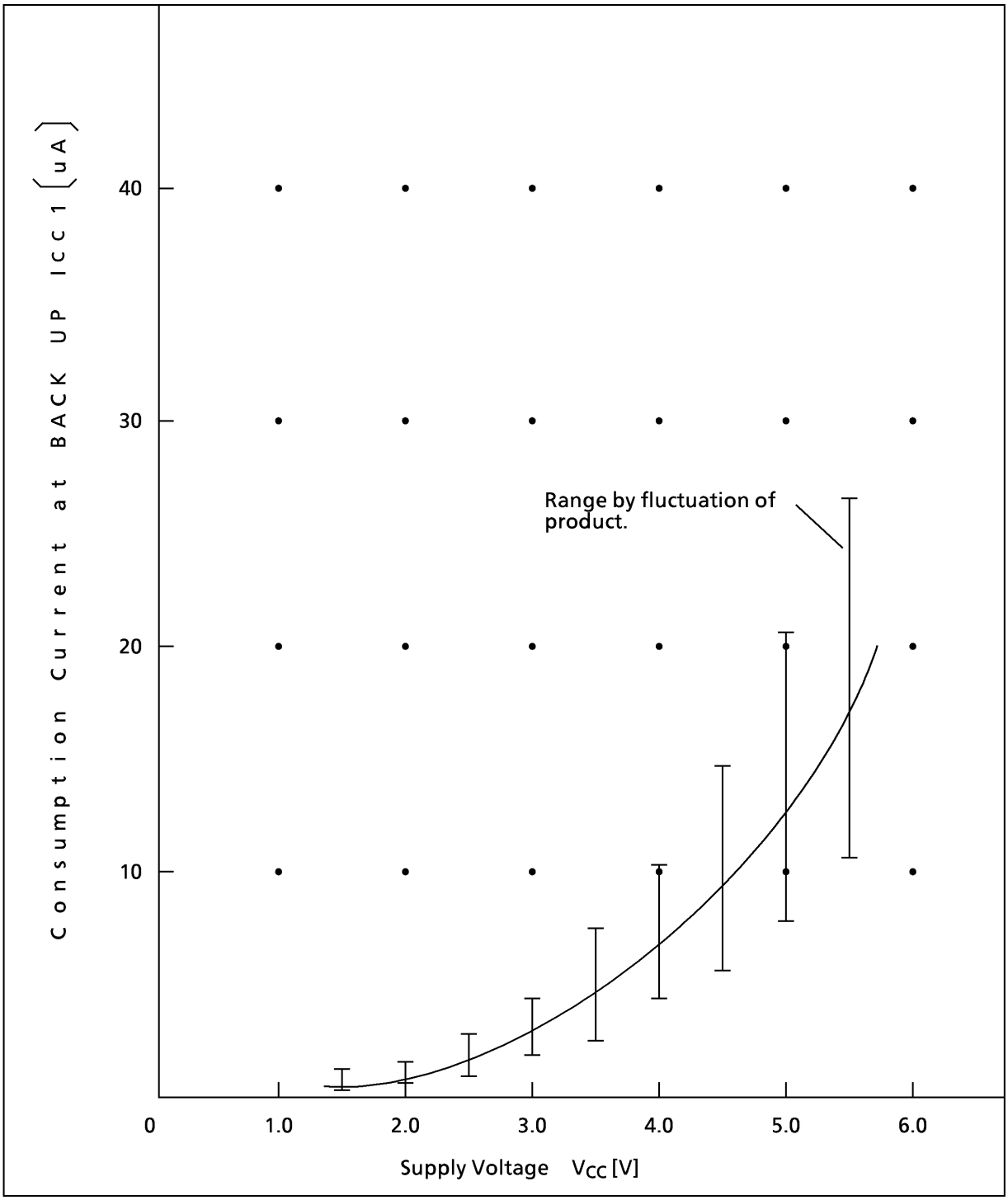
6.4.2 READ OPERATION (CS = "H")



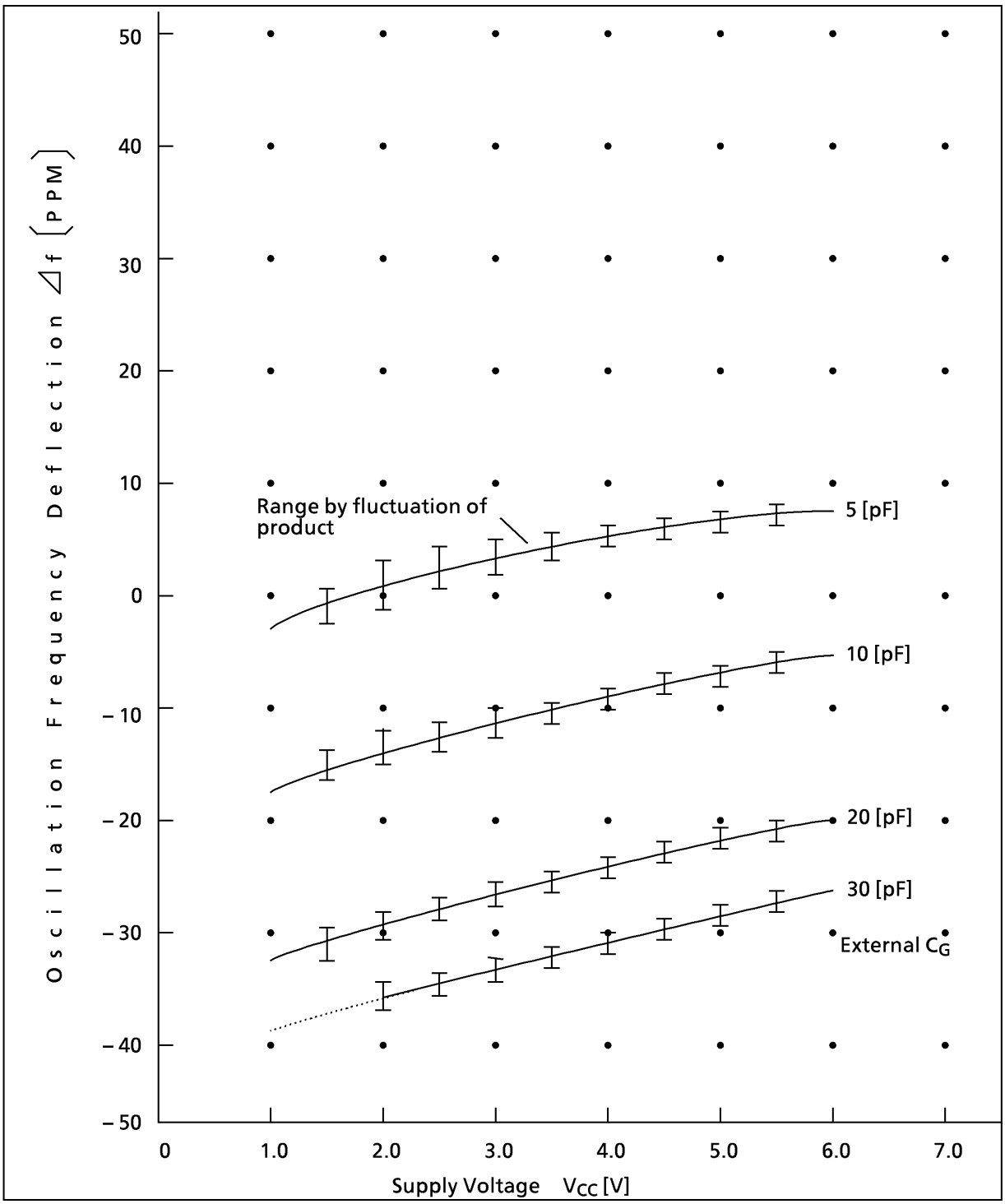
6.4.3 AC TEST WAVEFORM



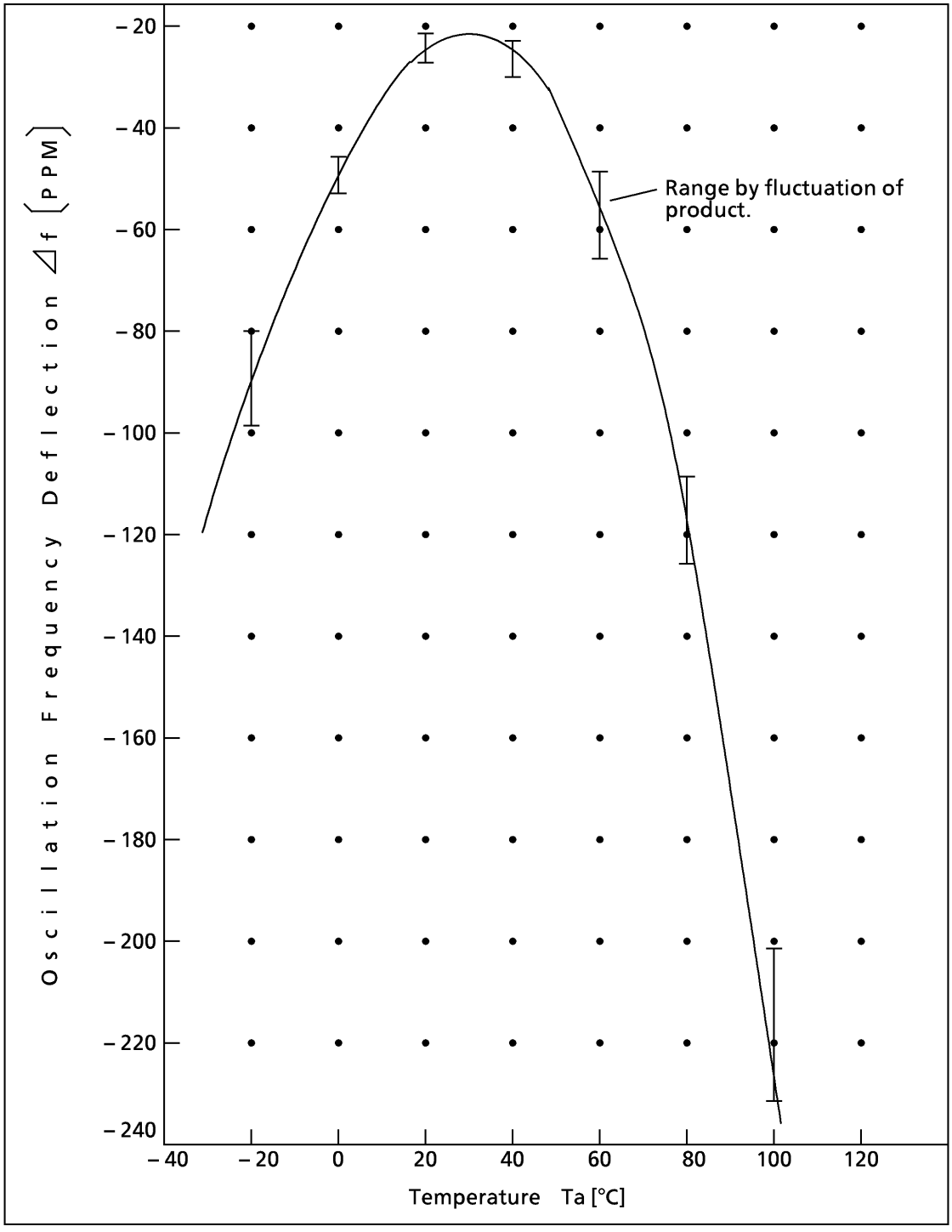
Characteristic of Consumption Current at BACK UP (C_G = 20pF, C_D = 30pF, Ta = 25°C)



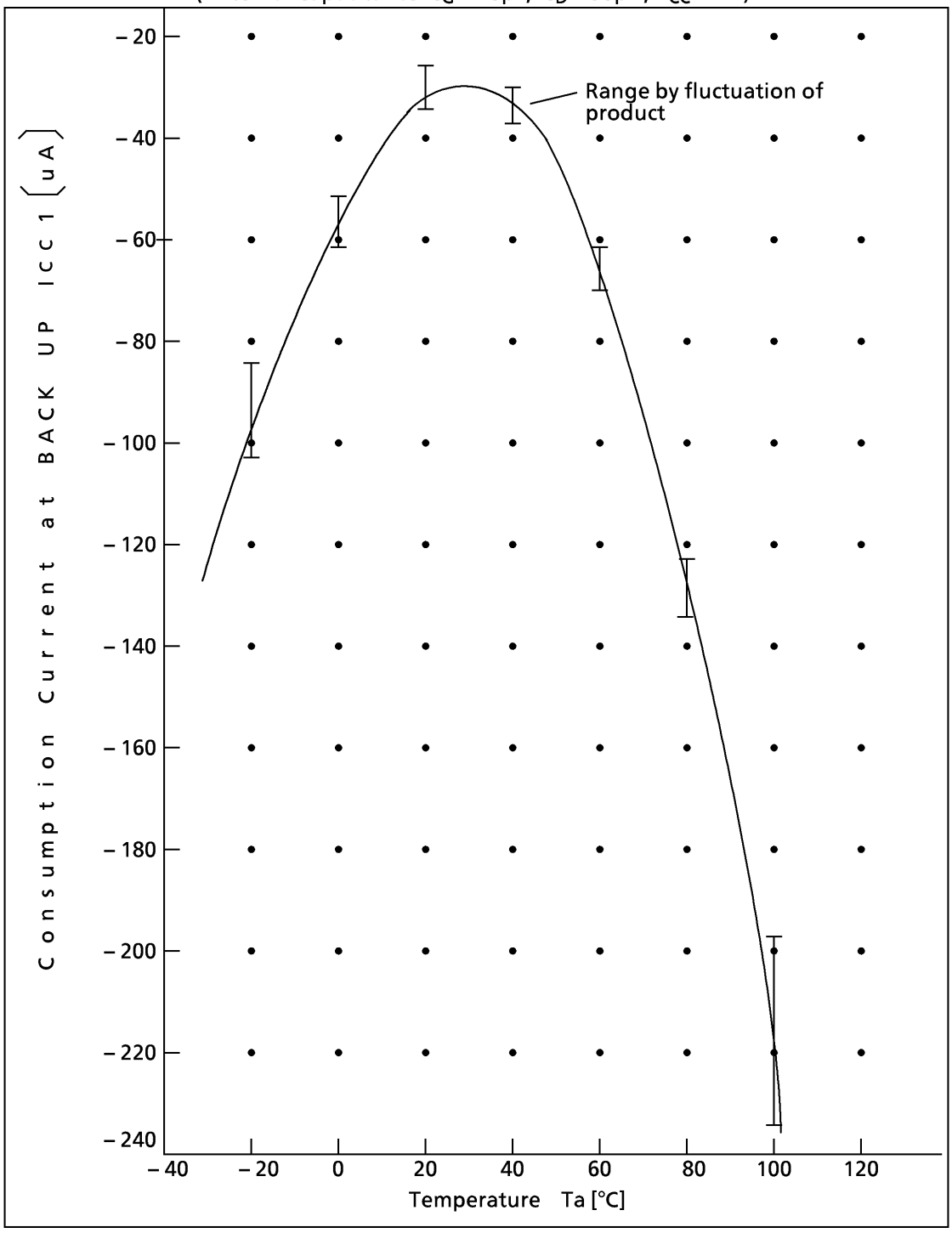
Supply Voltage Dependence of Oscillation Frequency (C_D = 30pF, Ta = 25°C)



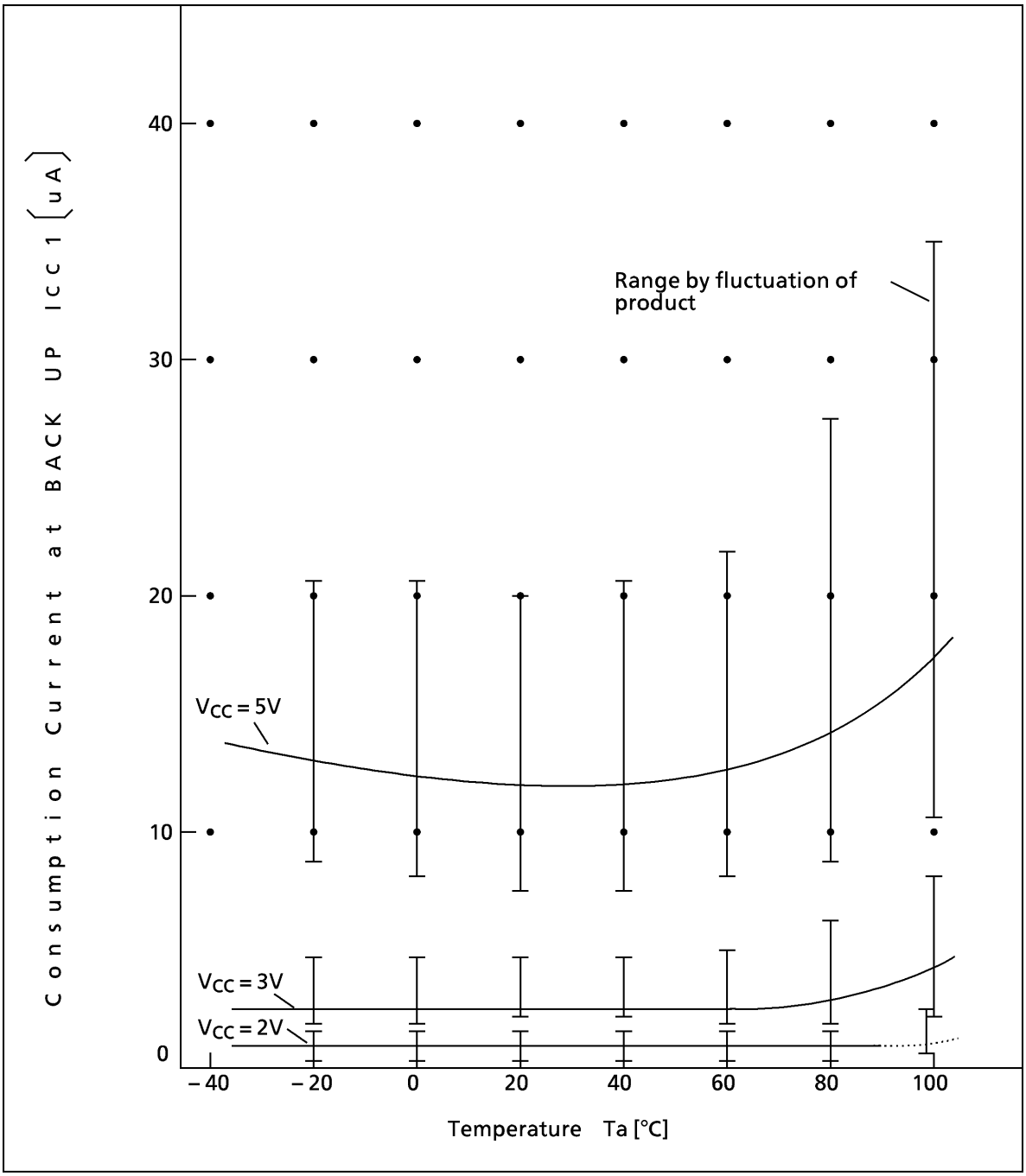
Temperature Characteristic of Oscillation Frequency
(External Capacitance : C_G = 20pF, C_D = 30pF , V_{CC} = 5V)



Temperature Characteristic of Oscillation Frequency
(External Capacitance C_G = 20pF, C_D = 30pF , V_{CC} = 2V)



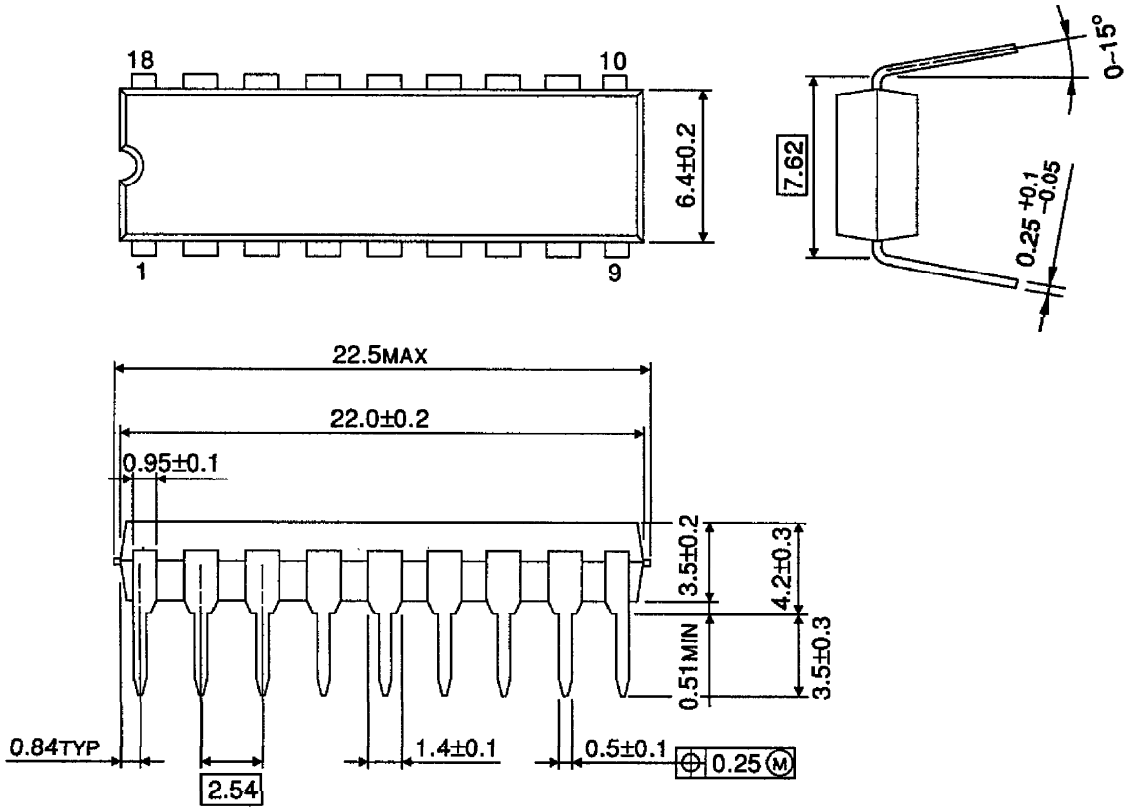
Temperature Characteristic of Consumption Current (C_G = 20pF, C_D = 30pF)



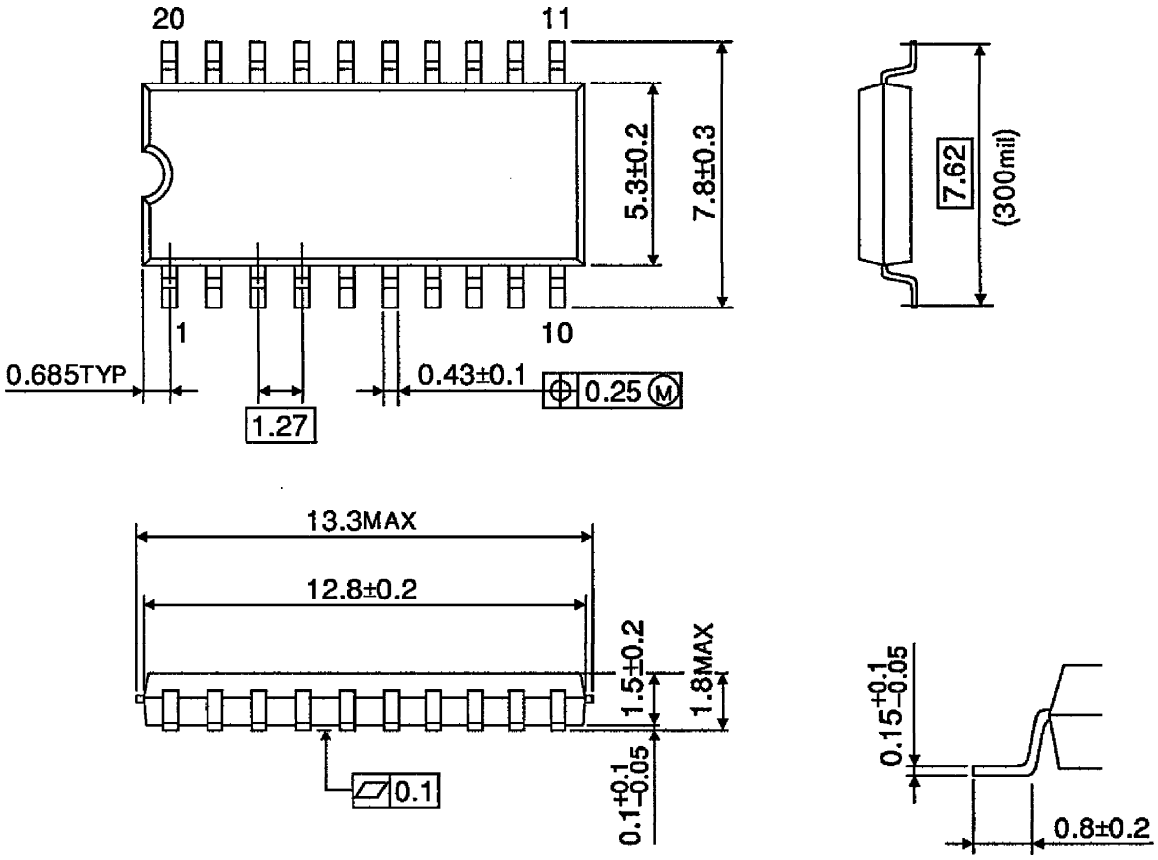
7. PACKAGE DIMENSION

DIP18-P-300-2.54A

Unit : mm



SOP20-P-300-1.27 Unit : mm



note) SOP20-P-300 is capable of solder dip and Near infrared mounting. (See TOSHIBA Package Manual (Page 69).
However, we don't guarantee in case of TC8521AM.

PACKAGE			OVERALL HEATING METHOD				LOCALIZED HEATING METHOD			
Package and number of leads	Package size (mm)	Maximum die pad size	Solder dip	Near infared	Far/medium infared with top and bottom heating	V.P.S	Solder Iron	Pulse heater	Hot air	Laser
SOP 20	5.3 × 12.8 × 1.5	2.7 × 3.5	×	×	◎	◎	◎	◎	◎	◎

◎ : Mounting is capable

If you have any question, we will appreciate.