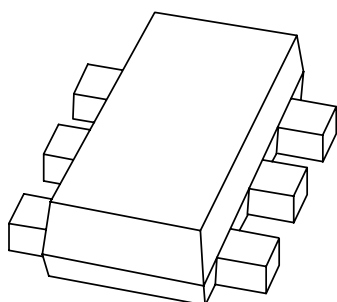


# DATA SHEET



## **PEMH9**

**NPN resistor-equipped transistors;  
R1 = 10 k $\Omega$ , R2 = 47 k $\Omega$**

Product specification  
Supersedes data of 2001 Oct 22

2001 Nov 07

# NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 47 kΩ

# PEMH9

FEATURES

- 300 mW total power dissipation
- Very small 1.6 × 1.2 mm ultra thin package
- Self alignment during soldering due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

NPN resistor-equipped transistors in a SOT666 plastic package.

MARKING

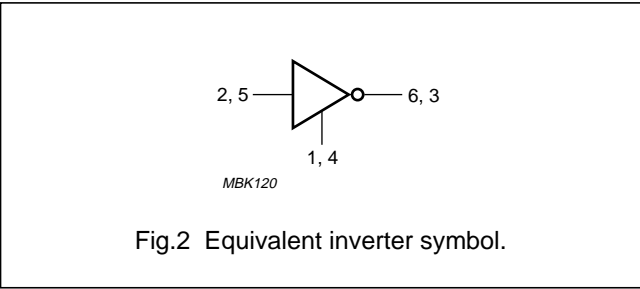
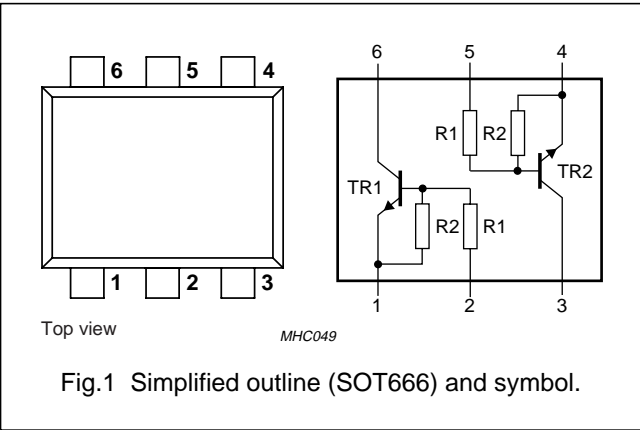
TYPE NUMBER	MARKING CODE
PEMH9	H9

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	50	V
I <sub>CM</sub>	peak collector current	100	mA
TR1	NPN	–	–
TR2	NPN	–	–
R1	bias resistor	10	kΩ
R2	bias resistor	47	kΩ

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



# NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 47 kΩ

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>i</sub>	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

## Note

1. Transistor mounted on an FR4 printed-circuit board.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

## Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

# NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 47 kΩ

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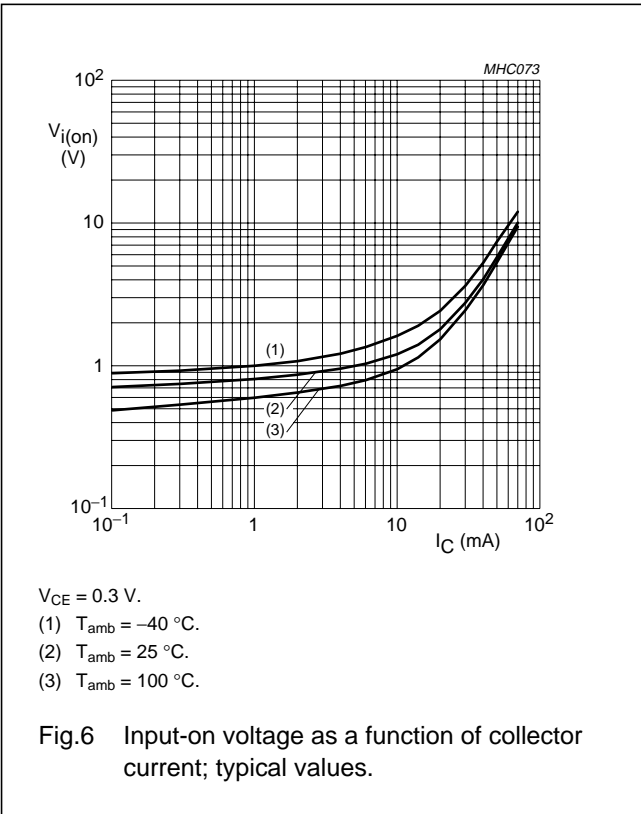
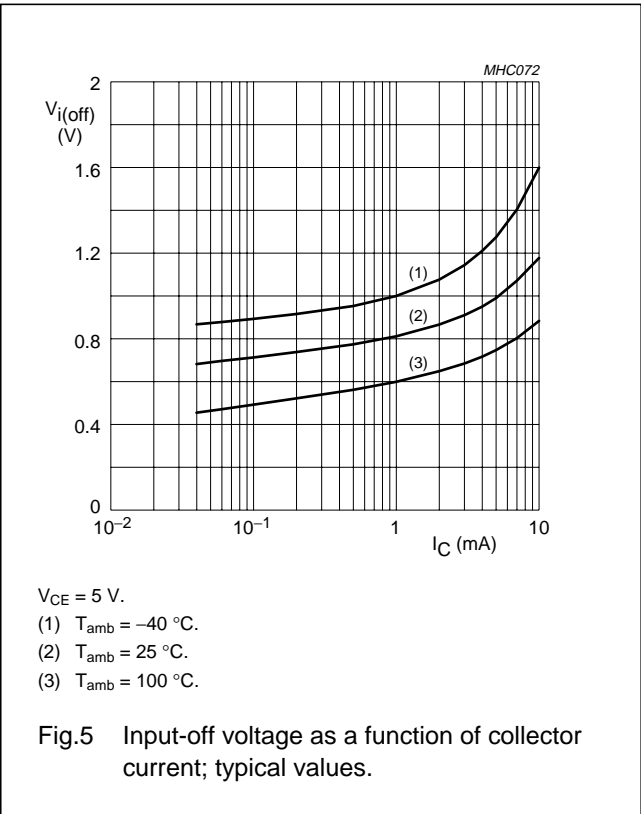
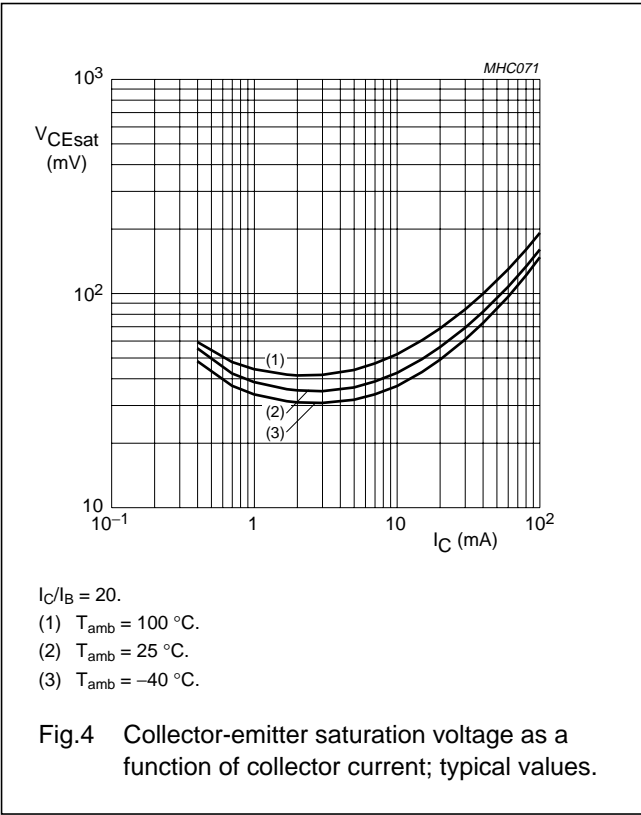
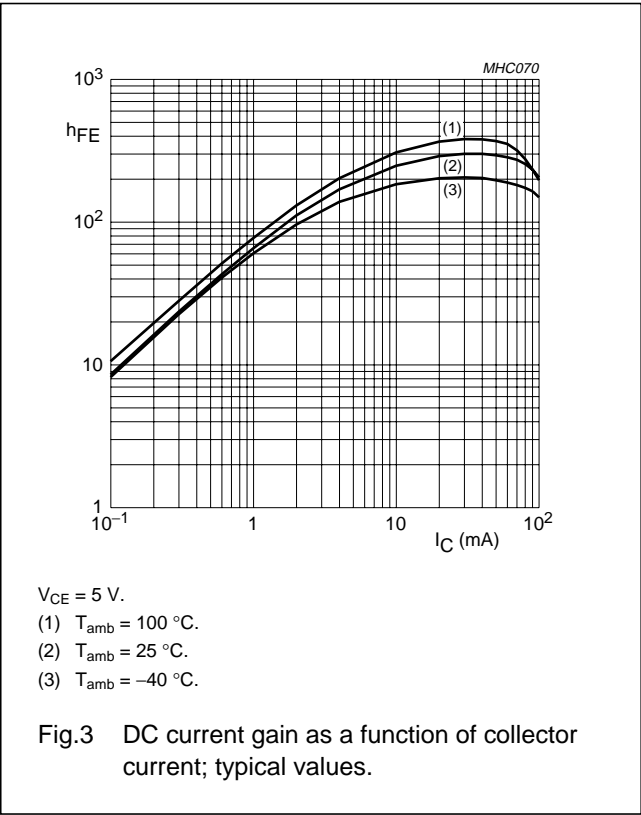
## CHARACTERISTICS

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0$	–	–	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 50\text{ V}; I_B = 0$	–	–	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0; T_j = 150\text{ °C}$	–	–	50	μA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	150	μA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	100	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}$	–	–	100	mV
$V_{i(off)}$	input off voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ μA}$	–	0.7	0.5	V
$V_{i(on)}$	input on voltage	$V_{CE} = 0.3\text{ V}; I_C = 1\text{ mA}$	1.4	0.8	–	V
R1	input resistor		7	10	13	kΩ
$\frac{R2}{R1}$	resistor ratio		3.7	4.7	5.7	
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	–	2.5	pF

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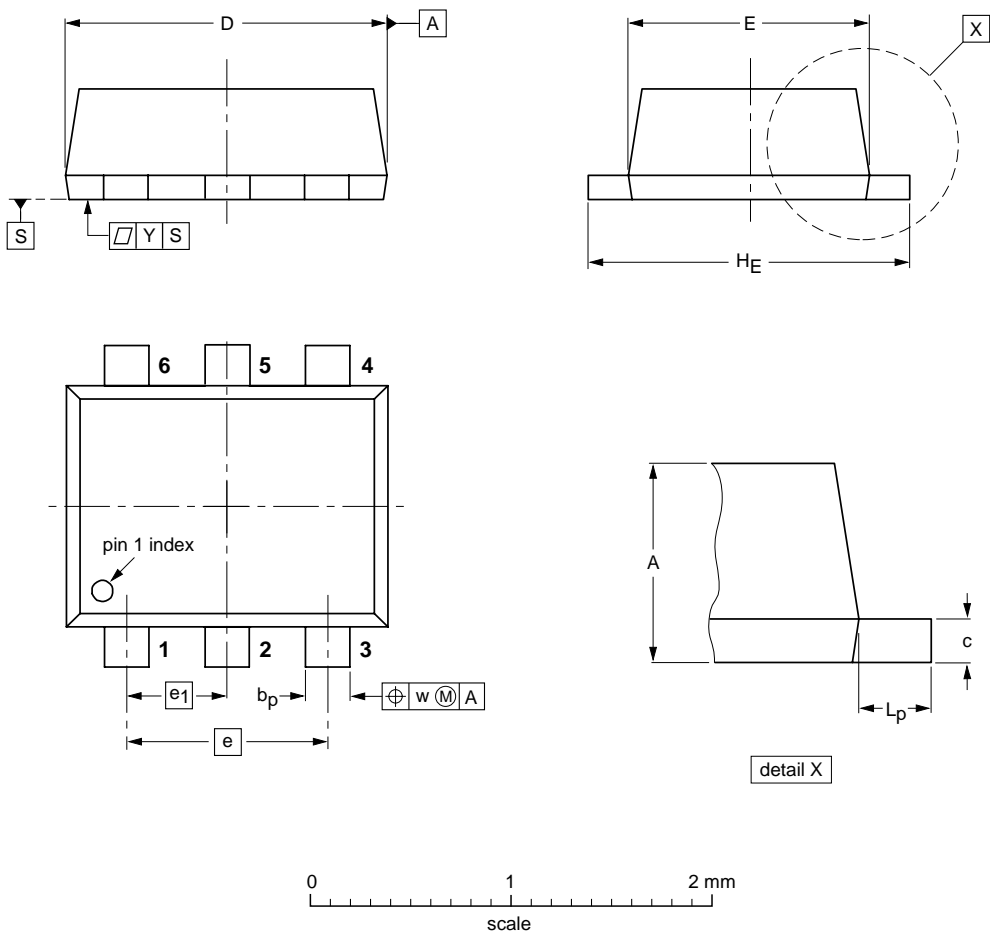
NPN resistor-equipped transistors;  
R1 = 10 kΩ, R2 = 47 kΩ

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						-01-01-04- 01-08-27

NPN resistor-equipped transistors;  
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