8K x 8 CMOS Static RAM

FEATURES

- Available in 70/100 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:

  MS6264
  - 495mW (Max.) Operating
  - 82.5mW (Max.) Standby
  - 11mW (Max.) Power Down

  MS6264L
  - 467.5mW (Max.) Operating
  - 16.5mW (Max.) Standby
  - 550µW (Max.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion

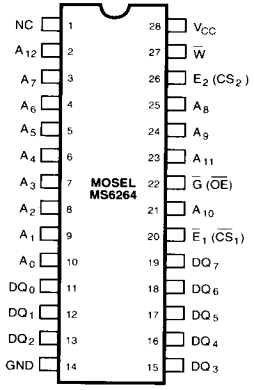
DESCRIPTION

The MOSEL MS6264 is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and tri-state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

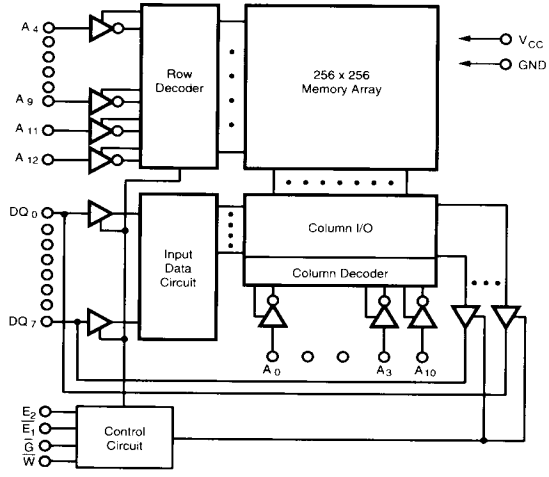
The device is manufactured in MOSEL's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MOSEL MS6264 is packaged in the JEDEC standard 28 pin 600 mil wide DIP and 330 mil wide SOP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{12} Address Inputs
These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input
E_2 Chip Enable 2 Input
$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

3

TRUTH TABLE

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

DC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264			MS6264L			UNITS
			MIN.	TYP.(1)	MAX.	MIN.	TYP.(1)	MAX.	
V_{IL}	Guaranteed Input Low Voltage(2)		-0.5	-	+0.8	-0.5	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	3.5	6.0	2.2	3.5	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	2	-	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	-	-	2	-	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	-	50	90	-	45	85	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	15	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$ $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	.02	2	-	. 01	0.1	mA

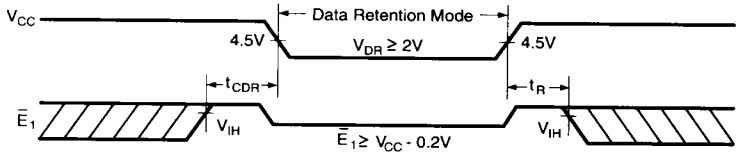
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

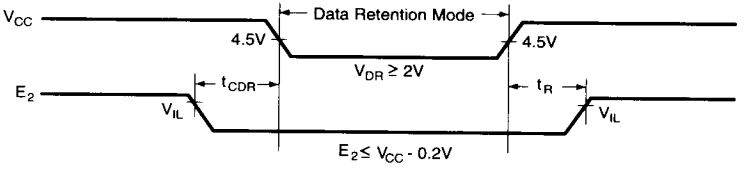
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{E}_1$ Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (E_2 Controlled)



AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

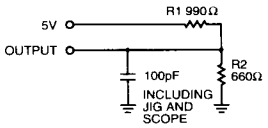


Figure 1a

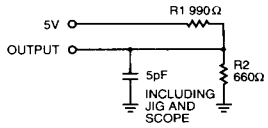
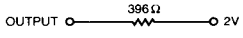


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

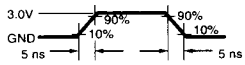


Figure 2

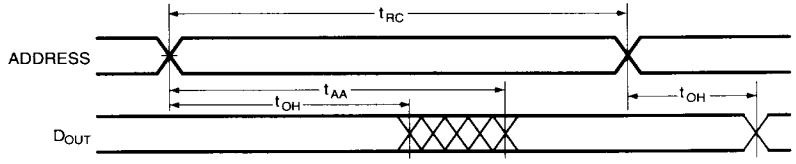
AC ELECTRICAL CHARACTERISTICS (over the operating range)

READ CYCLE

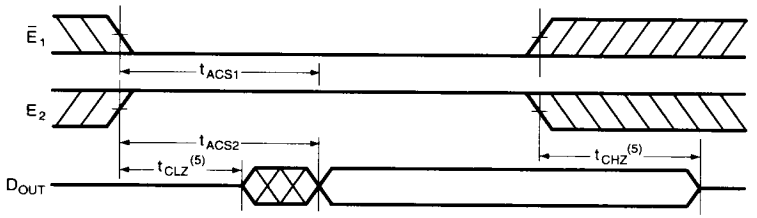
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264-70 MS6264L-70 MIN.	TYP.	MAX.	MS6264-10 MS6264L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time	70	-	-	100	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	-	70	-	-	100	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time ($\overline{E}_1$)	-	-	70	-	-	100	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time (E_2)	-	-	70	-	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	-	35	-	-	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z ($\overline{E}_1$)	5	-	-	5	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to to Output Low Z (E_2)	5	-	-	5	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	-	5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z ($\overline{E}_1$)	0	-	35	0	-	35	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z (E_2)	0	-	35	0	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	-	30	0	-	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (READ CYCLE)

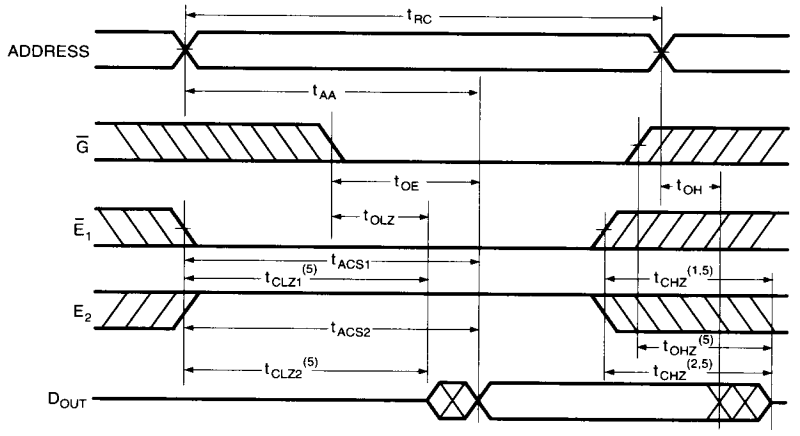
READ CYCLE 1[1,2,4]



READ CYCLE 2[1,3,4]



READ CYCLE 3[1,4]



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

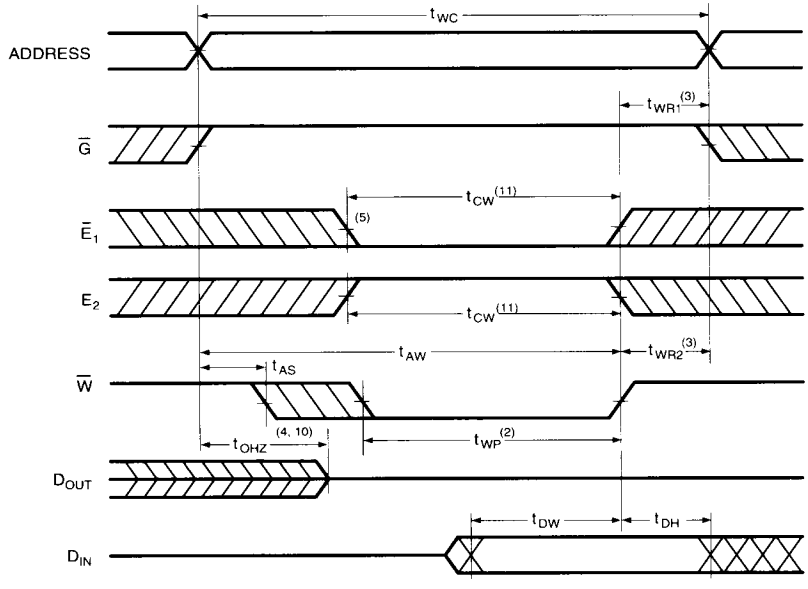
AC ELECTRICAL CHARACTERISTICS (over the operating range)

WRITE CYCLE

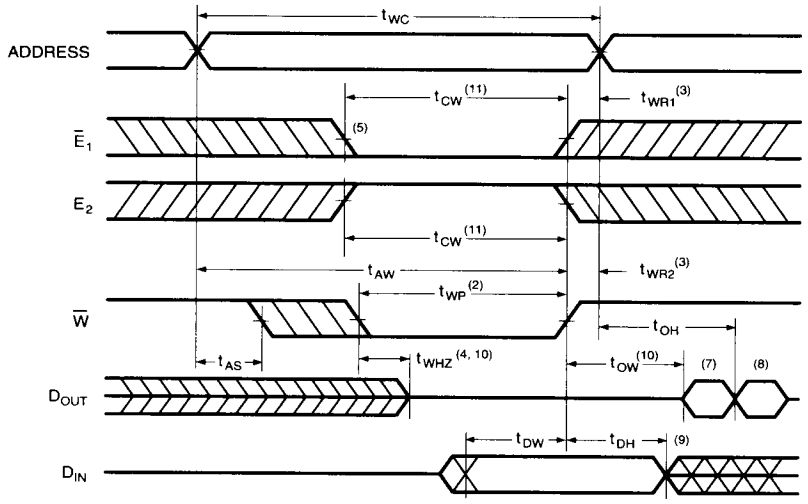
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264-70 MS6264L-70 MIN.	TYP.	MAX.	MS6264-10 MS6264L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		70	-	-	100	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write		45	-	-	80	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		65	-	-	80	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		45	-	-	60	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	$\overline{E}_1, \overline{W}$	5	-	-	5	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	5	-	-	5	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		0	-	30	-	-	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		30	-	-	40	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	30	0	-	35	ns
t_{WHQX}	t_{OW}	End of Write to Output Active		5	-	-	5	-	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
70	MS6264-70PC	P28-1	0°C to +70°C
70	MS6264-70FC	S28-2	0°C to +70°C
70	MS6264L-70PC	P28-1	0°C to +70°C
70	MS6264L-70FC	S28-2	0°C to +70°C
100	MS6264-10PC	P28-1	0°C to +70°C
100	MS6264-10FC	S28-2	0°C to +70°C
100	MS6264L-10PC	P28-1	0°C to +70°C
100	MS6264L-10FC	S28-2	0°C to +70°C