ISL85410

Wide V_{IN} 1A Synchronous Buck Regulator

FN8375
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The ISL85410 is a 1A synchronous buck regulator with an input range of 3V to 40V. It provides an easy-to-use, high efficiency low BOM count solution for a variety of applications.

The ISL85410 integrates both high-side and low-side NMOS FETs and features a PFM mode for improved efficiency at light loads. This feature can be disabled if a forced PWM mode is needed. The ISL85410 switches at a default frequency of 500kHz; however, it can also be programmed using an external resistor from 300kHz to 2MHz. The ISL85410 has the ability to use internal or external compensation. By integrating both NMOS devices and providing internal configuration options, minimal external components are required, which reduces BOM count and complexity of design.

With a wide V_{IN} range and reduced BOM, the ISL85410 provides an easy to implement design solution for a variety of applications while giving superior performance. The ISL85410 provides a very robust design for high-voltage industrial applications and an efficient solution for battery powered applications.

The ISL85410 is available in a small Pb-free 4mmx3mm DFN plastic package with a full-range industrial temperature of -40°C to +125°C.

Related Literature

For a full list of related documents, visit our website:

- ISL85410 device page

Features

- Wide input voltage range: 3V to 40V
- Synchronous operation for high efficiency
- No compensation required
- Integrated high-side and low-side NMOS devices
- Selectable PFM or forced PWM mode at light loads
- Internal fixed frequency (500kHz) or adjustable switching frequency (300kHz to 2MHz)
- Continuous output current up to 1A
- Internal or external soft-start
- Minimal external components required
- Power-good and enable functions available

Applications

- Industrial control
- Medical devices
- Portable instrumentation
- Distributed power supplies
- Cloud infrastructure

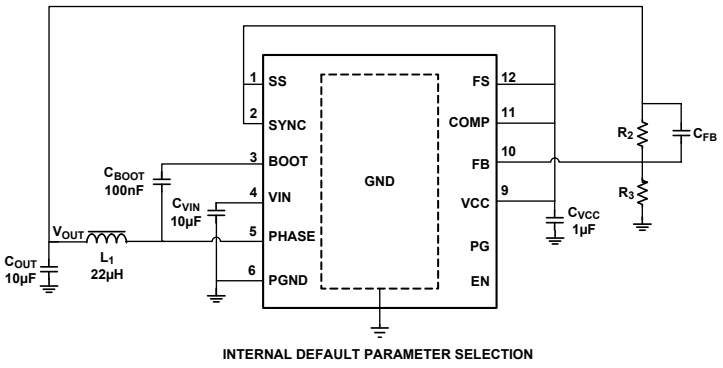

FIGURE 1. TYPICAL APPLICATION

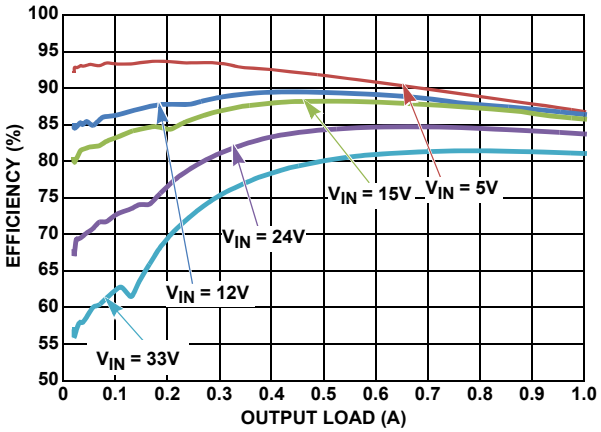

FIGURE 2. EFFICIENCY vs LOAD, PFM, V_{OUT} = 3.3V

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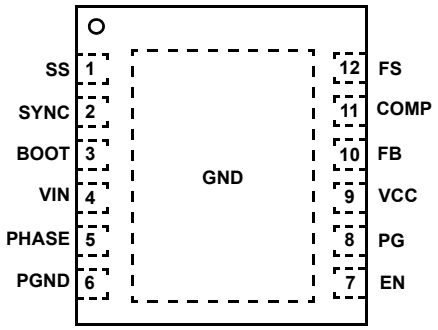
Pin Configuration

12 LD 4x3 DFN
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	SS	Controls the soft-start ramp time of the output. A single capacitor from the SS pin to ground determines the output ramp rate. See "Soft-Start" on page 14 for soft-start details. If the SS pin is tied to VCC, an internal soft-start of 2ms is used.
2	SYNC	Synchronization and light load operational mode selection input. Connect to logic high or VCC for PWM mode. Connect to logic low or ground for PFM mode. Logic ground enables the IC to automatically choose PFM or PWM operation. Connect to an external clock source for synchronization with positive edge trigger. The sync source must be higher than the programmed IC frequency. An internal 5MΩ pull-down resistor prevents an undefined logic state if SYNC is left floating.
3	BOOT	Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn on the internal N-Channel MOSFET. Connect an external 100nF capacitor from this pin to PHASE.
4	VIN	The input supply for the power stage of the regulator and the source for the internal linear bias regulator. Place a minimum of 4.7µF ceramic capacitance from VIN to GND and close to the IC for decoupling.
5	PHASE	Switch node output. It connects the switching FETs with the external output inductor.
6	PGND	Power ground connection. Connect directly to the system GND plane.
7	EN	Regulator enable input. The regulator and bias LDO are held off when the pin is pulled to ground. When the voltage on this pin rises above 1V, the chip is enabled. Connect this pin to VIN for automatic start-up. Do not connect the EN pin to VCC because the LDO is controlled by EN voltage.
8	PG	Open-drain, power-good output that is pulled to ground when the output voltage is below regulation limits or during the soft-start interval. There is an internal 5MΩ internal pull-up resistor.
9	VCC	Output of the internal 5V linear bias regulator. Decouple to PGND with a 1µF ceramic capacitor at the pin.
10	FB	Feedback pin for the regulator. FB is the inverting input to the voltage loop error amplifier. COMP is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the PWM regulator's power-good and UVLO circuits use FB to monitor the regulator output voltage.
11	COMP	COMP is the output of the error amplifier. When it is tied to VCC, internal compensation is used. When only an RC network is connected from COMP to GND, external compensation is used. See "Loop Compensation Design" on page 17 for more details.
12	FS	Frequency selection pin. Tie to VCC for 500kHz switching frequency. Connect a resistor to GND for adjustable frequency from 300kHz to 2MHz.
EPAD	GND	Signal ground connections. Connect to the application board GND plane with at least five vias. All voltage levels are measured with respect to this pin. The EPAD MUST NOT float.

Typical Application Schematics

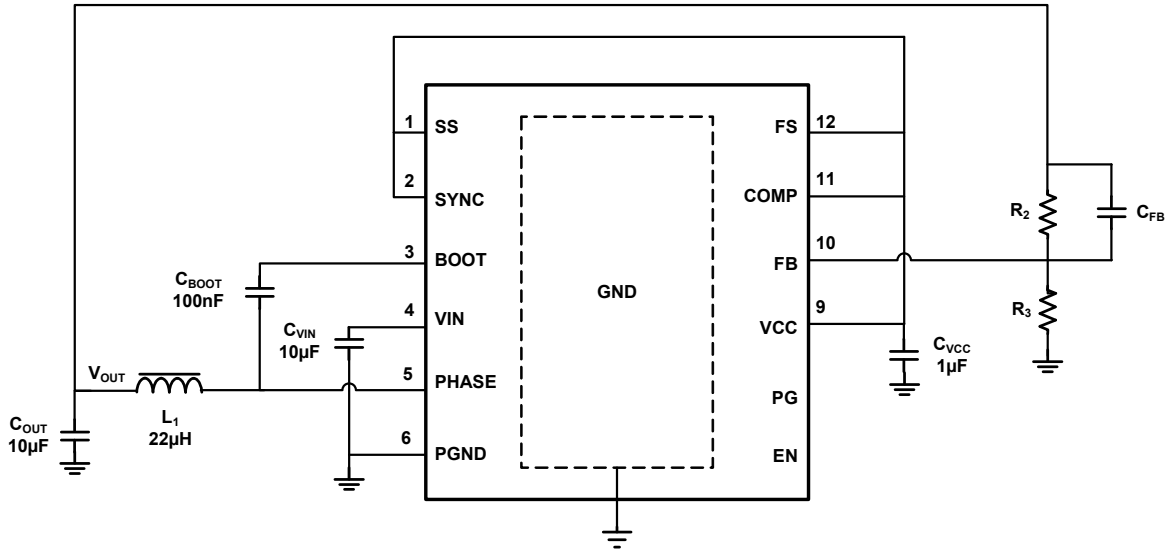


FIGURE 3. INTERNAL DEFAULT PARAMETER SELECTION

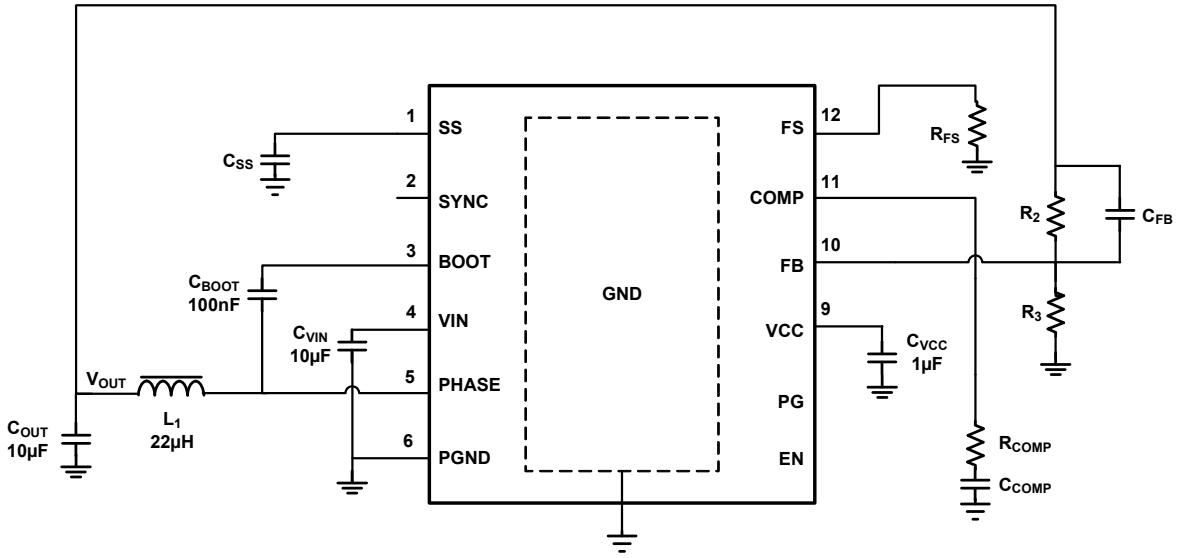


FIGURE 4. USER PROGRAMMABLE PARAMETER SELECTION

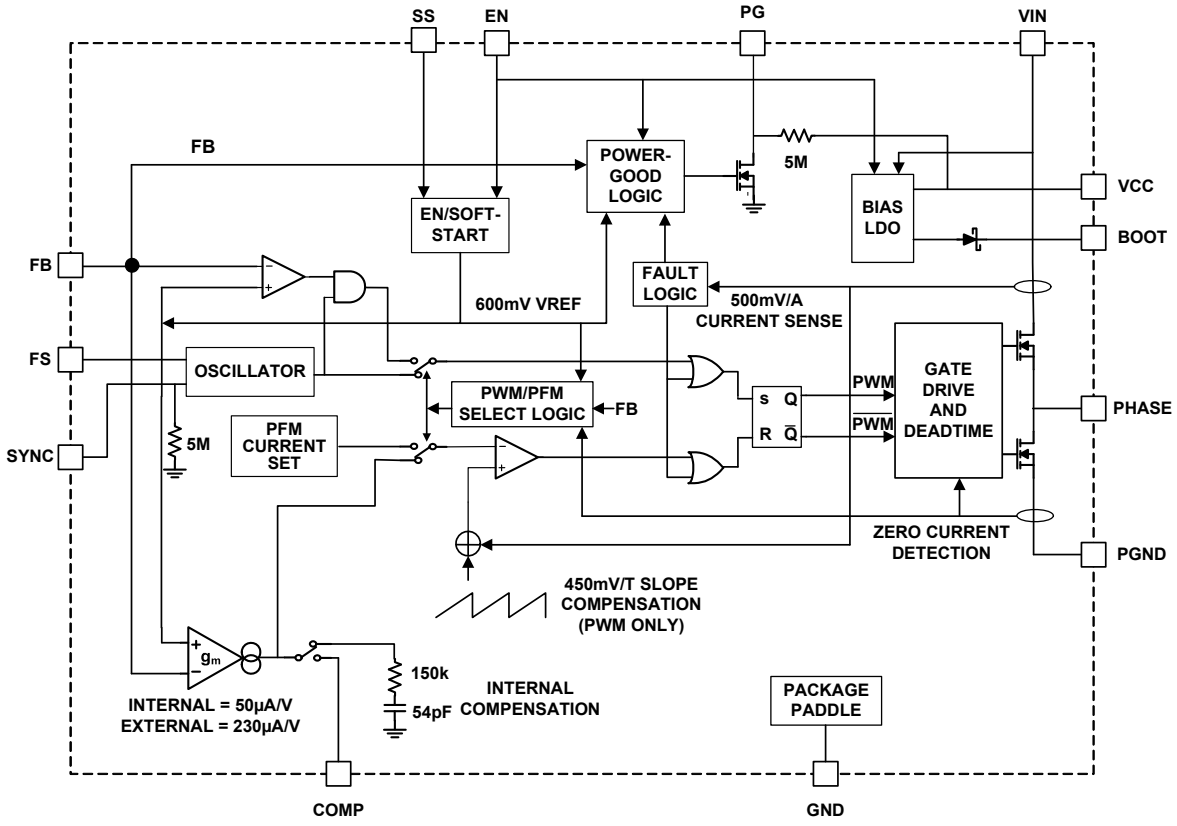
TABLE 1. EXTERNAL COMPONENT SELECTION

V_{OUT} (V)	L_1 (µH)	C_{OUT} (µF)	R_2 (kΩ)	R_3 (kΩ)	C_{FB} (pF)	R_{FS} (kΩ)	R_{COMP} (kΩ)	C_{COMP} (pF)
12	22	2 x 22	90.9	4.75	22	115	150	470
5	22	47 + 22	90.9	12.4	27	DNP (Note 1)	100	470
3.3	22	47 + 22	90.9	20	27	DNP (Note 1)	100	470
2.5	22	47 + 22	90.9	28.7	27	DNP (Note 1)	100	470
1.8	12	47 + 22	90.9	45.5	27	DNP (Note 1)	70	470

NOTE:

1. Connect FS to V_{CC}.

Functional Block Diagram



Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 2)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL85410FRZ	5410	-40 to +125	-	12 Ld DFN	L12.4x3
ISL85410FRZ-T	5410	-40 to +125	6k	12 Ld DFN	L12.4x3
ISL85410FRZ -T7A	5410	-40 to +125	250	12 Ld DFN	L12.4x3
ISL85410EVAL1Z	Evaluation Board				
ISL85410DEMO1Z	Demonstration Board				

NOTES:

2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL85410 device page. For more information about MSL, see TB363.

Absolute Maximum Ratings

VIN to GND . . . . . -0.3V to +43V
PHASE to GND . . . . . -0.3V to VIN+0.3V (DC)
PHASE to GND . . . . . -2V to +44V (20ns)
EN to GND . . . . . -0.3V to +43V
BOOT to PHASE . . . . . -0.3V to +5.5V
COMP, FS, PG, SYNC, SS, VCC to GND . . . . . -0.3V to +5.9V
FB to GND . . . . . -0.3V to +2.95V
ESD Rating
Human Body Model (Tested per JESD22-A114) 2kV
Charged Device Model (Tested per JESD22-C101E) 1.5kV
Latch-Up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 5, 6)	42	4.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature . . . . . -40°C to +125°C
Supply Voltage . . . . . +3V to +40V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A = -40°C to +125°C, V_{IN} = 3V to 40V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
SUPPLY VOLTAGE						
V_{IN} Voltage Range	V_{IN}		**3**		**40**	V
V_{IN} Quiescent Supply Current	I_Q	V_{FB} = 0.7V, SYNC = 0V, f_{SW} = V_{CC}		80		µA
V_{IN} Shutdown Supply Current	I_{SD}	EN = 0V, V_{IN} = 40V (Note 7)		2	**4**	µA
V_{CC} Voltage	V_{CC}	V_{IN} = 6V, I_{OUT} = 0 to 10mA	**4.5**	5.1	**5.7**	V
POWER-ON RESET						
V_{CC} POR Threshold		Rising edge		2.75	**2.95**	V
		Falling edge	**2.35**	2.6		V
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	FS pin = V_{CC}	**430**	500	**570**	kHz
		Resistor from the FS pin to GND = 340kΩ	**240**	300	**360**	kHz
		Resistor from the FS pin to GND = 32.4kΩ		2000		kHz
Minimum Off-Time	t_{MIN_OFF}	V_{IN} = 3V		150		ns
Minimum On-Time	t_{MIN_ON}	(Note 10)		90		ns
FS Voltage	V_{FS}	R_{FS} = 100kΩ	**0.39**	0.4	**0.41**	V
Synchronization Frequency	SYNC		**300**		**2000**	kHz
SYNC Pulse Width			**100**			ns
ERROR AMPLIFIER						
Error Amplifier Transconductance Gain	g_m	External compensation	**165**	230	**295**	µA/V
		Internal compensation		50		µA/V
FB Leakage Current		V_{FB} = 0.6V		1	**150**	nA
Current Sense Amplifier Gain	R_T		**0.46**	0.5	**0.54**	V/A
FB Voltage		T_A = -40°C to +85°C	0.590	0.599	0.606	V
		T_A = -40°C to +125°C	**0.590**	0.599	**0.607**	V

Electrical Specifications T_A = -40°C to +125°C, V_{IN} = 3V to 40V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
POWER-GOOD						
Lower PG Threshold - VFB Rising				90	**94**	%
Lower PG Threshold - VFB Falling			**82.5**	86		%
Upper PG Threshold - VFB Rising				116.5	**120**	%
Upper PG Threshold - VFB Falling			**107**	112		%
PG Propagation Delay		Percentage of the soft-start time		10		%
PG Low Voltage		I_{SINK} = 3mA, EN = V_{CC}, V_{FB} = 0V		0.05	**0.3**	V
TRACKING AND SOFT-START						
Soft-Start Charging Current	I_{SS}		**4.2**	5.5	**6.5**	µA
Internal Soft-Start Ramp Time		EN/SS = V_{CC}	**1.5**	2.4	**3.4**	ms
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising threshold		150		°C
	T_{HYS}	Hysteresis		20		°C
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	IPLIMIT	(Note 8)	**1.3**	1.5	**1.7**	A
PFM Peak Current Limit	I_{PK_PFM}		**0.34**	0.4	**0.5**	A
Zero Cross Threshold				15		mA
Negative Current Limit	INLIMIT	(Note 8)	**-0.67**	-0.6	**-0.53**	A
POWER MOSFET						
High-Side	R_{HDS}	I_{PHASE} = 100mA, V_{CC} = 5V		250	**350**	mΩ
Low-Side	R_{LDS}	I_{PHASE} = 100mA, V_{CC} = 5V		90	**130**	mΩ
PHASE Leakage Current		EN = PHASE = 0V			**300**	nA
PHASE Rise Time	t_{RISE}	V_{IN} = 40V		10		ns
EN/SYNC						
Input Threshold		Falling edge, logic low	**0.4**	1		V
		Rising edge, logic high		1.2	**1.4**	V
EN Logic Input Leakage Current		EN = 0V/40V	**-0.5**		**0.5**	µA
SYNC Logic Input Leakage Current		SYNC = 0V		10	**100**	nA
		SYNC = 5V		1.0	**1.55**	µA

NOTES:

7. Test condition: V_{IN} = 40V, FB forced above regulation point (0.6V), switching and power MOSFET gate charging current not included.
8. Established by both current sense amplifier gain test and current sense amplifier output test at I_L = 0A.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Minimum on-time required to maintain loop stability.

Efficiency Curves f_{SW} = 500kHz, T_A = +25°C

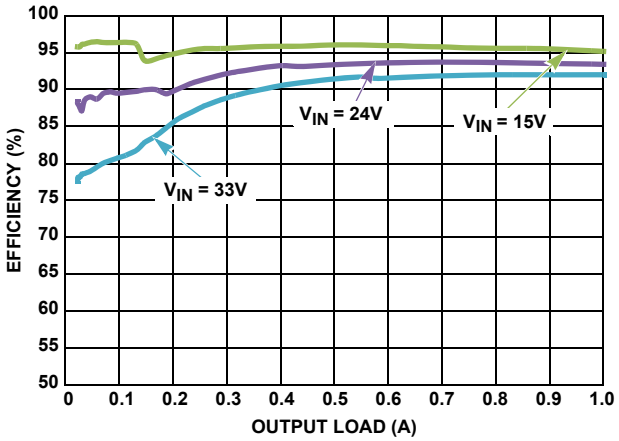


FIGURE 5. EFFICIENCY vs LOAD, PFM, V_{OUT} = 12V

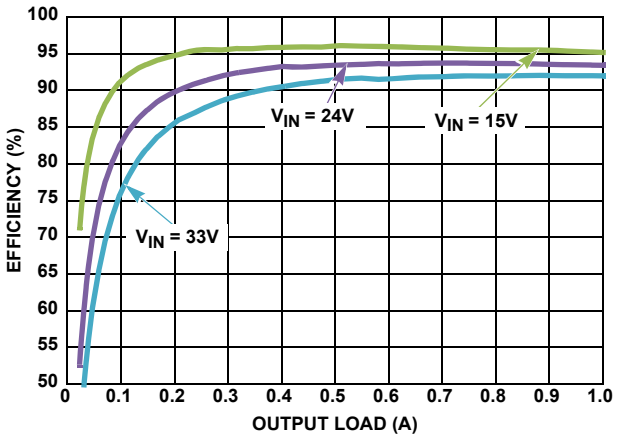


FIGURE 6. EFFICIENCY vs LOAD, PWM, V_{OUT} = 12V

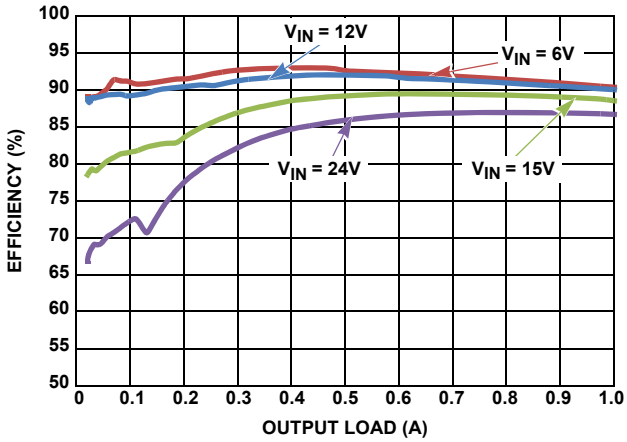


FIGURE 7. EFFICIENCY vs LOAD, PFM, V_{OUT} = 5V, L_1 = 30µH

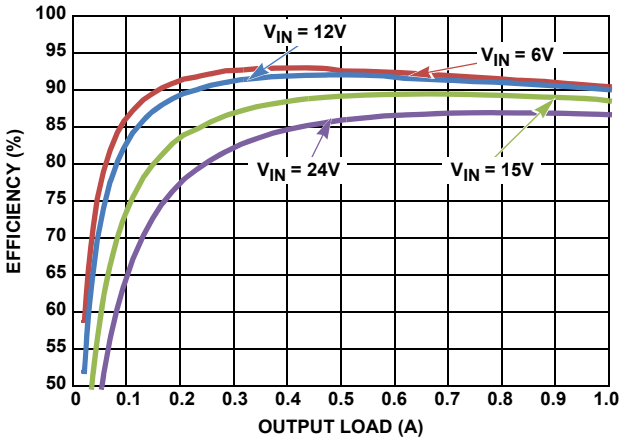


FIGURE 8. EFFICIENCY vs LOAD, PWM, V_{OUT} = 5V, L_1 = 30µH

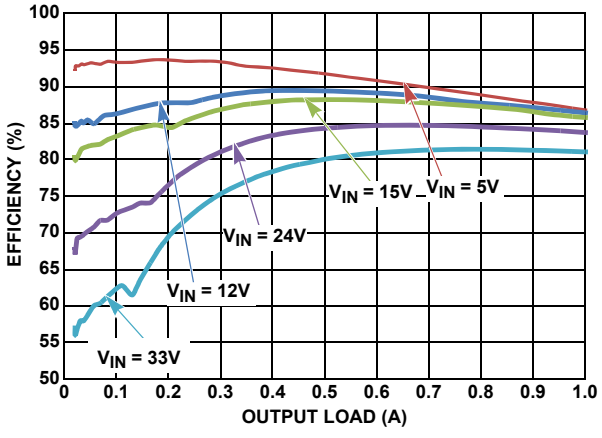


FIGURE 9. EFFICIENCY vs LOAD, PFM, V_{OUT} = 3.3V

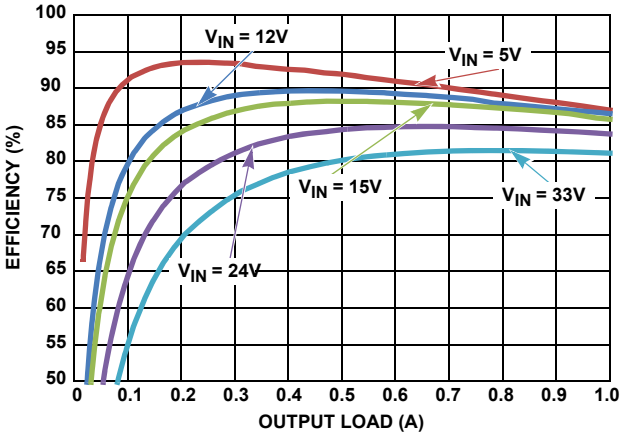


FIGURE 10. EFFICIENCY vs LOAD, PWM, V_{OUT} = 3.3V

Efficiency Curves f_{SW} = 500kHz, T_A = +25°C (Continued)

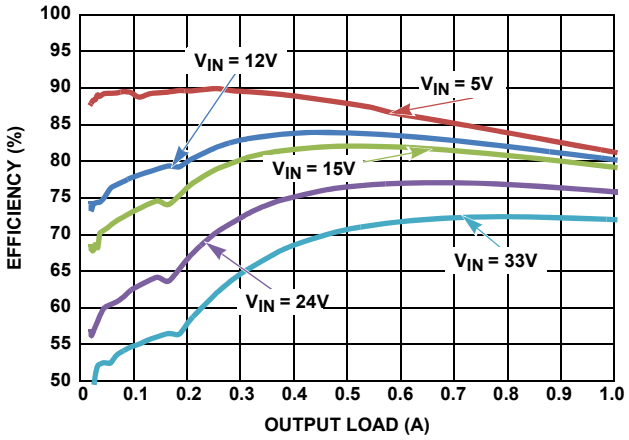


FIGURE 11. EFFICIENCY vs LOAD, PFM, V_{OUT} = 1.8V

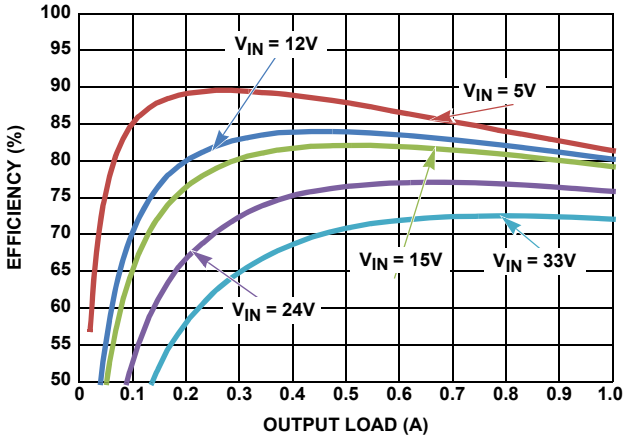


FIGURE 12. EFFICIENCY vs LOAD, PWM, V_{OUT} = 1.8V

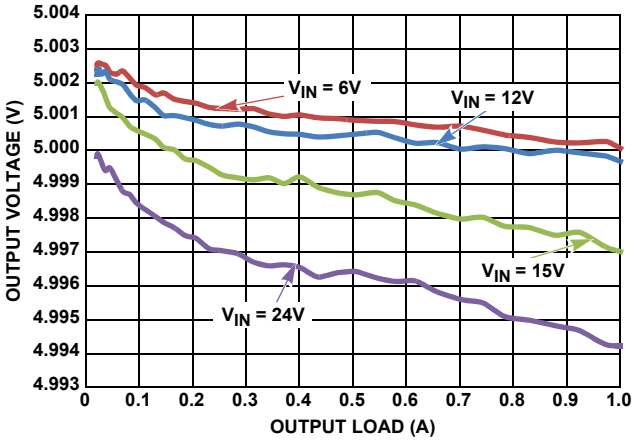


FIGURE 13. V_{OUT} REGULATION vs LOAD, PWM, V_{OUT} = 5V, L_1 = 30µH

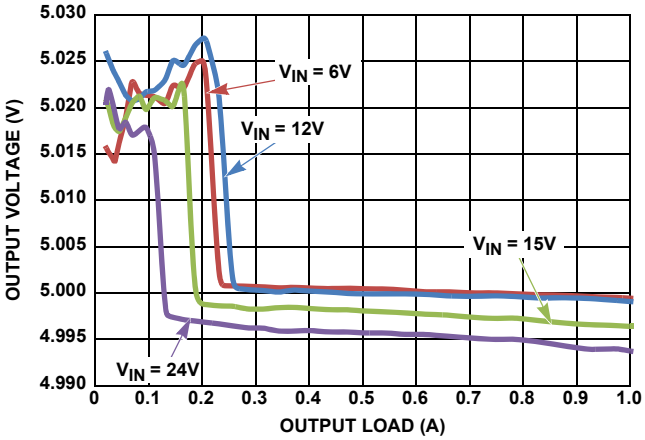


FIGURE 14. V_{OUT} REGULATION vs LOAD, PFM, V_{OUT} = 5V, L_1 = 30µH

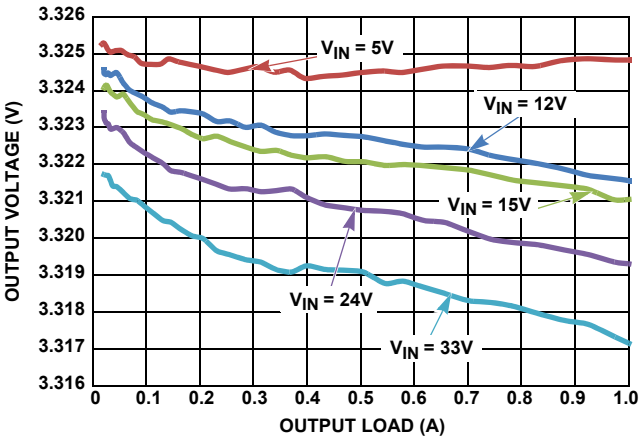


FIGURE 15. V_{OUT} REGULATION vs LOAD, PWM, V_{OUT} = 3.3V

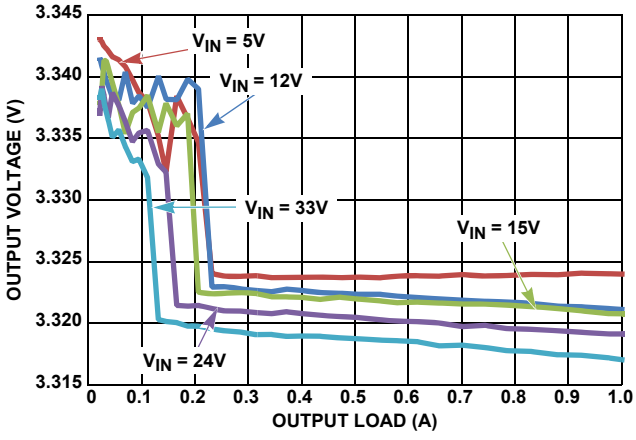


FIGURE 16. V_{OUT} REGULATION vs LOAD, PFM, V_{OUT} = 3.3V

Efficiency Curves f_{SW} = 500kHz, T_A = +25°C (Continued)

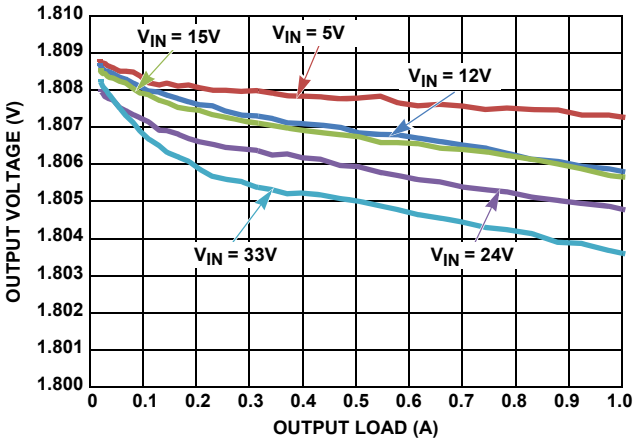


FIGURE 17. V_{OUT} REGULATION vs LOAD, PWM, V_{OUT} = 1.8V

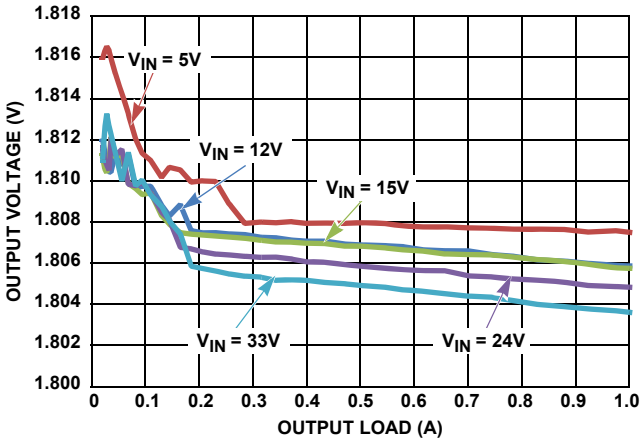


FIGURE 18. V_{OUT} REGULATION vs LOAD, PFM, V_{OUT} = 1.8V

Measurements f_{SW} = 500kHz, V_{IN} = 24V, V_{OUT} = 3.3V, T_A = +25°C

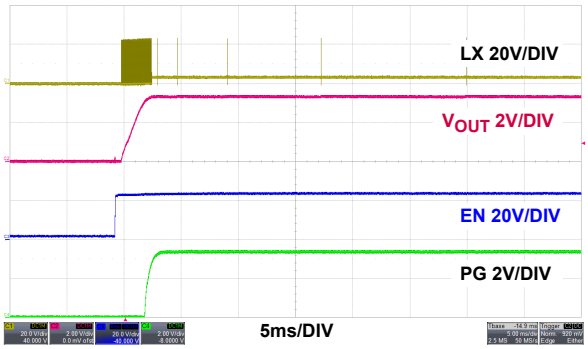


FIGURE 19. START-UP AT NO LOAD, PFM

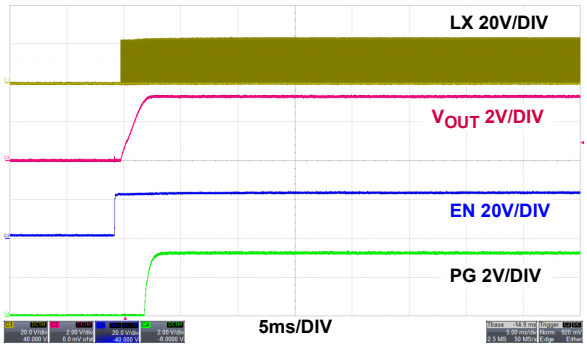


FIGURE 20. START-UP AT NO LOAD, PWM

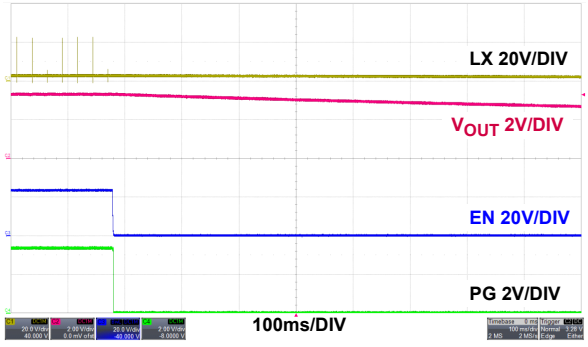


FIGURE 21. SHUTDOWN AT NO LOAD, PFM

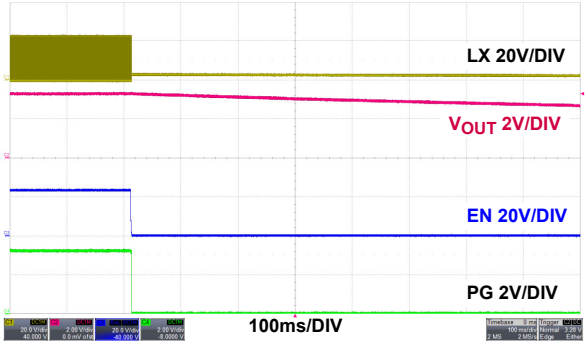


FIGURE 22. SHUTDOWN AT NO LOAD, PWM

Measurements f_{SW} = 500kHz, V_{IN} = 24V, V_{OUT} = 3.3V, T_A = +25°C (Continued)

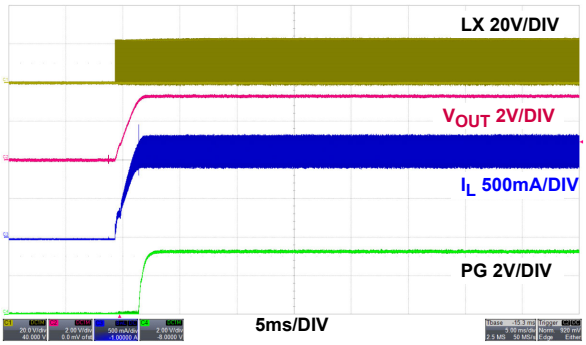


FIGURE 23. START-UP AT 1A, PWM

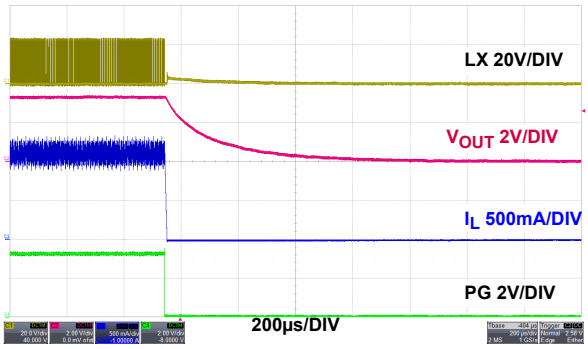


FIGURE 24. SHUTDOWN AT 1A, PWM

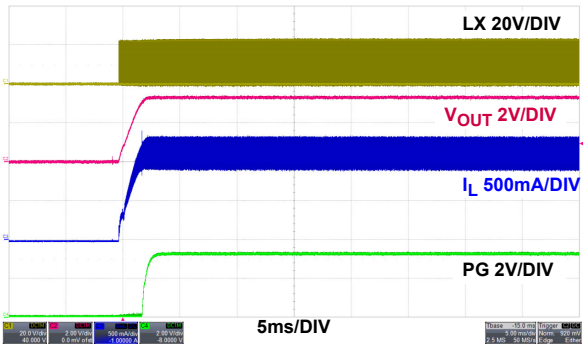


FIGURE 25. START-UP AT 1A, PFM

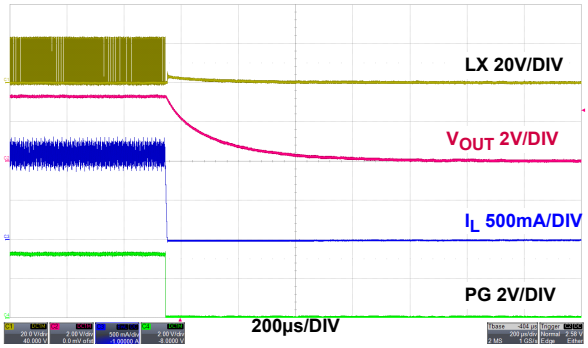


FIGURE 26. SHUTDOWN AT 1A, PFM

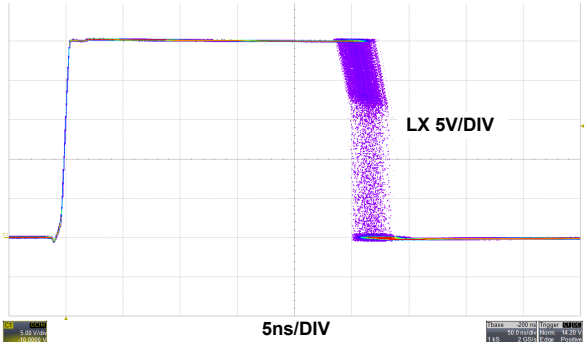


FIGURE 27. JITTER AT NO LOAD, PWM

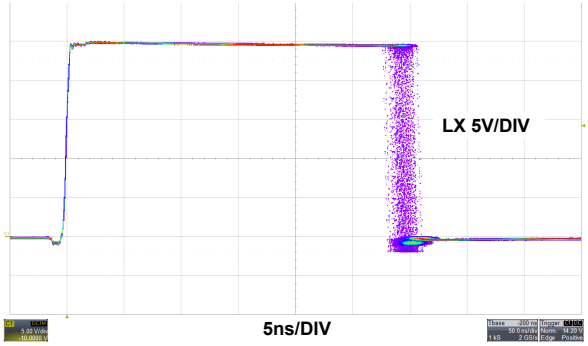


FIGURE 28. JITTER AT 1A LOAD, PWM

Measurements f_{SW} = 500kHz, V_{IN} = 24V, V_{OUT} = 3.3V, T_A = +25°C (Continued)

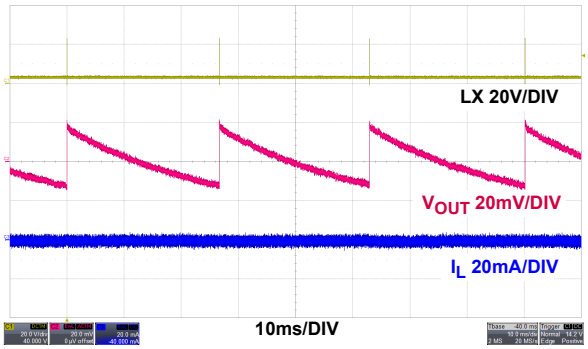


FIGURE 29. STEADY STATE AT NO LOAD, PFM

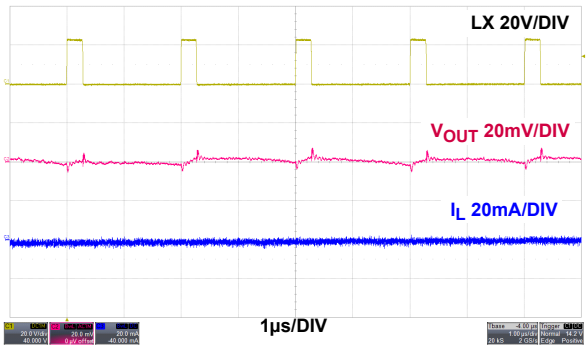


FIGURE 30. STEADY STATE AT NO LOAD, PWM

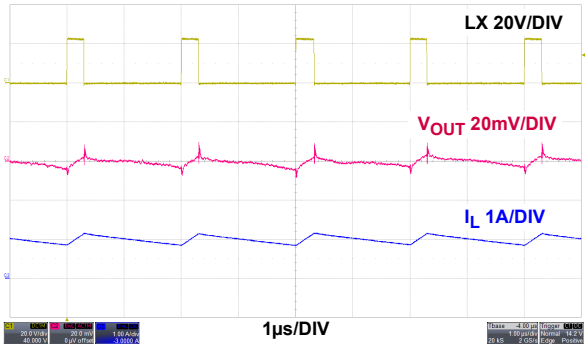


FIGURE 31. STEADY STATE AT 1A, PWM

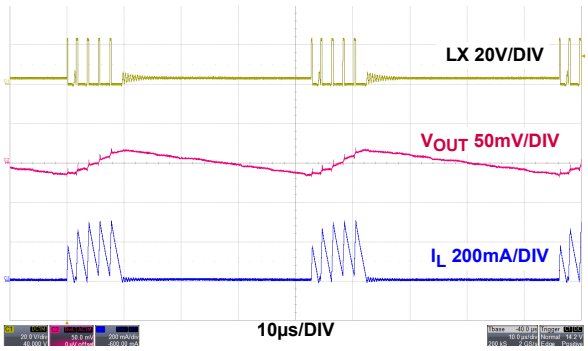


FIGURE 32. LIGHT LOAD OPERATION AT 20mA, PFM

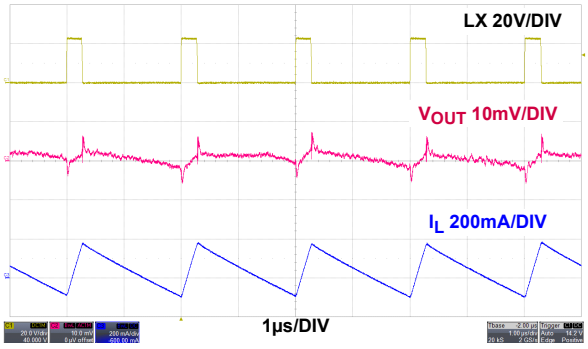


FIGURE 33. LIGHT LOAD OPERATION AT 20mA, PWM

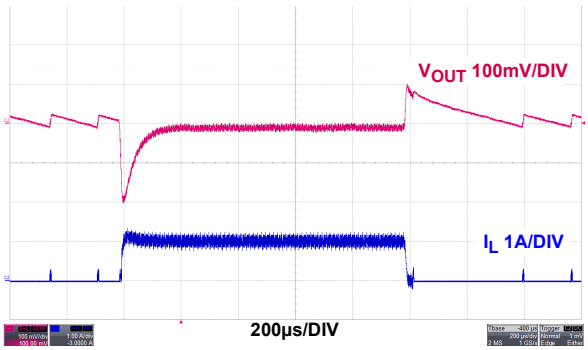


FIGURE 34. LOAD TRANSIENT, PFM

Measurements f_{SW} = 500kHz, V_{IN} = 24V, V_{OUT} = 3.3V, T_A = +25°C (Continued)

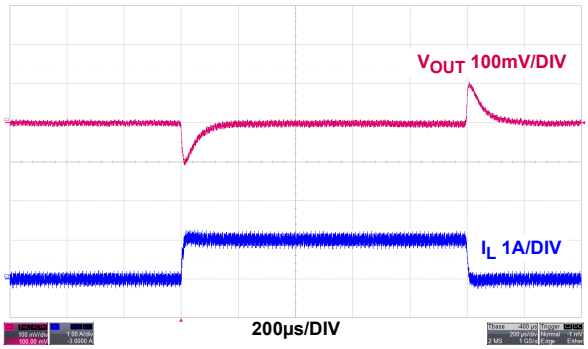


FIGURE 35. LOAD TRANSIENT, PWM

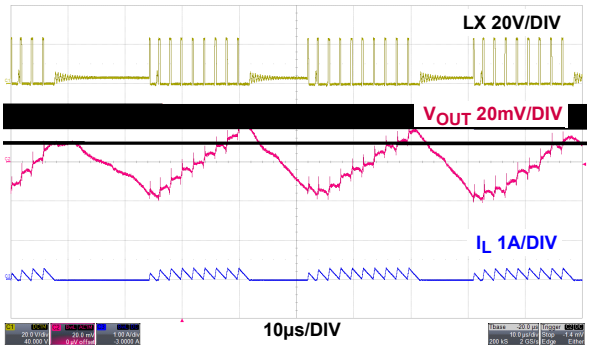


FIGURE 36. PFM TO PWM TRANSITION

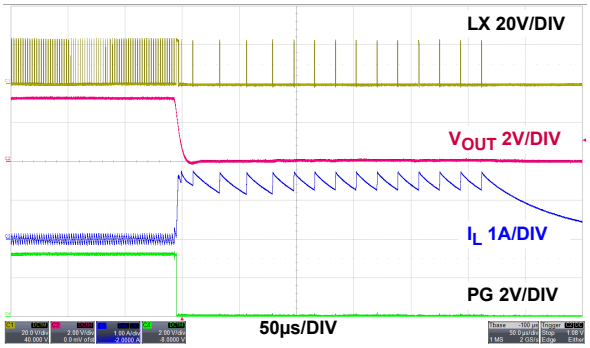


FIGURE 37. OVERCURRENT PROTECTION, PWM

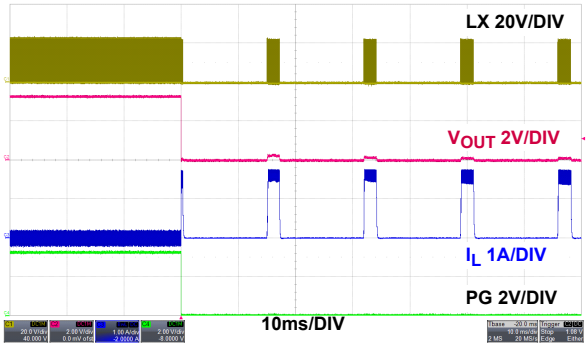


FIGURE 38. OVERCURRENT PROTECTION HICCUP, PWM

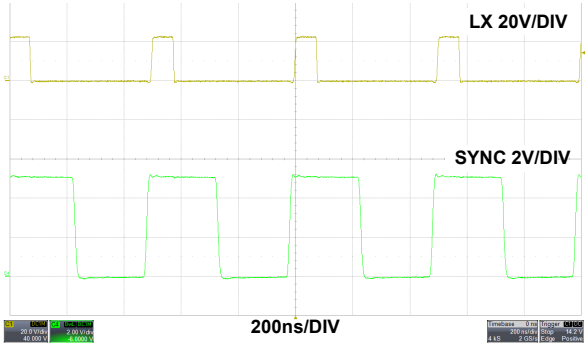


FIGURE 39. SYNC AT 1A LOAD, PWM

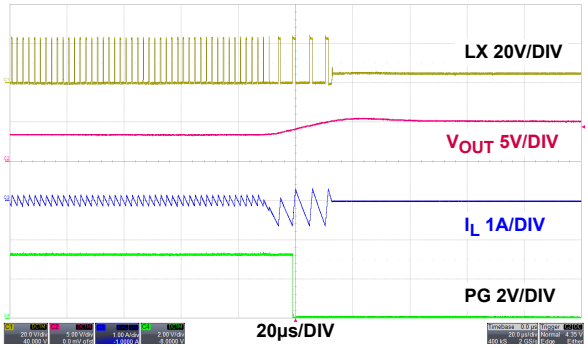


FIGURE 40. NEGATIVE CURRENT LIMIT, PWM

Measurements f_{SW} = 500kHz, V_{IN} = 24V, V_{OUT} = 3.3V, T_A = +25°C (Continued)

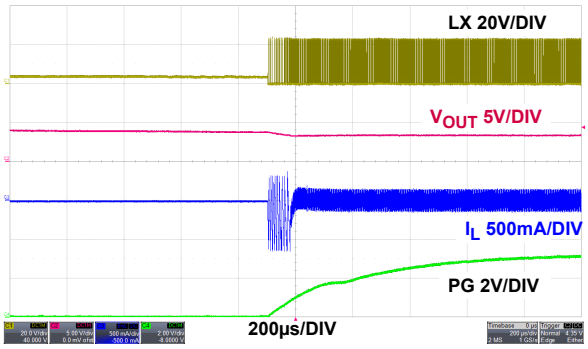


FIGURE 41. NEGATIVE CURRENT LIMIT RECOVERY, PWM

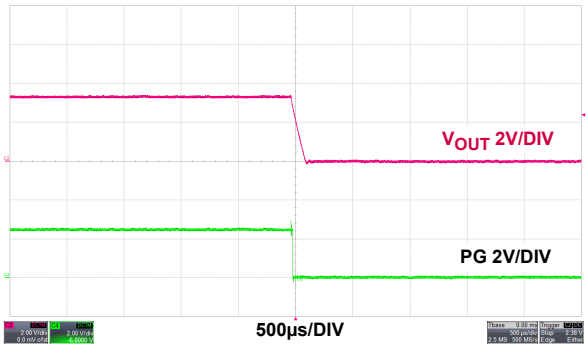


FIGURE 42. OVER-TEMPERATURE PROTECTION, PWM

Detailed Description

The ISL85410 combines a synchronous buck PWM controller with integrated power switches. The buck controller drives internal high-side and low-side N-channel MOSFETs to deliver load current up to 1A. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +3V to +40V. An internal LDO provides bias to the low voltage portions of the IC.

Peak current mode control is used to simplify feedback loop compensation and reject input voltage variation. User selectable internal feedback loop compensation further simplifies design. The ISL85410 switches at a default 500kHz.

The buck regulator is equipped with an internal current sensing circuit and the peak current limit threshold is typically set at 1.5A.

Power-On Reset

The ISL85410 automatically initializes upon receipt of the input power supply and continually monitors the EN pin state. If EN is held below its logic rising threshold, the IC is held in shutdown and consumes typically 2µA from the V_{IN} supply. If EN exceeds its logic rising threshold, the regulator enables the bias LDO and begins to monitor the VCC pin voltage. When the VCC pin voltage clears its rising POR threshold, the controller initializes the switching regulator circuits. If VCC never clears the rising POR threshold, the controller does not allow the switching regulator to operate. If VCC falls below its falling POR threshold while the switching regulator is operating, the switching regulator is shut down until VCC returns.

Soft-Start

To avoid large in-rush current, V_{OUT} is slowly increased at start-up to its final regulated value. Soft-start time is determined by the SS pin connection. If SS is pulled to VCC, an internal 2ms timer is selected for soft-start. For other soft-start times, connect a capacitor from SS to GND. In this case, a 5.5µA current pulls up the SS voltage and the FB pin follows this ramp until it reaches the 600mV reference level. The soft-start time for this case is described by Equation 1:

$$Time(ms) = C(nF)*0.109 \quad \text{(EQ. 1)}$$

Power-Good

PG is the open-drain output of a window comparator that continuously monitors the buck regulator output voltage vrom the FB pin. PG is actively held low when EN is low and during the buck regulator soft-start period. After the soft-start period completes, PG becomes high impedance if the FB pin is within the range specified in the “Electrical Specifications” on page 7. If FB exits the specified window, PG is pulled low until FB returns. Over-temperature faults also force PG low until the fault condition is cleared by an attempt to soft-start. There is an internal 5MΩ internal pull-up resistor.

PWM Control Scheme

The ISL85410 employs peak current-mode pulse-width modulation (PWM) control for fast transient response and pulse-by-pulse current limiting, as shown in the “Functional Block Diagram” on page 5. The current loop consists of the current sensing circuit, slope compensation ramp, PWM comparator, oscillator, and latch. Current sense trans-resistance is typically 500mV/A and slope compensation rate, Se, is typically 450mV/T where T is the switching cycle period. The control reference for the current loop comes from the error amplifier’s output (V_{COMP}).

A PWM cycle begins when a clock pulse sets the PWM latch and the upper FET is turned on. Current begins to ramp up in the upper FET and inductor. This current is sensed (V_{CSA}), converted to a voltage and summed with the slope compensation signal. This combined signal is compared to V_{COMP} and when the signal is equal to V_{COMP}, the latch is reset. Upon latch reset, the upper FET is turned off and the lower FET turned on allowing current to ramp down in the inductor. The lower FET remains on until the clock initiates another PWM cycle. Figure 44 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the current sense and slope compensation signal.

Output voltage is regulated as the error amplifier varies VCOMP and therefore varies the output inductor current. The error amplifier is a transconductance type and its output (COMP) is terminated with a series RC network to GND. This termination is internal (150k/54pF) if the COMP pin is tied to VCC. Additionally, the transconductance for COMP = VCC is 50µA/V vs 230µA/V for external RC connection. Its noninverting input is internally connected to a 600mV reference voltage and its inverting input is connected to the output voltage from the FB pin and its associated divider network.

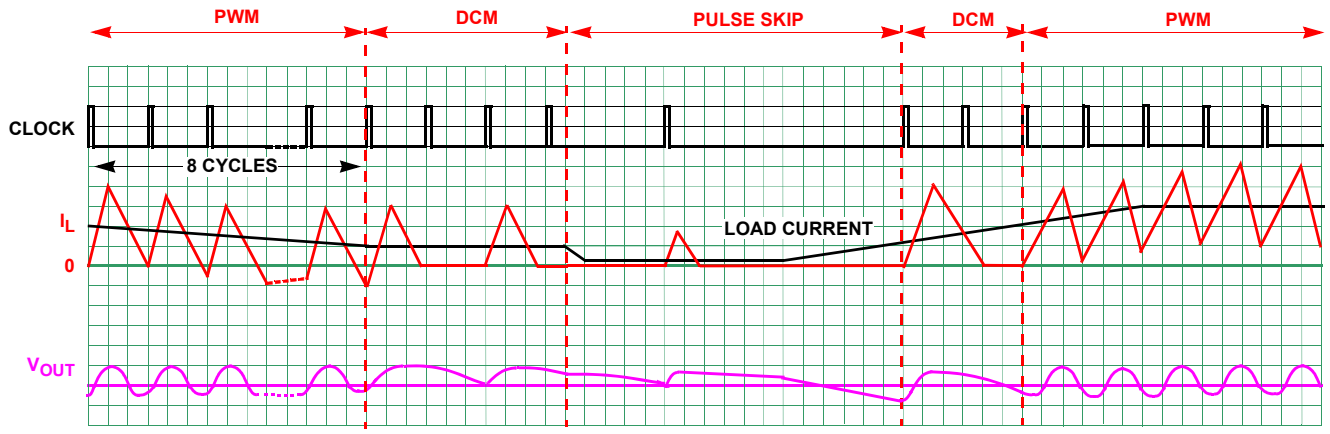


FIGURE 43. DCM MODE OPERATION WAVEFORMS

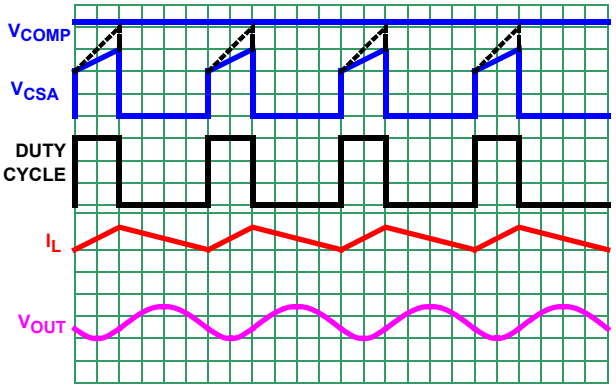


FIGURE 44. PWM OPERATION WAVEFORMS

Light Load Operation

At light loads, converter efficiency can be improved by enabling variable frequency operation (PFM). Connecting the SYNC pin to GND allows the controller to choose such operation automatically when the load current is low. Figure 43 shows the DCM operation. The IC enters DCM mode when eight consecutive cycles of inductor current crossing zero are detected. This corresponds to a load current equal to 1/2 the peak-to-peak inductor ripple current and set by Equation 2:

$$I_{OUT} = \frac{V_{OUT}(1-D)}{2Lf_{SW}} \quad \text{(EQ. 2)}$$

where D = duty cycle, f_{SW} = switching frequency, L = inductor value, I_{OUT} = output loading current, V_{OUT} = output voltage.

While operating in PFM mode, the regulator controls the output voltage with a simple comparator and pulsed FET current. A comparator indicates the point at which FB is equal to the 600mV reference, at which time the regulator begins providing pulses of current until FB is moved above the 600mV reference by 1%. The current pulses are approximately 400mA and are issued at a frequency equal to the converter's programmed PWM operating frequency.

Due to the pulsed current nature of PFM mode, the converter can supply limited current to the load. If load current rises beyond the limit, V_{OUT} begins to decline. A second comparator signals an FB voltage 2% lower than the 600mV reference and forces the converter to return to PWM operation.

Output Voltage Selection

The regulator output voltage is programmed using an external resistor divider to scale V_{OUT} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; see Figure 45.

The output voltage programming resistor, R_3, depends on the value chosen for the feedback resistor, R_2, and the needed output voltage, V_{OUT}, of the regulator. Equation 3 describes the relationship between V_{OUT} and resistor values.

$$R_3 = \frac{R_2 x 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 3)}$$

If the needed output voltage is 0.6V, then R_3 is left unpopulated and R_2 is 0Ω.

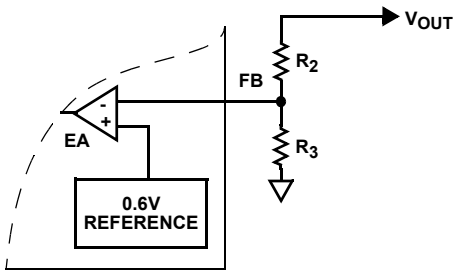


FIGURE 45. EXTERNAL RESISTOR DIVIDER

Protection Features

The ISL85410 is protected from overcurrent, negative overcurrent and over-temperature. The protection circuits operate automatically.

Overcurrent Protection

During PWM on-time, current through the upper FET is monitored and compared to a nominal 1.5A peak overcurrent limit. If current reaches the limit, the upper FET is turned off until the

next switching cycle. In this way, FET peak current is always well limited.

If the overcurrent condition persists for 17 sequential clock cycles, the regulator begins its hiccup sequence. In this case, both FETs are turned off and PG is pulled low. This condition is maintained for eight soft-start periods, after which the regulator attempts a normal soft-start.

If output fault persists, the regulator repeats the hiccup sequence indefinitely. There is no danger even if the output is shorted during soft-start.

If V_{OUT} is shorted very quickly, FB may collapse below $5/8^{ths}$ of its target value before 17 cycles of overcurrent are detected. The ISL85410 recognizes this condition and begins to lower its switching frequency proportional to the FB pin voltage. This adjustment ensures that the inductor current does not run away under any circumstance (even with VOUT near 0V).

Negative Current Limit

If an external source somehow drives current into V_{OUT}, the controller attempts to regulate V_{OUT} by reversing its inductor current to absorb the externally sourced current. If the external source is low impedance, the current may be reversed to unacceptable levels and the controller initiates its negative current limit protection. Similar to normal overcurrent, the negative current protection is realized by monitoring the current through the lower FET. When the valley point of the inductor current reaches negative current limit, the lower FET is turned off and the upper FET is forced on until current reaches the **POSITIVE** current limit or an internal clock signal is issued. Next, the lower FET is allowed to operate. If the current is pulled to the negative limit again on the next cycle, the upper FET is forced on again and the current is forced to $1/6^{th}$ of the positive current limit. Next, the controller turns off both FETs and waits for COMP to indicate a return to normal operation. During this time, the controller applies a 100Ω load from PHASE to PGND and attempts to discharge the output. Negative current limit is a pulse-by-pulse style operation and recovery is automatic.

Over-Temperature Protection

Over-temperature protection limits maximum junction temperature in the ISL85410. When junction temperature (T_J) exceeds +150°C, both FETs are turned off and the controller waits for temperature to decrease by approximately 20°C. During this time PG is pulled low. When temperature is within an acceptable range, the controller initiates a normal soft-start sequence. For continuous operation, do not exceed the +125°C junction temperature rating.

Boot Undervoltage Protection

If the boot capacitor voltage falls below 1.8V, the boot undervoltage protection circuit turns on the lower FET for 400ns to recharge the capacitor. This operation may arise during long periods of no switching such as PFM no load situations. In PWM operation near dropout (V_{IN} near V_{OUT}), the regulator can hold the upper FET on for multiple clock cycles. To prevent the boot capacitor from discharging, the lower FET is forced on for approximately 200ns every 10 clock cycles.

Application Guidelines

Simplifying the Design

While the ISL85410 offers user programmed options for most parameters, the easiest implementation with fewest components involves selecting internal settings for SS, COMP, and FS. Table 1 on page 4 provides component value selections for a variety of output voltages and allows you to implement solutions with a minimum of effort.

Operating Frequency

The ISL85410 operates at a default switching frequency of 500kHz if the FS pin is tied to V_{CC}. Tie a resistor from the FS pin to GND to program the switching frequency from 300kHz to 2MHz, as shown in Equation 4.

$$R_{FS}[k\Omega] = 108.75k\Omega * (t - 0.2\mu s)/1\mu s \quad \text{(EQ. 4)}$$

Where:

t is the switching period in µs.

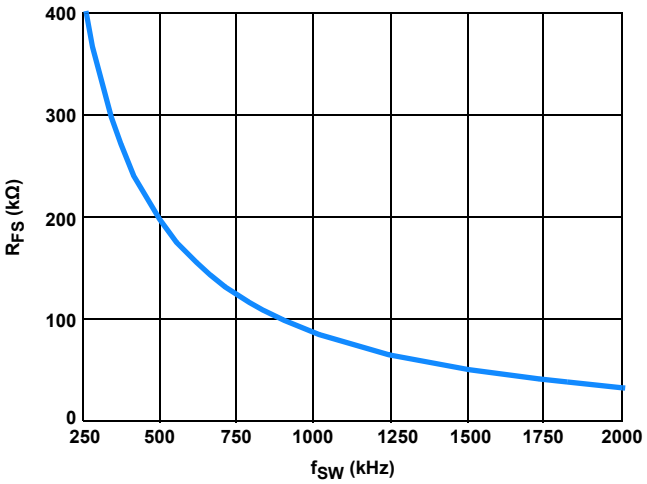


FIGURE 46. R_{FS} SELECTION vs f_{SW}

Minimum On/Off-Time Limitation

Minimum on-time (t_{MIN_ON}) is the shortest duration of time that the HS FET can be turned on and minimum off time (t_{MIN_OFF}) is the shortest duration of time that the HS FET can be turned off. The typical t_{MIN_ON} is 90ns and the typical t_{MIN_OFF} is 150ns. For a given t_{MIN_ON} and t_{MIN_OFF}, a higher switching frequency results in a narrower range of allowed duty cycle, which translates to a smaller allowed V_{IN} range.

For a given output voltage (V_{OUT}) and switching frequency (f_{SW}), the maximum allowed voltage is given by (Equation 5):

$$V_{IN(max)} = \frac{V_{OUT}}{f_{SW} \times t_{MIN_ON}} \quad \text{(EQ. 5)}$$

The minimum allowed voltage is given by (Equation 6):

$$V_{IN(min)} = \frac{V_{OUT}}{1 - f_{SW} \times t_{MIN_OFF}} \quad \text{(EQ. 6)}$$

Table 2 shows the recommended switching frequencies for the various V_{OUT} to operate up to the maximum V_{IN} (40V).

TABLE 2. RECOMMENDED SWITCHING FREQUENCIES FOR VARIOUS V_{OUT}

$V_{IN\ (max)}$ (V)	V_{OUT} (V)	f_{SW} (kHz)
40	5	500
40	3.3	500
40	2.5	500
40	1.8	300

Synchronization Control

The frequency of operation can be synchronized up to 2MHz by an external signal applied to the SYNC pin. The rising edge on the SYNC triggers the rising edge of PHASE. To properly sync, the external source must be at least 10% greater than the programmed free running IC frequency.

Output Inductor Selection

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% of total load current. The inductor value can then be calculated using Equation 7:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 7)}$$

Increasing the value of inductance reduces the ripple current and thus, the ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be such that it does not saturate in overcurrent conditions. For typical ISL85410 applications, inductor values generally lie in the 10µH to 47µH range. In general, higher V_{OUT} causes higher inductance.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current. The current mode control loop allows the use of low ESR ceramic capacitors and thus supports very small circuit implementations on the PC board. Electrolytic and polymer capacitors can also be used.

While ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturer's datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction generally suffices. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. Nonetheless, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

Use the following equations to calculate the required capacitance for ripple voltage. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * f_{SW} * C_{OUT}} \quad \text{(EQ. 8)}$$

where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors,

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 9)}$$

Loop Compensation Design

When COMP is not connected to VCC, the COMP pin is active for external loop compensation. The ISL85410 uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 47 shows the small signal model of the synchronous buck regulator.

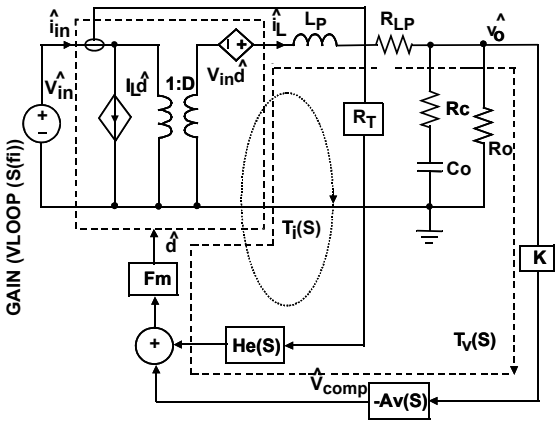


FIGURE 47. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

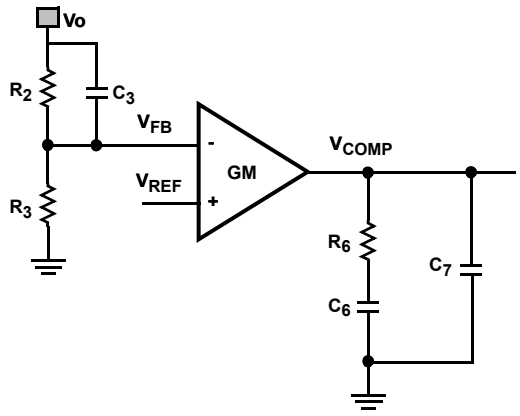


FIGURE 48. TYPE II COMPENSATOR

Figure 48 shows the type II compensator and its transfer function is expressed as shown in Equation 10:

$$A_V(S) = \frac{\hat{v}_{COMP}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 10)}$$

where;

$$\omega_{cz1} = \frac{1}{R_6 C_6},\ \omega_{cz2} = \frac{1}{R_2 C_3},\ \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7},\ \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

- High DC gain
- Choose loop bandwidth f_c less than 100kHz
- Gain margin: >10dB
- Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 11.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 22.75 \times 10^3 \cdot f_c V_o C_o \quad \text{(EQ. 11)}$$

where GM is the transconductance, g_m, of the voltage error amplifier in each phase. Compensator capacitor C_6 is then given by Equation 12.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_{SW} R_6}\right) \quad \text{(EQ. 12)}$$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 12. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

Put compensator zero 2 to 5 times f_c.

$$C_3 = \frac{1}{\pi f_c R_2} \quad \text{(EQ. 13)}$$

Example: V_{IN} = 12V, V_O = 5V, I_O = 1A, f_{SW} = 500kHz, R_2 = 90.9kΩ, C_o = 22µF/5mΩ, L = 39µH, f_c = 50kHz, then compensator resistance R_6:

$$R_6 = 22.75 \times 10^3 \cdot 50kHz \cdot 5V \cdot 22\mu F = 125.12k\Omega \quad \text{(EQ. 14)}$$

It is acceptable to use 124kΩ as the closest standard value for R_6.

$$C_6 = \frac{5V \cdot 22\mu F}{1A \cdot 124k\Omega} = 0.88nF \quad \text{(EQ. 15)}$$

$$C_7 = \max\left(\frac{5m\Omega \cdot 22\mu F}{124k\Omega}, \frac{1}{\pi \cdot 500kHz \cdot 124k\Omega}\right) = (0.88pF, 5.1pF) \quad \text{(EQ. 16)}$$

It is also acceptable to use the closest standard values for C_6 and C_7. There is approximately 3pF parasitic capacitance from V_{COMP} to GND; Therefore, C_7 is optional. Use C_6 = 1500pF and C_7 = OPEN.

$$C_3 = \frac{1}{\pi \cdot 50kHz \cdot 90.9k\Omega} = 70pF \quad \text{(EQ. 17)}$$

Use C_3 = 68pF. Note that C_3 may increase the loop bandwidth from previous estimated value. Figure 49, on page 19 shows the simulated voltage loop gain. It is shown that it has a 75kHz loop bandwidth with a 61° phase margin and 6dB gain margin. It may be more desirable to achieve an increased gain margin., which can be accomplished by lowering R_6 by 20% to 30%. In practice, ceramic capacitors have significant derating on voltage and temperature, depending on the type. See the ceramic capacitor datasheet for more details.

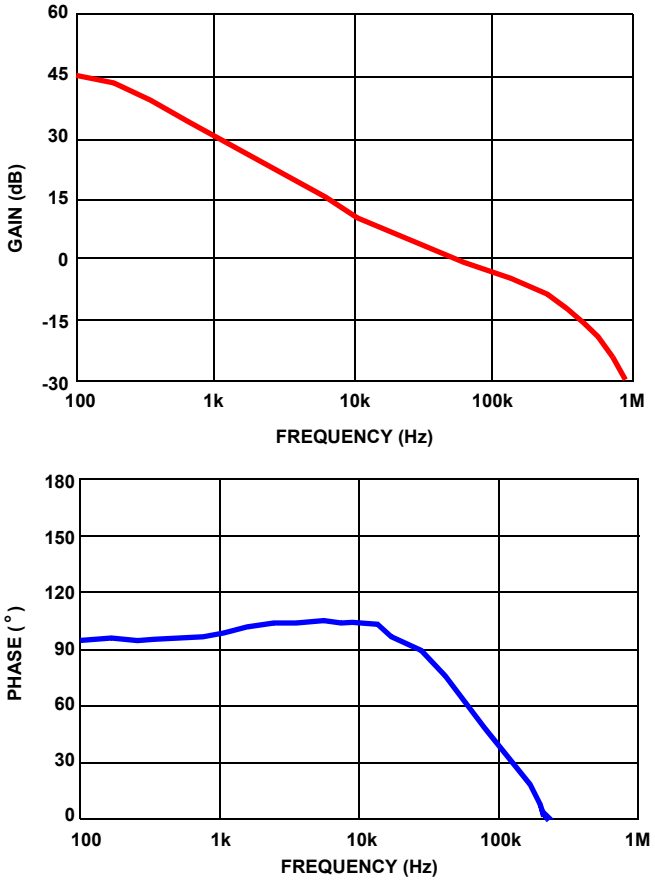


FIGURE 49. SIMULATED LOOP GAIN

Layout Considerations

Proper layout of the power converter minimizes EMI and noise and ensures first pass success of the design. Printed Circuit Board (PCB) layouts are provided in multiple formats on the Renesas website. In addition, Figure 50 illustrates the important points in PCB layout. In reality, PCB layout of the ISL85410 is quite simple.

A multilayer PCB with GND plane is recommended. Figure 50 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} can each represent multiple physical capacitors. The most critical connections are to tie the PGND pin to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane ensures a low impedance path for all return current and an excellent thermal path to dissipate heat. With this connection made, place the high frequency MLCC input capacitor near the VIN pin and use vias directly at the capacitor pad to tie the capacitor to the system GND plane.

The boot capacitor is easily placed on the PCB side opposite the controller IC and two vias directly connect the capacitor to BOOT and PHASE.

Place a 1µF MLCC near the VCC pin and directly connect its return with a via to the system GND plane.

Place the feedback divider close to the FB pin and do not route any feedback components near PHASE or BOOT. If external components are used for SS, COMP, or FS, the same advice applies.

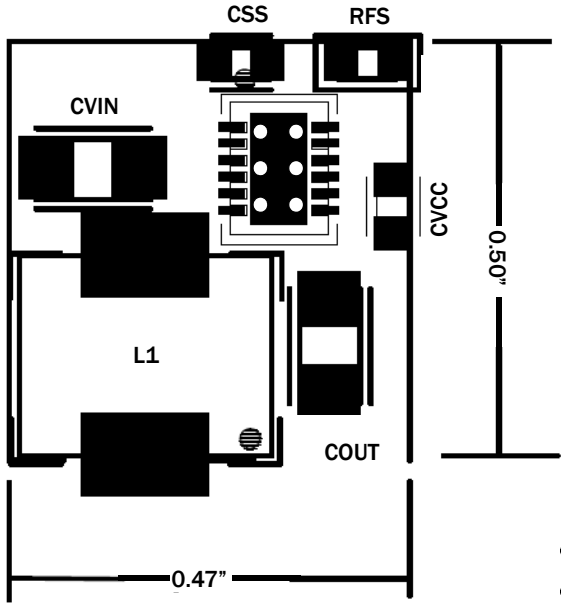


FIGURE 50. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Mar 15, 2019	FN8375.8	Updated links throughout document. Updated Related Literature section Updated the Ordering Information table by adding tape and reel parts, demo board, and updated notes. Under Light Load Operation section changed 300mA to 400mA and 1% to 2%. Added Minimum On/Off-Time Limitation section. Removed About Intersil section. Updated Disclaimer. Updated POD L12.4x3 to the latest version changes are as follows: Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
Mar 13, 2015	FN8375.7	On page 1, updated all 36V references to 40V and replaced Figure 2. On page 6, under “Absolute Maximum Ratings” for VIN to GND updated max from “+42V” to “+43V” for PHASE to GND updated max from “43V” to “+44V” for EN to GND updated max from “+42V” to “+43V” Under “Recommended Operating Conditions” updated supply voltage max from “36V” to “+40V”. In “Electrical Specifications” updated all occurrences of VIN value from “36V” to “40V”. Replaced Figure 9, on page 8. On page 14, under “Detailed Description” section updated voltage range max from “+36V” to “+40V”.
Aug 28, 2014	FN8375.6	POD changed from L12.3x4 back to original L12.4x3.
Jul 24, 2014	FN8375.5	Changed title of Figure 13, on page 9 from “Efficiency vs Load, PWM, V_{OUT} = 5V, L_1 = 30µH” to “V_{OUT} Regulation vs Load, PWM, V_{OUT} = 5V, L_1 = 30µH”. Replaced Figure Figure 46, on page 16. Updated POD from L12.4x3 to L12.3x4
Feb 25, 2014	FN8375.4	“Power-On Reset” on page 14 changed 10µA to 2µA.
Jan 17, 2014	FN8375.3	“Functional Block Diagram” on page 5 changed Internal=50µs, External=230µs to Internal=50µA/V, External=230µA/V and 600mA/Amp to 500mV/A “Detailed Description” on page 14 changed 0.9A to 1.5A “Power-On Reset” on page 14 changed 1µA to 10µA “PWM Control Scheme” on page 14 changed in last paragraph 50µs vs 220µs to 50µA/V vs 230µA/V and 600mA/Amp to 500mV/A in 1st paragraph “Overcurrent Protection” on page 15 changed 0.9A to 1.5A
Nov 22, 2013	FN8375.2	Initial Release.

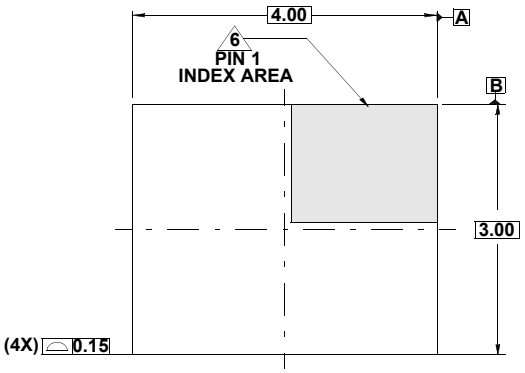
Package Outline Drawing

For the most recent package outline drawing, see L12.4x3.

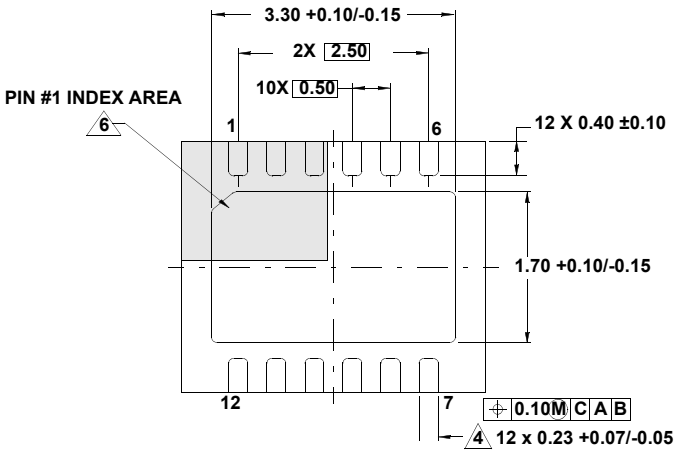
L12.4x3

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

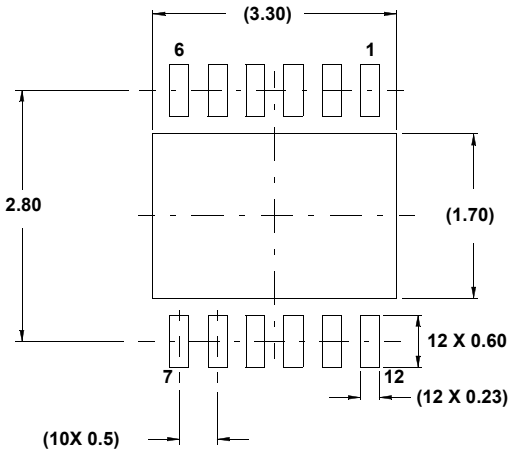
Rev 3, 3/15



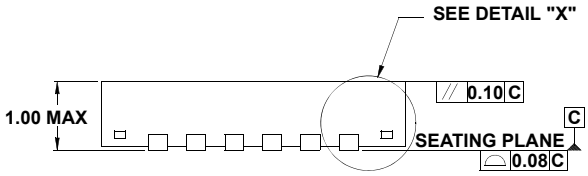
TOP VIEW



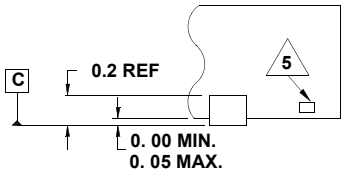
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 V4030D-4 issue E.

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