# M27W1282

## 128 Mbit (two 64 Mbit, x16, FlexibleROM™) 3V Supply, Multiple Memory Product

**FEATURES SUMMARY**

- ONE TIME PROGRAMMABLE
- TWO 64 Mbit FlexibleROM™ MEMORIES STACKED IN A SINGLE PACKAGE
- SUPPLY VOLTAGE
  - $V_{CC}$ = 2.7 to 3.6V for Read
  - $V_{PP}$ = 11.4 to 12.6V for Program
- ACCESS TIME
  - 90ns at $V_{CC}$ = 3.0 to 3.6V
  - 100, 120ns at $V_{CC}$ = 2.7 to 3.6V
- PROGRAMMING TIME
  - 9µs per Word typical
  - Multiple Word Programming Option (16s typical Chip Program)
- SUITABLE FOR ON-BOARD PROGRAMMING
- PROGRAM CONTROLLER
  - Embedded Word Program algorithms
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code : 8888h

**Figure 1. Packages**



SO44 (M)

**TABLE OF CONTENTS**

## SUMMARY DESCRIPTION

The M27W1282 is a 128 Mbit (8Mb x16) non-volatile, One Time Programmable (OTP), FlexibleROM™ Memory. Read operations can be performed using a single low voltage (2.7 to 3.6V) supply. Program operations require an additional $V_{PP}$ (11.4 to 12.6V) power supply. On power-up the memory defaults to Read mode where it can be read in the same way as a ROM or EPROM.

The Mask-ROM compatibility is obtained using a dual function Address/Voltage Supply pin (A22/$V_{PP}$). In Read mode the A22/$V_{PP}$ pin works as an address pin; in Program mode it also works as a voltage supply pin. At the beginning of any program operation, a specific procedure (see Figure 4) must be performed to internally memorize the A22 value that will be used during the program operation.

Program commands are written to the Command Interface of the memory. An on-chip Program Controller (PC) simplifies the process of programming the memory by taking care of all of the special operations that are required to update the memory contents.

The device is composed of two 64Mbit memories assembled side by side in a single package. Recommended operating conditions do not allow both memories to be active at the same time. Address A22 selects the memory to be enabled. The other memory is in Standby mode.

In Read mode the A22 pin works as an address pin: A22 at $V_{IH}$ selects the Top die; A22 at $V_{IL}$ selectrs the Bottom die. At the beginning of any program operation, a specific procedure (see Figure 4) must be performed to internally memorize the A22 value that will be used during the program operation.

The M27W1282 features an innovative command, Multiple Word Program, used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written to the memory at any one time. Using this command the entire memory can be programmed in 8s, compared to 36s using the standard Word Program.

The end of a program operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable and Output Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in SO44 package and is supplied with all the bits set to '1'.

**Figure 2. Logic Diagram**



AI08220
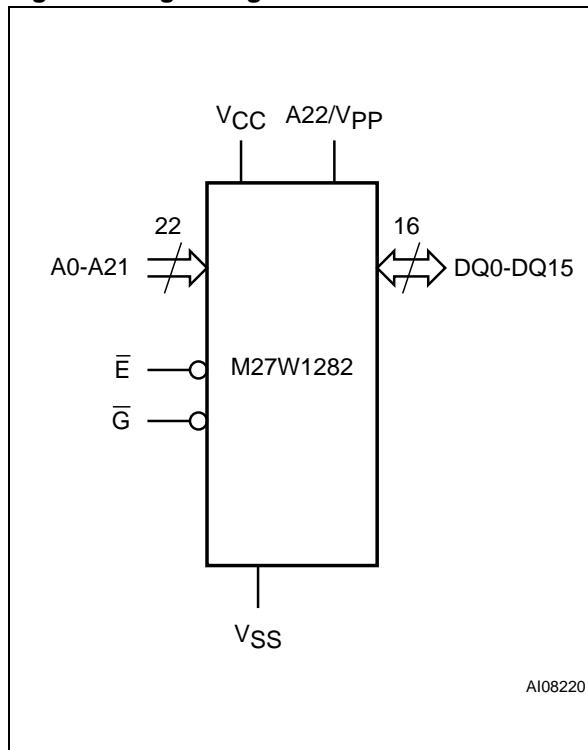
**Table 1. Signal Names**

| A0-A21 | Address Inputs |
|---|---|
| A22/$V_{PP}$ | Address Input/Supply Voltage for Program |
| DQ0-DQ15 | Data Inputs/Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $V_{CC}$ | Supply Voltage read |
| $V_{SS}$ | Ground |

**Figure 3. SO Connections**

| | | | | |
|---|---|---|---|---|
| A21 | 1 | | 44 | A20 |
| A18 | 2 | | 43 | A19 |
| A17 | 3 | | 42 | A8 |
| A7 | 4 | | 41 | A9 |
| A6 | 5 | | 40 | A10 |
| A5 | 6 | | 39 | A11 |
| A4 | 7 | | 38 | A12 |
| A3 | 8 | | 37 | A13 |
| A2 | 9 | | 36 | A14 |
| A1 | 10 | | 35 | A15 |
| A0 | 11 | M27W1282 | 34 | A16 |
| $\overline{E}$ | 12 | | 33 | A22/$V_{PP}$ |
| $V_{SS}$ | 13 | | 32 | $V_{SS}$ |
| $\overline{G}$ | 14 | | 31 | DQ15 |
| DQ0 | 15 | | 30 | DQ7 |
| DQ8 | 16 | | 29 | DQ14 |
| DQ1 | 17 | | 28 | DQ6 |
| DQ9 | 18 | | 27 | DQ13 |
| DQ2 | 19 | | 26 | DQ5 |
| DQ10 | 20 | | 25 | DQ12 |
| DQ3 | 21 | | 24 | DQ4 |
| DQ11 | 22 | | 23 | $V_{CC}$ |

AI08221
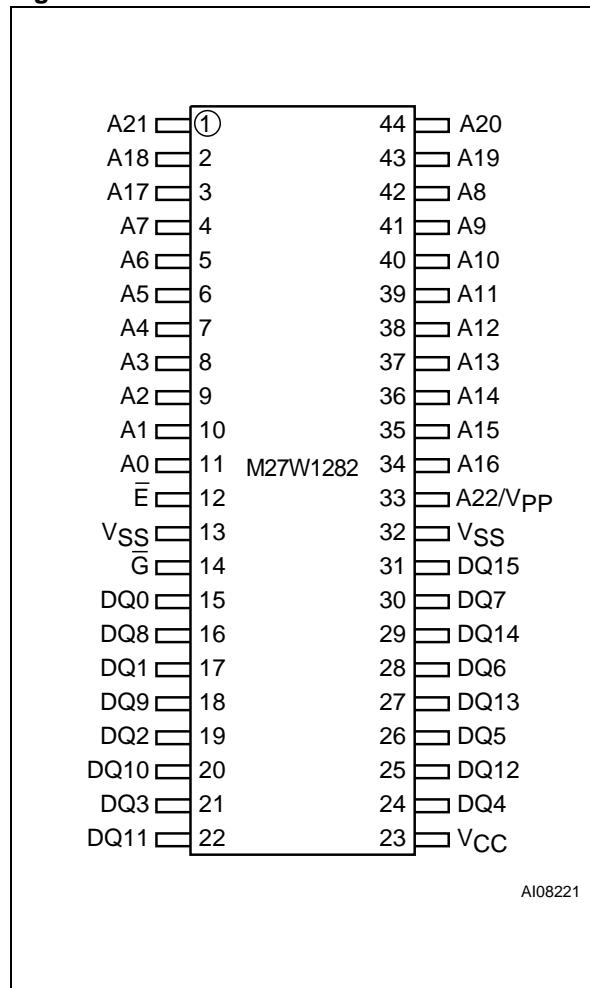
## SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

**Address Inputs (A0-A21).** The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program Controller.

**Address/Voltage Supply (A22/V$_{PP}$).** The A22/V$_{PP}$ signal has two functions.

During read operations the A22/V$_{PP}$ signal works as an address input, which is used to select the Top (A22 = V$_{IH}$) or Bottom (A22 = V$_{IL}$) die.

During program operations it also works as a V$_{PP}$ voltage supply pin. At the beginning of any program operation, a specific procedure (see Figure 4) must be performed to internally memorize the A22 value that will be used during the program operation.

When the V$_{PP}$ is in the V$_{HH}$ range (see Table 11, DC Characteristic, for the relevant values) program operations are enabled. During such operations V$_{PP}$ must be stable in the V$_{HH}$ range. Program operation are not allowed when V$_{PP}$ is below the V$_{HH}$ range.

**Data Inputs/Outputs (DQ0-DQ7).** The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the command sent to the Command Interface of the Program Controller. When reading the Status Register they report the status of the ongoing algorithm.

**Data Inputs/Outputs (DQ8-DQ15).** The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations the Command Interface does not use these bits. When reading the Status Register these bits should be ignored.

**Chip Enable ($\overline{E}$).** The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read operations to be performed. It also controls the Bus Write operations, when V$_{PP}$ is in the V$_{HH}$ range.

**Output Enable ($\overline{G}$).** The Output Enable, $\overline{G}$, controls the Bus Read operations of the memory. It also allows Bus Write operations, when V$_{PP}$ is in the V$_{HH}$ range.

**V$_{CC}$ Supply Voltage.** The V$_{CC}$ Supply Voltage supplies the power for Read operations.

A 0.1µF capacitor should be connected between the V$_{CC}$ Supply Voltage pin and the V$_{SS}$ Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program operations, I$_{CC3}$.

**Vss Ground.** The V$_{SS}$ Ground is the reference for all voltage measurements.

## BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Electronic Signature. See Table 2, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

**Bus Read.** Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs and applying a Low signal, $V_{IL}$, to Chip Enable and Output Enable. The Data Inputs/Outputs will output the value, see Figure 11, Read AC Waveforms, and Table 12, Read AC Characteristics, for details of when the output becomes valid.

**Bus Write.** Bus Write operations write to the Command Interface. Bus Write is enabled only when $V_{PP}$ is set to $V_{HH}$. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable. Output Enable must remain High, $V_{IH}$, during the whole Bus Write operation. See Figure 12, Write AC Waveforms, and Table 13, Write AC Characteristics, for details of the timing requirements.

**Output Disable.** The Data Inputs/Outputs are in the high impedance state when Output Enable is High, $V_{IH}$.

**Standby.** When Chip Enable is High, $V_{IH}$, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, $I_{CC2}$, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 11, DC Characteristics.

During program operation the memory will continue to use the Program Supply Current, $I_{CC3}$, for Program operation until the operation completes.

**Automatic Standby.** If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, $I_{CC2}$. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

**Electronic Signature.** The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Table 2, Bus Operations, once the Auto Select Command is executed. To exit Electronic Signature mode, the Read/Reset command must be issued.

**Table 2. Bus Operations**

| Operation | $\overline{E}$ | $\overline{G}$ | A22/V$_{PP}$(2) | Address Inputs A0-A21 | Data Inputs/Outputs DQ15-DQ0 |
|---|---|---|---|---|---|
| Bus Read | $V_{IL}$ | $V_{IL}$ | $V_{IL}/V_{IH}$(3) | Cell Address | Data Output |
| Bus Write | $V_{IL}$ | $V_{IH}$ | $V_{HH}$(4) | Command Address | Data Input |
| Output Disable | X | $V_{IH}$ | X | X | Hi-Z |
| Standby | $V_{IH}$ | X | X | X | Hi-Z |
| Read Manufacturer Code | $V_{IL}$ | $V_{IL}$ | $V_{HH}$ | A0 = $V_{IL}$, A1 = $V_{IL}$, Others $V_{IL}$ or $V_{IH}$ | 0020h |
| Read Device Code | $V_{IL}$ | $V_{IL}$ | $V_{HH}$ | A0 = $V_{IH}$, A1 = $V_{IL}$, Others $V_{IL}$ or $V_{IH}$ | 8888h |

Note: 1. X = $V_{IL}$ or $V_{IH}$.
2. When reading the Status Register during a program operation A22/V$_{PP}$ must be kept at $V_{HH}$.
3. $V_{IL}$ enables the Bottom die, $V_{IH}$ enables the Top die during read array operation.
4. $V_{HH}$ after latching A22 at $V_{IL}$ or $V_{IH}$.

## COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

Refer to Tables 4 and 5, for a summary of the commands.

### Read/Reset Command.

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

$V_{PP}$ must be set to $V_{HH}$ during the Read/Reset command. If $V_{PP}$ is set to either $V_{IL}$ or $V_{IH}$ the command will be ignored. The command can be issued, between Bus Write cycles before the start of a program operation, to return the device to read mode. Once the program operation has started the Read/Reset command is no longer accepted.

### Auto Select Command.

The Auto Select command is used to read the Manufacturer Code and the Device Code. $V_{PP}$ must be set to $V_{HH}$ during the Auto Select command. If $V_{PP}$ is set to either $V_{IL}$ or $V_{IH}$ the command will be ignored. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued, all other commands are ignored.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = $V_{IL}$ and A1 = $V_{IL}$. The other address bits may be set to either $V_{IL}$ or $V_{IH}$.

The Device Code can be read using a Bus Read operation with A0 = $V_{IH}$ and A1 = $V_{IL}$. The other address bits may be set to either $V_{IL}$ or $V_{IH}$.

### Word Program Command.

The Word Program command can be used to program a Word to the memory array. $V_{PP}$ must be set to $V_{HH}$ during Word Program. If $V_{PP}$ is set to either $V_{IL}$ or $V_{IH}$ the command will be ignored, the data will remain unchanged and the device will revert to Read/Reset mode. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the PC.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'.

### Multiple Word Program Command

The Multiple Word Program command can be used to program large streams of data. It greatly reduces the total programming time when a large number of Words are written in the memory at once. $V_{PP}$ must be set to $V_{HH}$ during Multiple Word Program. If $V_{PP}$ is set either $V_{IL}$ or $V_{IH}$ the command will be ignored, the data will remain unchanged and the device will revert to Read mode.

It has four phases: the Setup Phase to initiate the command, the Program Phase to program the data to the memory, the Verify Phase to check that the data has been correctly programmed and reprogram if necessary and the Exit Phase.

**Setup Phase.** The Multiple Word Program command requires three Bus Write operations to initiate the command (refer to Table 4, Multiple Word Program Command and Figure 8, Multiple Word Program Flowchart).

The Status Register must be read in order to check that the PC has started (see Table 7 and Figure 7).

**Program Phase.** The Program Phase requires n+1 Bus Write operations, where n is the number of Words, to execute the programming phase (refer to Table 5, Multiple Word Program and Figure 6, Multiple Word Program Flowchart).

Before any Bus Write operation of the Program Phase, the Status Register must be read in order to check that the PC is ready to accept the operation (see Table 7 and Figure 7).

The Program Phase is executed in three different sub-phases:

1. The first Bus Write operation of the Program Phase (the 4th of the command) latches the Start Address and the first Word to be programmed.

2. Each subsequent Bus Write operation latches the next Word to be programmed and automatically increments the internal Address Bus. It is not necessary to provide the address of the location to be programmed but only a Continue Address, CA (A17 to A21 equal to the

Start Address), that indicates to the PC that the Program Phase has to continue. A0 to A16 are 'don't care'.

3. Finally, after all Words have been programmed, a Bus Write operation (the (n+1)[th]) with a Final Address, FA (A17 or a higher address pin different from the Start Address), ends the Program Phase.

The memory is now set to enter the Verify Phase.

**Verify Phase.** The Verify Phase is similar to the Program Phase in that all Words must be resent to the memory for them to be checked against the programmed data.

Before any Bus Write Operation of the Verify Phase, the Status Register must be read in order to check that the PC is ready for the next operation or if the reprogram of the location has failed (see Table 7 and Figure 7).

Three successive steps are required to execute the Verify Phase of the command:

1. The first Bus Write operation of the Verify Phase latches the Start Address and the Word to be verified.

2. Each subsequent Bus Write operation latches the next Word to be verified and automatically increments the internal Address Bus. As in the Program Phase, it is not necessary to provide the address of the location to be programmed but only a Continue Address, CA (A17 to A21 equal to the Start Address).

3. Finally, after all Words have been verified, a Bus Write cycle with a Final Address, FA (A17 or a higher address pin different from the Start Address) ends the Verify Phase.

**Exit Phase.** After the Verify Phase ends, the Status Register must be read to check if the command has successfully completed or not (see Table 7 and Figure 7).

If the Verify Phase is successful, the memory returns to Read mode and DQ6 stops toggling.

If the PC fails to reprogram a given location, the Verify Phase terminates, DQ6 continues toggling and error bit DQ5 is set in the Status Register. If the error is due to a $V_{PP}$ failure DQ4 is also set.

When the operation fails a Read/Reset command must be issued to return the device to Read mode.

During the Multiple Word Program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

Note that the Multiple Word Program command cannot change a bit set to '0' back to '1'.

**Figure 4. A22 Latch Procedure Waveforms**
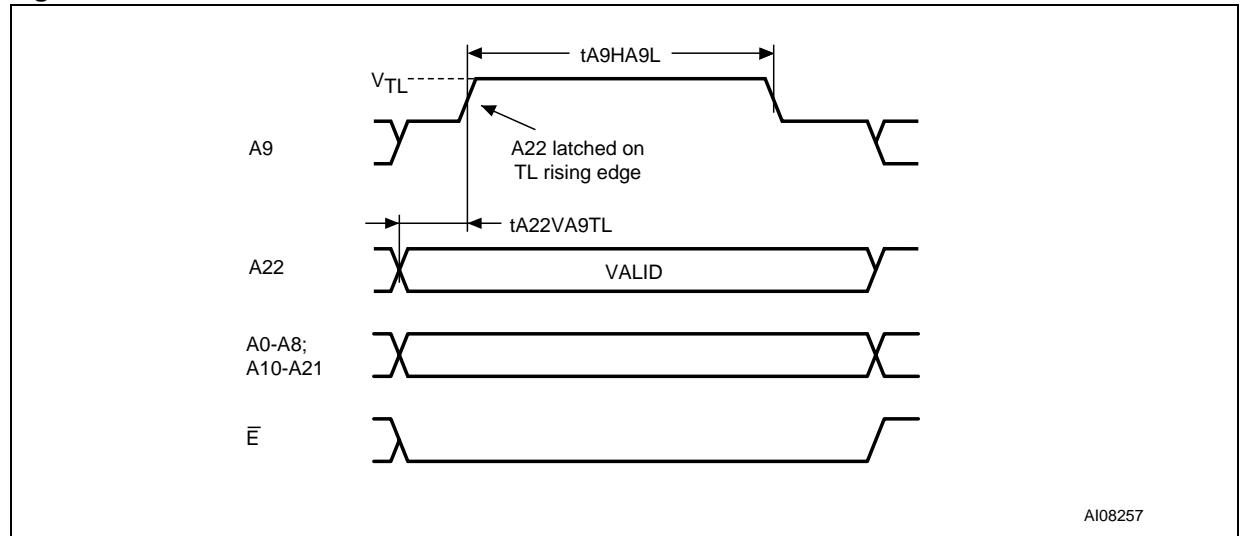


Note: $\overline{G}$ = $V_{IH}$; DQ0–DQ15 are Don't care; $V_{TL}$ = 10.5 ± 0.25V; $V_{CC}$ = 2.7 to 3.6V; $V_{PP}$ = $V_{IL}$ or $V_{IH}$.

**Table 3. A22 Latch Procedure AC Characteristics**

| Symbol | Parameter | Min | Unit |
|---|---|---|---|
| $t_{A22VA9TL}$ | A22 valid to A9 at Third Level | 1 | µs |
| $t_{A9HA9L}$ | A9 High to A9 Low | 1 | µs |

**Figure 5. Programming Flowchart**
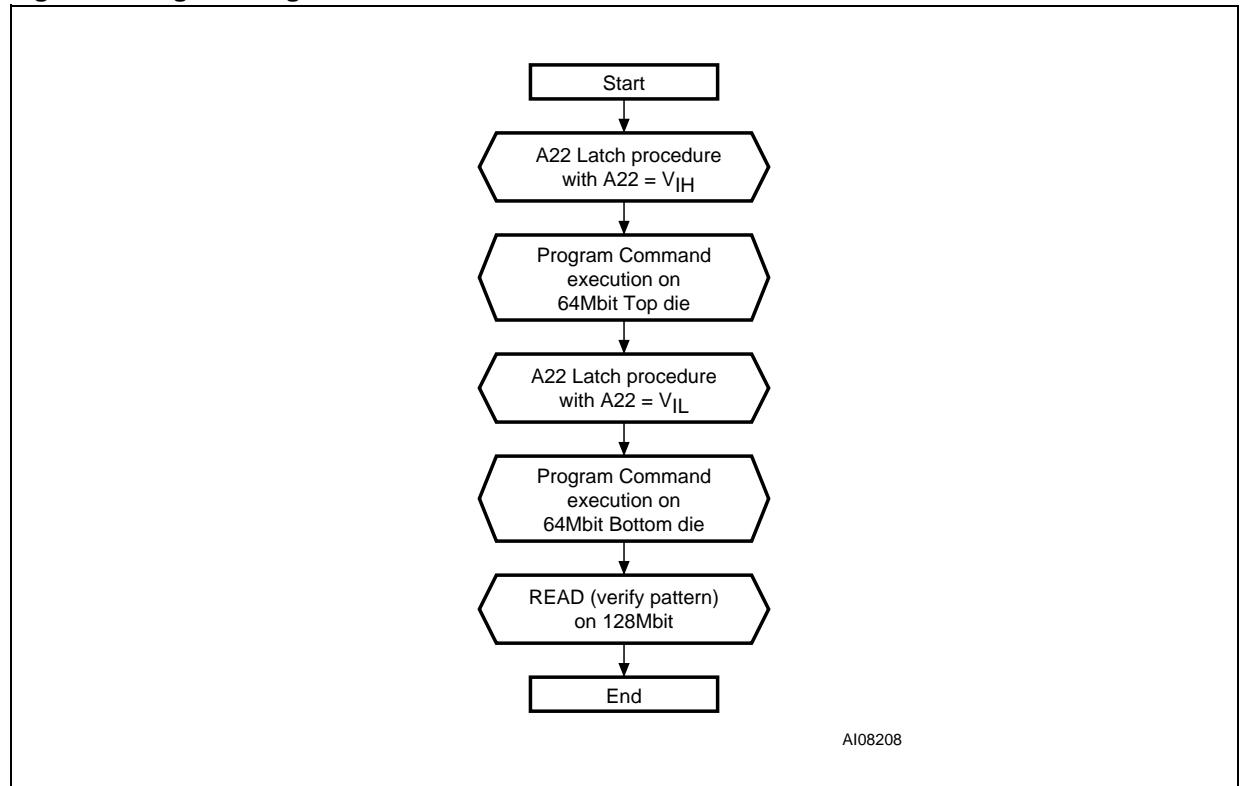
**Table 4. Standard Commands**

| Command | Length | Bus Write Operations | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 1st | | 2nd | | 3rd | | 4th | |
| | | Add | Data | Add | Data | Add | Data | Add | Data |
| Read/Reset | 1 | X | F0 | | | | | | |
| | 3 | 555 | AA | 2AA | 55 | X | F0 | | |
| Auto Select | 3 | 555 | AA | 2AA | 55 | 555 | 90 | | |
| Word Program | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD |

Note: X Don't Care, PA Program Address, PD Program Data. All values in the table are in hexadecimal. The Command Interface only uses A0-A10 and DQ0-DQ7 to verify the commands; A11-A21, DQ8-DQ15 are Don't Care.

**Table 5. Multiple Word Program Command**

| Phase | Length | Bus Write Operations | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | | | nth | | Final | |
| | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | | | Add | Data | Add | Data |
| Set-Up | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | | | | | |
| Program | n+1 | SA | PD1 | CA | PD2 | CA | PD3 | CA | PD4 | CA | PD5 | | | CA | PAn | FA | X |
| Verify | n+1 | SA | PD1 | CA | PD2 | CA | PD3 | CA | PD4 | CA | PD5 | | | CA | PAn | FA | X |

Note: A Bus Read must be done between each Write cycle where the data is programmed or verified, to Read the Status Register and check that the memory is ready to accept the next data. SA is the Start Address. CA is the Continue Address. FA is the Final Address. X Don't Care, n = number of Words to be programmed.

**Table 6. Program Times**

| Parameter | Typ [1] | Max | Unit |
|---|---|---|---|
| Program (Word) | 9 | 200 | µs |
| Chip Program (Multiple Word) | 16 | 280 | s |
| Chip Program (Word by Word) | 72 | 280 | s |

Note: 1. $T_A = 25°C$, $V_{PP} = 12V$.

**Figure 6. Multiple Word Program Flowchart for 64Mbit Top and Bottom Die**



AI05954b
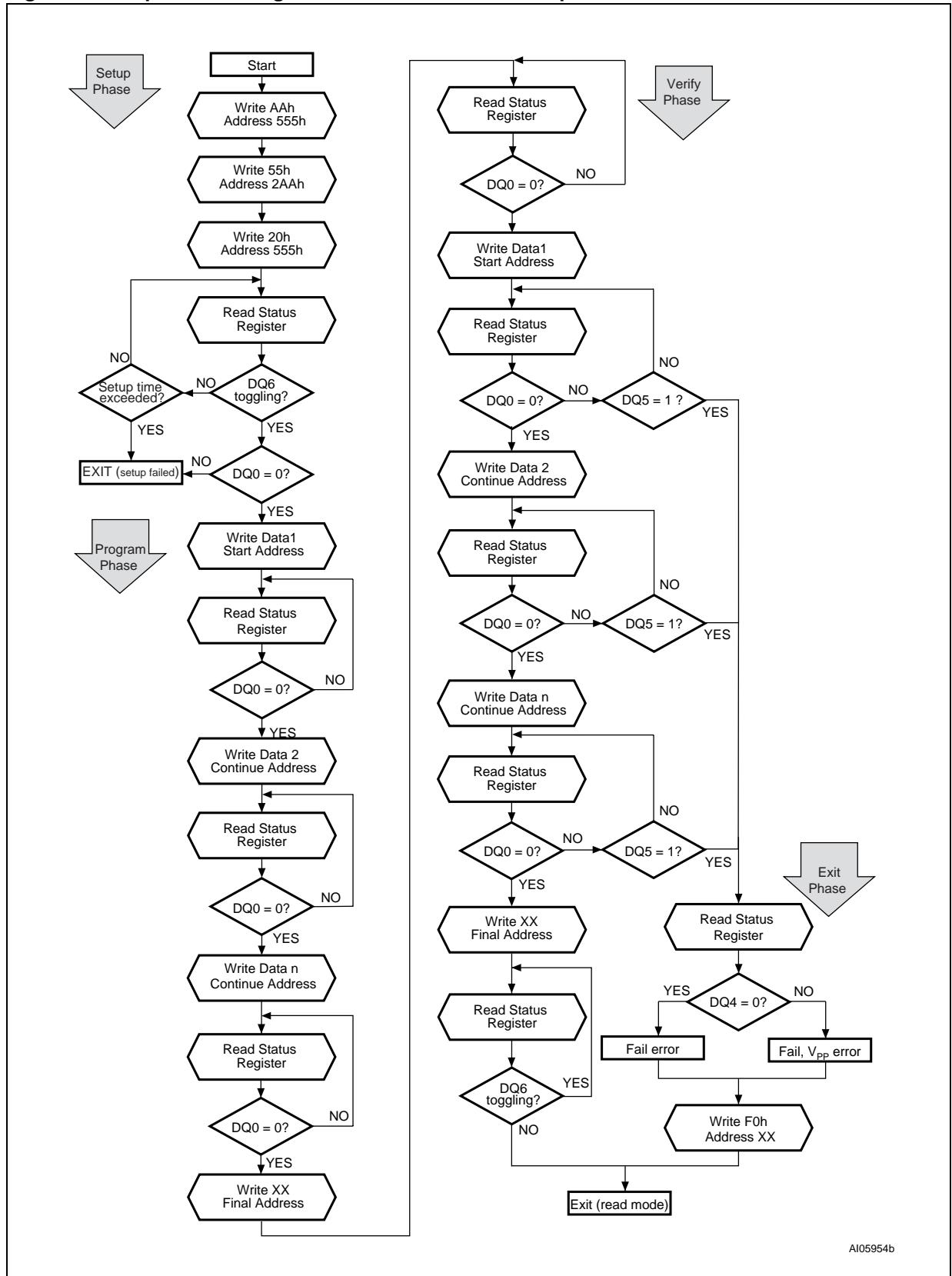
## STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program operations. The bits in the Status Register are summarized in Table 7, Status Register Bits.

**Data Polling Bit (DQ7).** The Data Polling Bit can be used to identify whether the Program Controller has successfully completed its operation. The Data Polling Bit is output on DQ7 when the Status Register is read.

During a Word Program operation the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Word Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

Figure 7, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed.

**Toggle Bit (DQ6).** The Toggle Bit can be used to identify whether the Program Controller has successfully completed its operation. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

Figure 8, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

**Error Bit (DQ5).** The Error Bit can be used to identify errors detected by the Program Controller. The Error Bit is set to '1' when a Program operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'.

**$V_{PP}$ Status Bit (DQ4).** The $V_{PP}$ Status Bit can be used to identify if any Program operation has failed due to a $V_{PP}$ error. If $V_{PP}$ falls below $V_{HH}$ during any Program operation, the operation aborts and DQ4 is set to '1'. If $V_{PP}$ remains at $V_{HH}$ throughout the Program operation, the operation completes and DQ4 is set to '0'.

**Multiple Word Program Bit (DQ0).** The Multiple Word Program Bit can be used to indicate whether the Program Controller is active or inactive during Multiple Word Program. When the Program Controller has written one Word and is ready to accept the next Word, the bit is set to '0'.

**Status Register Bit DQ1 is reserved.**

**Table 7. Status Register Bits**

| Command [1] | P.C. Status | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ0 |
|---|---|---|---|---|---|---|---|
| Multiple Word Program | Programming | – | Toggle | 0 | – | 0 | 1 |
| | Waiting for data | – | Toggle | 0 | – | 0 | 0 |
| | Program fail | – | Toggle | 1 | (2) | 0 | 1 |
| Word Program | Programming | $\overline{DQ7}$ | Toggle | 0 | – | 0 | – |
| | Program error | $\overline{DQ7}$ | Toggle | 1 | (2) | 0 | – |

Note: 1. Unspecified data bits should be ignored.
2. DQ4 = 0 if $V_{PP} \geq V_{HH}$ during Program algorithm execution; DQ4 = 1 if $V_{PP} < V_{HH}$ during Program algorithm execution.

**Figure 7. Data Polling Flowchart**
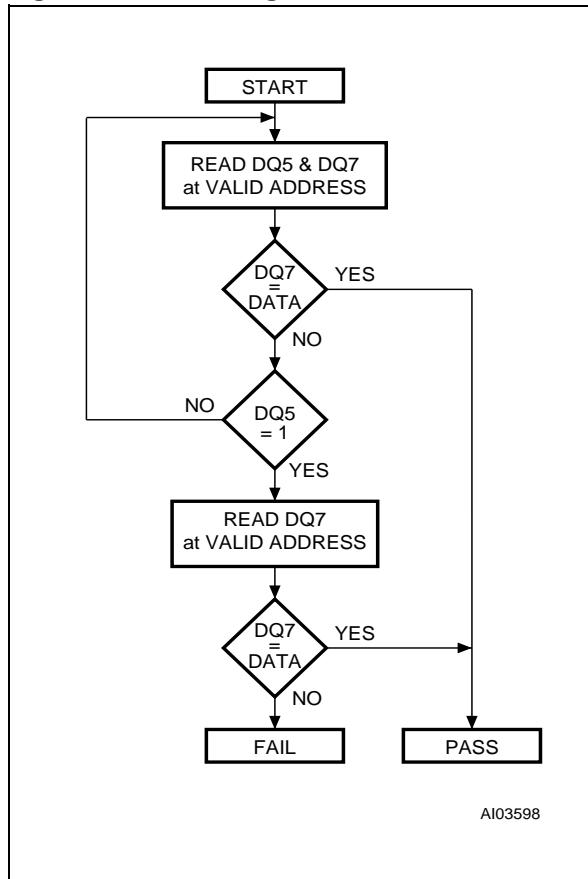


**Figure 8. Data Toggle Flowchart**
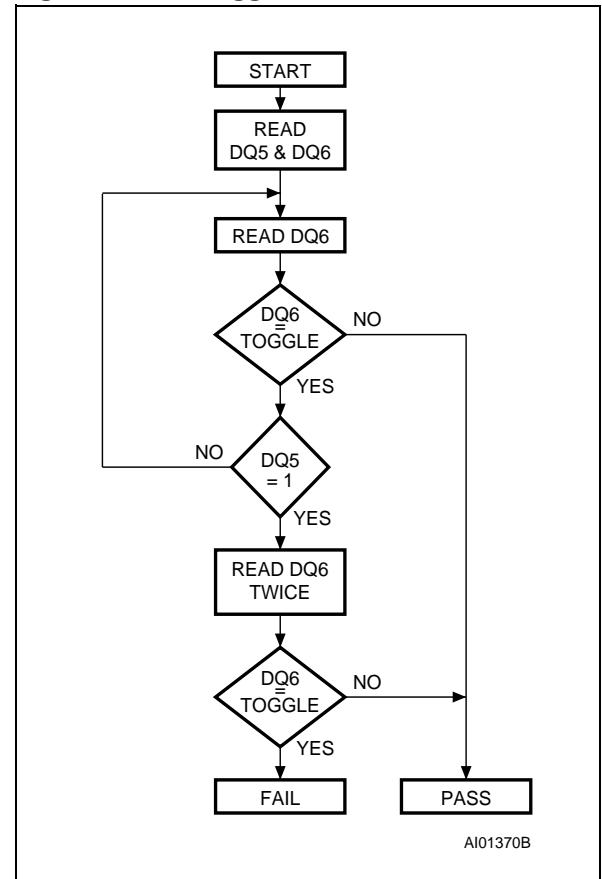
## MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 8. Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| $T_{BIAS}$ | Temperature Under Bias | −50 | 125 | °C |
| $T_{STG}$ | Storage Temperature | −65 | 150 | °C |
| $V_{IO}$ | Input or Output Voltage [1,2] | −0.6 | $V_{CC}$ +0.6 | V |
| $V_{CC}$ | Read Supply Voltage | −0.6 | 4 | V |
| $V_{PP}$ | Program Supply Voltage [3] | −0.6 | 13.5 | V |

Note: 1. Minimum voltage may undershoot to −2V for less than 20ns during transitions.
2. Maximum voltage may overshoot to $V_{CC}$ +2V for less than 20ns during transitions.
3. Maximum voltage may overshoot to 14.0V for less than 20ns during transitions. $V_{PP}$ must not remain at $V_{HH}$ for more than a total of 80hrs.

## DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 9, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 9. Operating and AC Measurement Conditions**

| Parameter | M27W1282 | | Unit |
| --- | --- | --- | --- |
| | 100, 120 | | |
| | Min | Max | |
| $V_{CC}$ Read Supply Voltage | 2.7 | 3.6 | V |
| $V_{PP}$ Program Supply Voltage | 11.4 | 12.6 | V |
| Ambient Operating Temperature | 0 | 70 | °C |
| Load Capacitance ($C_L$) | 30 | | pF |
| Input Rise and Fall Times | | 10 | ns |
| Input Pulse Voltages | 0 to 3 | | V |
| Input and Output Timing Ref. Voltages | 1.5 | | V |

**Figure 9. AC Measurement I/O Waveform**



AI05546
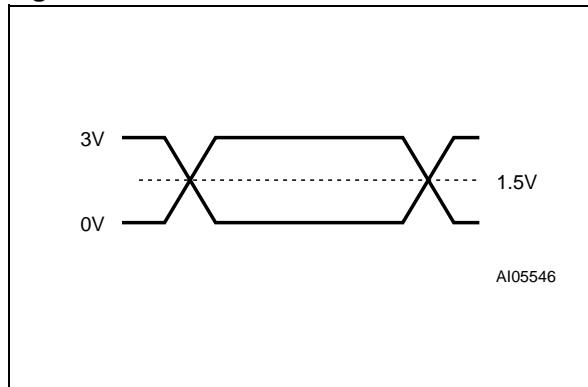
**Figure 10. AC Measurement Load Circuit**



$C_L$ = 30pF

$C_L$ includes JIG capacitance

AI05447
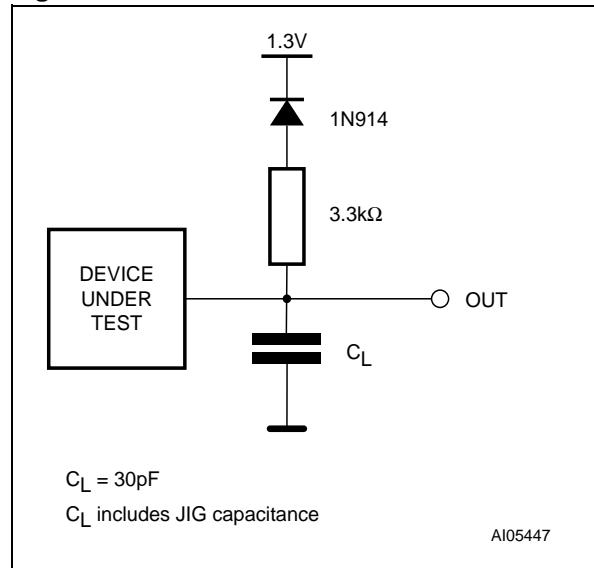
**Table 10. Device Capacitance**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
| --- | --- | --- | --- | --- | --- |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 12 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 24 | pF |
| $C_{A22/Vpp}$ | A22/$V_{PP}$ Capacitance | $V_{A22/Vpp}$ = 0V | | 50 | pF |

Note: Sampled only, not 100% tested.

**Table 11. DC Characteristics**

| Symbol | Parameter [1] | Test Condition | Min | Max | Unit |
|--------|---------------|----------------|-----|-----|------|
| $I_{LI}$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \leq V_{OUT} \leq V_{CC}$ | | ±1 | µA |
| $I_{CC1}$ | Supply Current (Read) | $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, $I_{OUT} = 0mA$, $f = 6MHz$ | | 10 | mA |
| $I_{CC2}$ [2] | Supply Current (Standby) | $\overline{E} = V_{CC} \pm 0.2V$ | | 150 | µA |
| $I_{CC3}$ | Supply Current (Program) | PC active | | 20 | mA |
| $V_{IL}$ | Input Low Voltage | | −0.5 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | $0.7V_{CC}$ | $V_{CC} +0.3$ | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 1.8mA$ | | 0.45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -100µA$ | $V_{CC} -0.4$ | | V |
| $V_{HH}$ | $V_{PP}$ Program Voltage | | 11.4 | 12.6 | V |
| $I_{HH}$ | $V_{PP}$ Current (Program) | PC Active | | 10 | mA |

Note: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
     2. Average Value.

**Figure 11. Read AC Waveforms**



AI08263
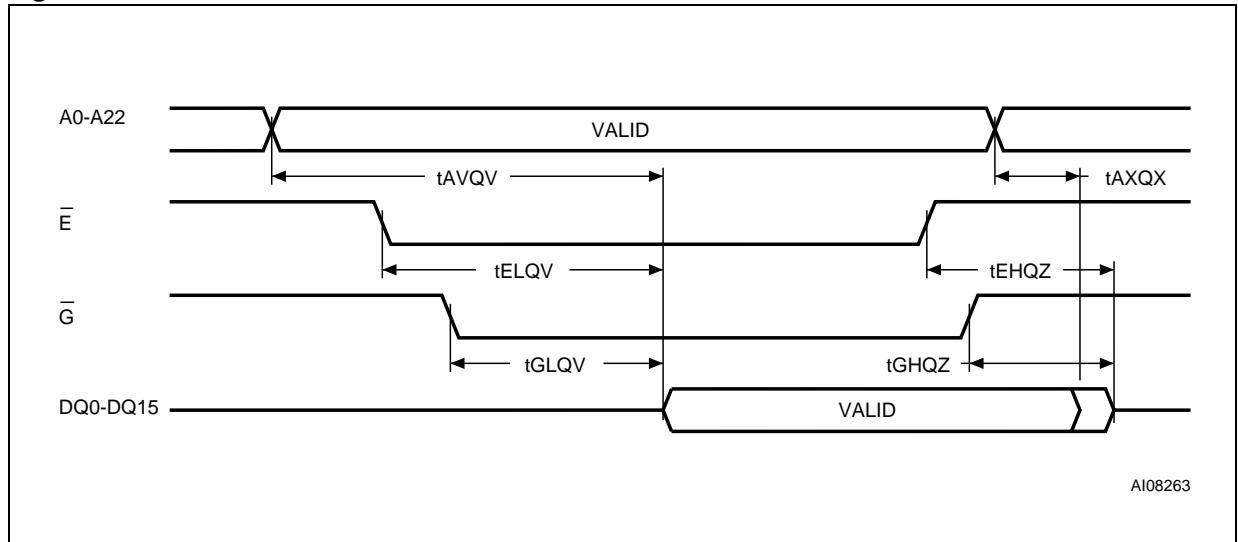
**Table 12. Read AC Characteristics**

| Symbol | Alt | Parameter [1] | Test Condition | | M27W1282 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | 100 | | 120 | |
| | | | | | $V_{CC}$ = 3.0 to 3.6V | $V_{CC}$ = 2.7 to 3.6V | $V_{CC}$ = 2.7 to 3.6V | |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | Max | 90 | 100 | 120 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G} = V_{IL}$ | Max | 90 | 100 | 120 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E} = V_{IL}$ | Max | 35 | 35 | 35 | ns |
| $t_{EHQZ}$ [2] | $t_{HZ}$ | Chip Enable High to Output Hi-Z | $\overline{G} = V_{IL}$ | Max | 30 | 30 | 30 | ns |
| $t_{GHQZ}$ [2] | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E} = V_{IL}$ | Max | 30 | 30 | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | | Min | 0 | 0 | 0 | ns |

Note: 1. $V_{PP}$ must be applied after $V_{CC}$ and with the Chip Enable ($\overline{E}$) at $V_{IH}$.
2. Sampled only, not 100% tested.

## Figure 12. Chip Enable Controlled, Write AC Waveforms
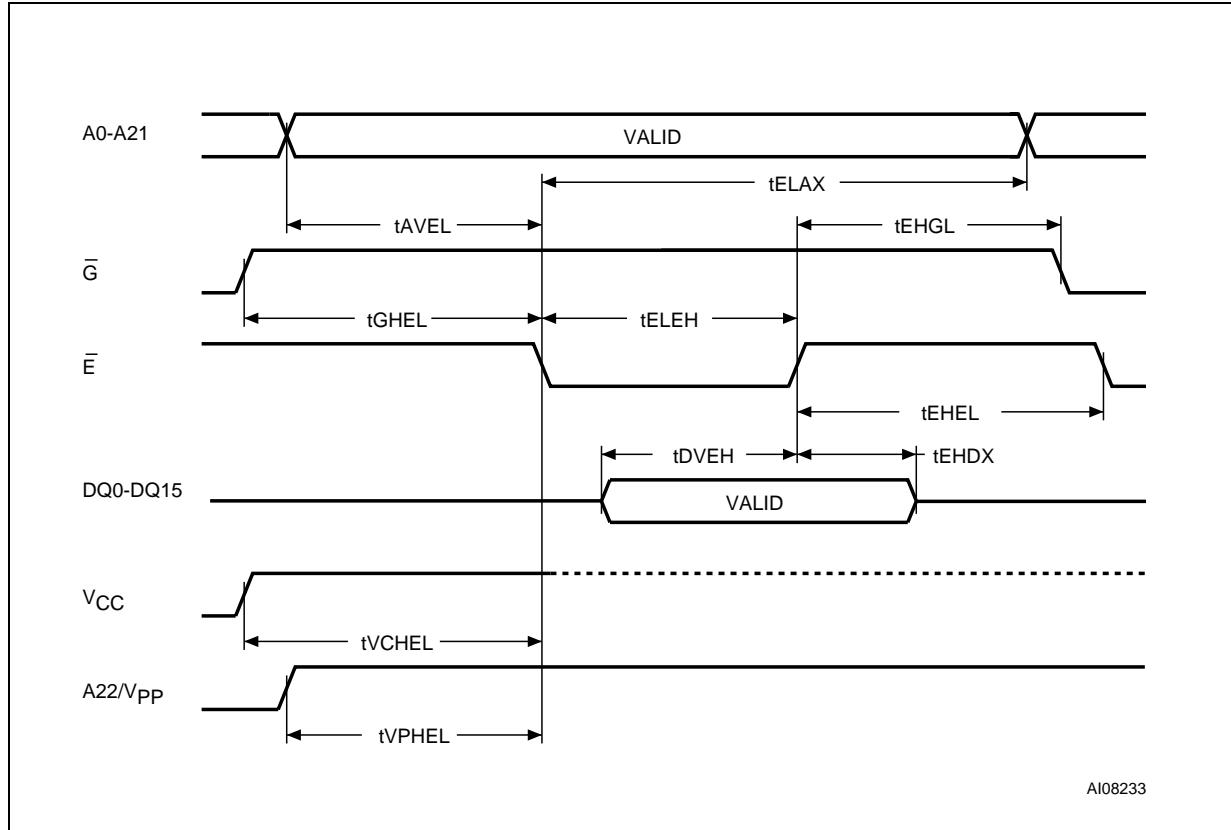


## Table 13. Chip Enable Controlled, Write AC Characteristics

| Symbol | Alt | Parameter [1] | | M27W1282 | Unit |
|--------|-----|---------------|-----|----------|------|
| $t_{ELEH}$ | $t_{CP}$ | Chip Enable Low to Chip Enable High | Min | 50 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Input Valid to Chip Enable High | Min | 50 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Chip Enable High to Input Transition | Min | 0 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | Chip Enable High to Chip Enable Low | Min | 50 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Valid to Chip Enable Low | Min | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Chip Enable Low to Address Transition | Min | 100 | ns |
| $t_{GHEL}$ | | Output Enable High Chip Enable Low | Min | 10 | ns |
| $t_{EHGL}$ | $t_{OEH}$ | Chip Enable High to Output Enable Low | Min | 10 | ns |
| $t_{VCHEL}$ | $t_{VCS}$ | $V_{CC}$ High to Chip Enable Low | Min | 50 | µs |
| $t_{VPHEL}$[2] | $t_{VCS}$ | $V_{PP}$ High to Chip Enable Low | Min | 500 | ns |

Note: 1. $T_A = 25°C$; $V_{PP} = 11.4$ to $12.6V$. $V_{CC} = 2.7$ to $3.6V$.
$V_{PP}$ must be applied after $V_{CC}$ and with the Chip Enable ($\overline{E}$) at $V_{IH}$.
Sampled only, not 100% tested.
2. Not required in Auto Select or Read/Reset command sequences.

## PACKAGE MECHANICAL

**Figure 13. SO44 - 44 lead Plastic Small Outline, 500 mils body width, Package Outline**
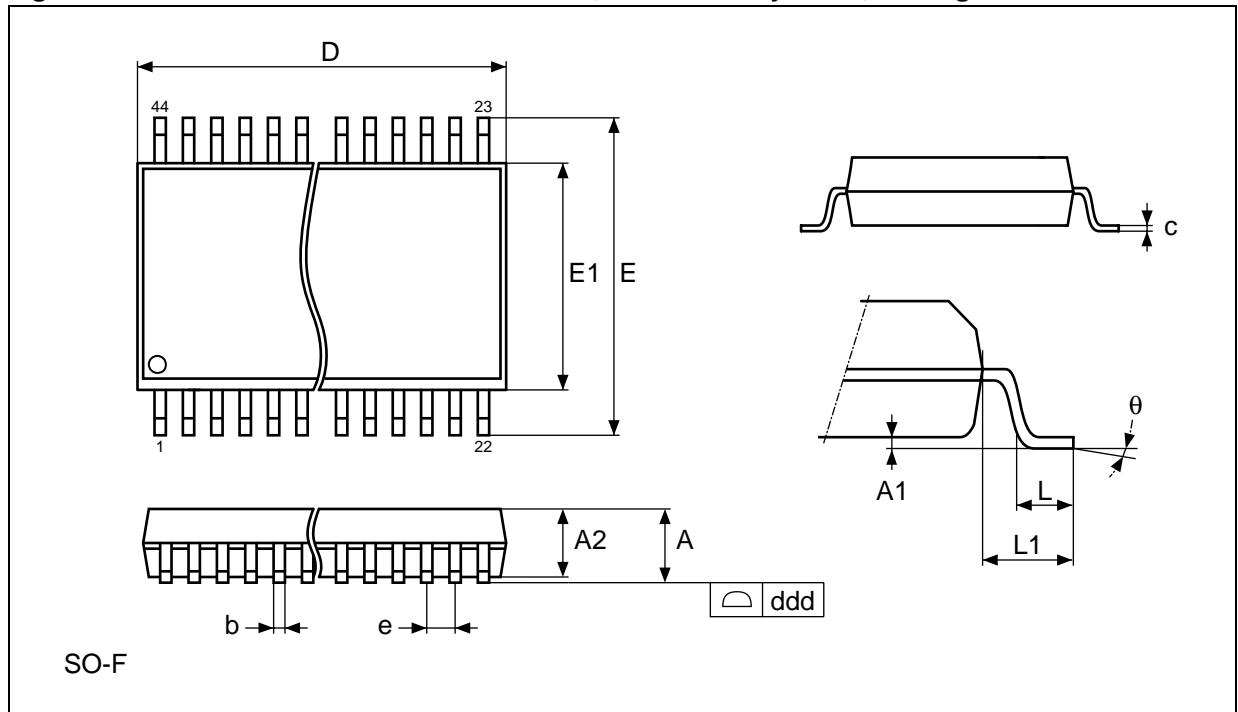


Note: Drawing is not to scale.

**Table 14. SO44 - 44 lead Plastic Small Outline, 500 mils body width, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|--------|-----|-----|-----|-----|-----|-----|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 3.00 | | | 0.118 |
| A1 | 0.10 | | | 0.004 | | |
| A2 | 2.69 | 2.56 | 2.79 | 0.106 | 0.101 | 0.110 |
| b | | 0.35 | 0.50 | | 0.014 | 0.020 |
| c | | 0.18 | 0.28 | | 0.007 | 0.011 |
| D | 28.50 | 28.37 | 28.63 | 1.122 | 1.117 | 1.127 |
| ddd | | | 0.10 | | | 0.004 |
| E | 16.03 | 15.77 | 16.28 | 0.631 | 0.621 | 0.641 |
| E1 | 12.60 | 12.47 | 12.73 | 0.496 | 0.491 | 0.501 |
| e | 1.27 | – | – | 0.050 | – | – |
| L | 0.79 | | | 0.031 | | |
| L1 | 1.73 | | | 0.068 | | |
| θ | | | 8° | | | 8° |
| N | 44 | | | 44 | | |

## PART NUMBERING

### Table 15. Ordering Information Scheme

Example:                           M27W128 2          100 N 1 T

**Device Type**
M27 = FlexibleROM™ Memory

**Operating Voltage**
W = V$_{CC}$ = 2.7 to 3.6V

**Device Function**
128 = 128 Mbit (x16)

**Device Function**
2 = 2 dice
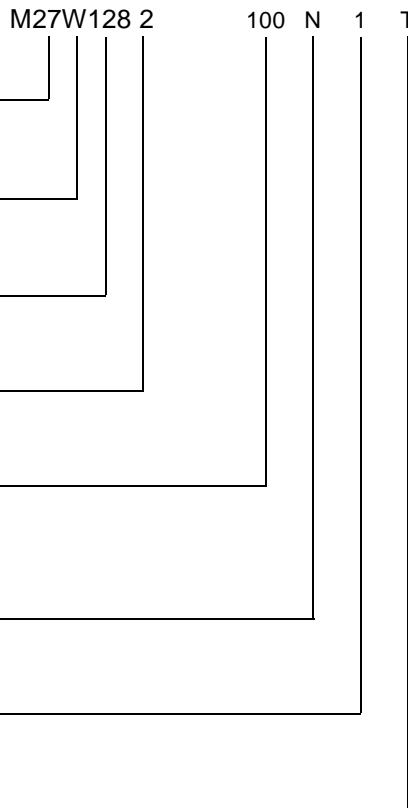
**Speed**
100 $^{(1)}$ = 100 ns
120 = 120 ns

**Package**
M = SO44, 500mils body width

**Temperature Range**
1 = 0 to 70 °C

**Option**
T = Tape & Reel Packing

Note: 1. This speed also guarantees 90ns access time at V$_{CC}$ = 3.0 to 3.6V.

Devices are shipped from the factory with all the bits set to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

## REVISION HISTORY

### Table 16. Document Revision History

| Date | Version | Revision Details |
|------|---------|------------------|
| 29-Apr-2003 | 1.0 | First Issue |
| 17-Sep-2003 | 1.1 | From Preliminary Data to Datasheet |
| 17-Nov-2003 | 1.2 | 100ns speed class also guarantees 90ns |

STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States

**www.st.com**