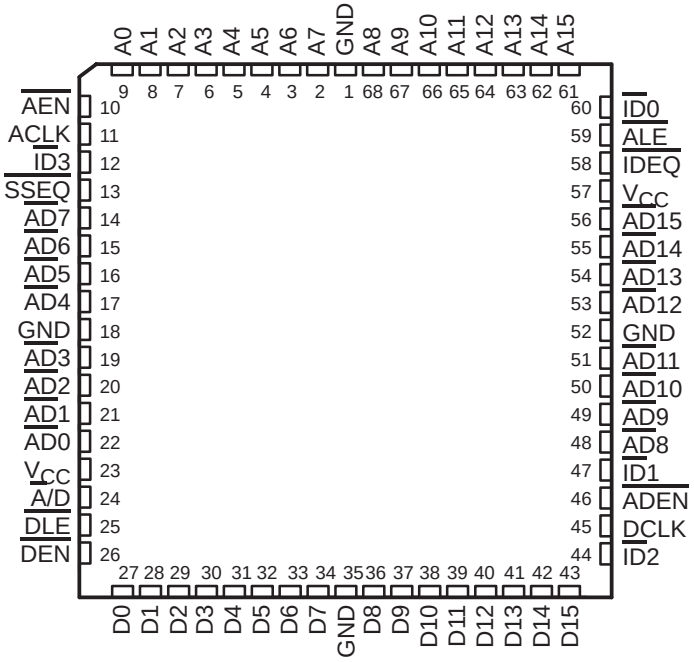
SDIS007A – D3159, NOVEMBER 1988 – REVISED JANUARY 1989

- **Designed for NuBus™ Interface Applications**
- **Conforms to ANSI/IEEE Std 1196-1987**
- **On-Chip Comparator Provides I/D Slot Identification**
- **Multiplexed Real-Time and Latched Address/Data**
- **Designed to Operate With SN74ACT2440 NuBus™ Controller**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas instruments Quality and Reliability**

**FN PACKAGE**
**(TOP VIEW)**




## description

The ’BCT2420 consists of bus transceiver circuits, D-type flip-flops, latches, and control circuitry arranged for multiplexed transmission of address and data information in NuBus™ applications. An on-chip comparator has been included to detect when a NuBus™ transfer cycle is requesting the local board. The device conforms to ANSI/IEEE Std 1196-1987 and operates with Texas instruments SN74ACT2440 NuBus™ Controller. In addition, the device is easily configured around ASIC or other PAL® -based controllers.

The ’BCT2420 was designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics and greatly reduces the standby power of the device when disabled. This feature is especially valuable when the device is not performing a NuBus™ transaction.

The $\overline{\text{AEN}}$, $\overline{\text{DEN}}$ and $\overline{\text{ADEN}}$ inputs control the transceiver functions. Three 16-bit I/O ports, A15–A0, D15–D0, and $\overline{\text{AD}}$15–$\overline{\text{AD}}$0, provide for address and data transfer. When the NuBus™ performs a write cycle to the local board, address information is saved on the rising edge of ACLK. During the last portion of the NuBus™ write cycle, data information is saved on the rising edge of DCLK.

When the local board is performing a write to the NuBus™, address and data is multiplexed onto the NuBus™ via the $\overline{\text{A}}$/D line. Address and data can be latched by using the $\overline{\text{ALE}}$ and $\overline{\text{DLE}}$ input lines respectively.

The $\overline{\text{IDEQ}}$ output is used to signal that the local board is being requested by the NuBus™. This output is typically fed to the NuBus™ controller. $\overline{\text{IDEQ}}$ goes active (low) when $\overline{\text{AD}}$15–$\overline{\text{AD}}$12 are low and $\overline{\text{AD}}$11–$\overline{\text{AD}}$8 match $\overline{\text{ID}}$3–$\overline{\text{ID}}$0. $\overline{\text{IDEQ}}$ stays valid until the next address clock (ACLK) occurs. Internal 10-kΩ pullup resistors are included on the $\overline{\text{ID}}$3–$\overline{\text{ID}}$0 inputs.

The $\overline{\text{SSEQ}}$ output is used to signal the local board that super-slot addresses are being requested. This output is active (low) whenever $\overline{\text{AD}}$15–$\overline{\text{AD}}$12 are equal to $\overline{\text{ID}}$3–$\overline{\text{AD}}$0, except when $\overline{\text{ID}}$3–$\overline{\text{ID}}$0 are all low.

In typical NuBus™ applications, two devices are required to provide the full 32-bit address/data path. Refer to the typical NuBus™ interface diagram on page 9 for additional information.

The SN74BCT2420 is characterized for operation from 0°C to 70°C.

NuBus is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories Inc.

## Function Tables

| INPUTS | | | | | | OUTPUTS |
|---|---|---|---|---|---|---|
| A15–A0 | D15–D0 | $\overline{ALE}$ | $\overline{DLE}$ | A/$\overline{D}$ | $\overline{ADEN}$ | $\overline{AD15}$–$\overline{AD0}$ |
| H | X | L | X | L | L | L |
| L | X | L | X | L | L | H |
| X | X | H | X | L | L | $Q_O$ |
| X | H | X | L | H | L | L |
| X | L | X | L | H | L | H |
| X | X | X | H | H | L | $Q_O$ |
| X | X | X | X | X | H | Z |

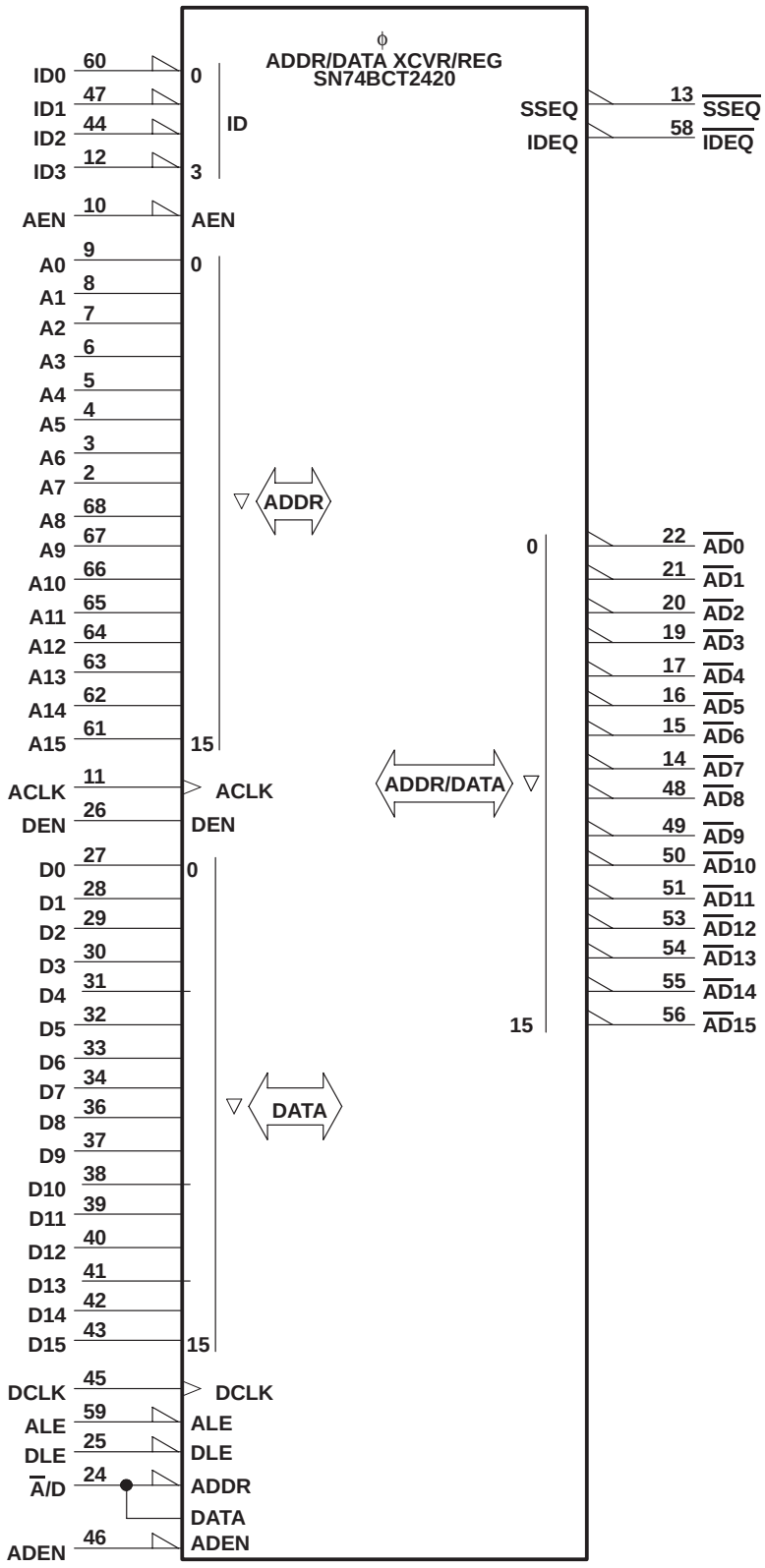
| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{AD15}$–$\overline{AD0}$ | ACLK, DCLK | $\overline{AEN}$, $\overline{DEN}$ | A15–A0, D15–DO |
| H | ↑ | L | L |
| L | ↑ | L | H |
| X | L | L | $Q_O$ |
| X | X | H | L |

| $\overline{AD15}$–$\overline{AD12}$ | $\overline{ID3}$–$\overline{ID0}$ | $\overline{SSEQ}$ |
|---|---|---|
| EQ $\overline{ID3}$–$\overline{ID0}$ | NE 0 | L |
| NE $\overline{ID3}$–$\overline{ID0}$ | X | H |
| X | EQ 0 | H |

| $\overline{AD15}$–$\overline{AD12}$ | $\overline{AD11}$–$\overline{AD8}$ | $\overline{IDEQ}$ |
|---|---|---|
| EQ 0 | EQ $\overline{ID3}$–$\overline{ID0}$ | L |
| X | NE $\overline{ID3}$–$\overline{ID0}$ | H |
| NE 0 | X | H |

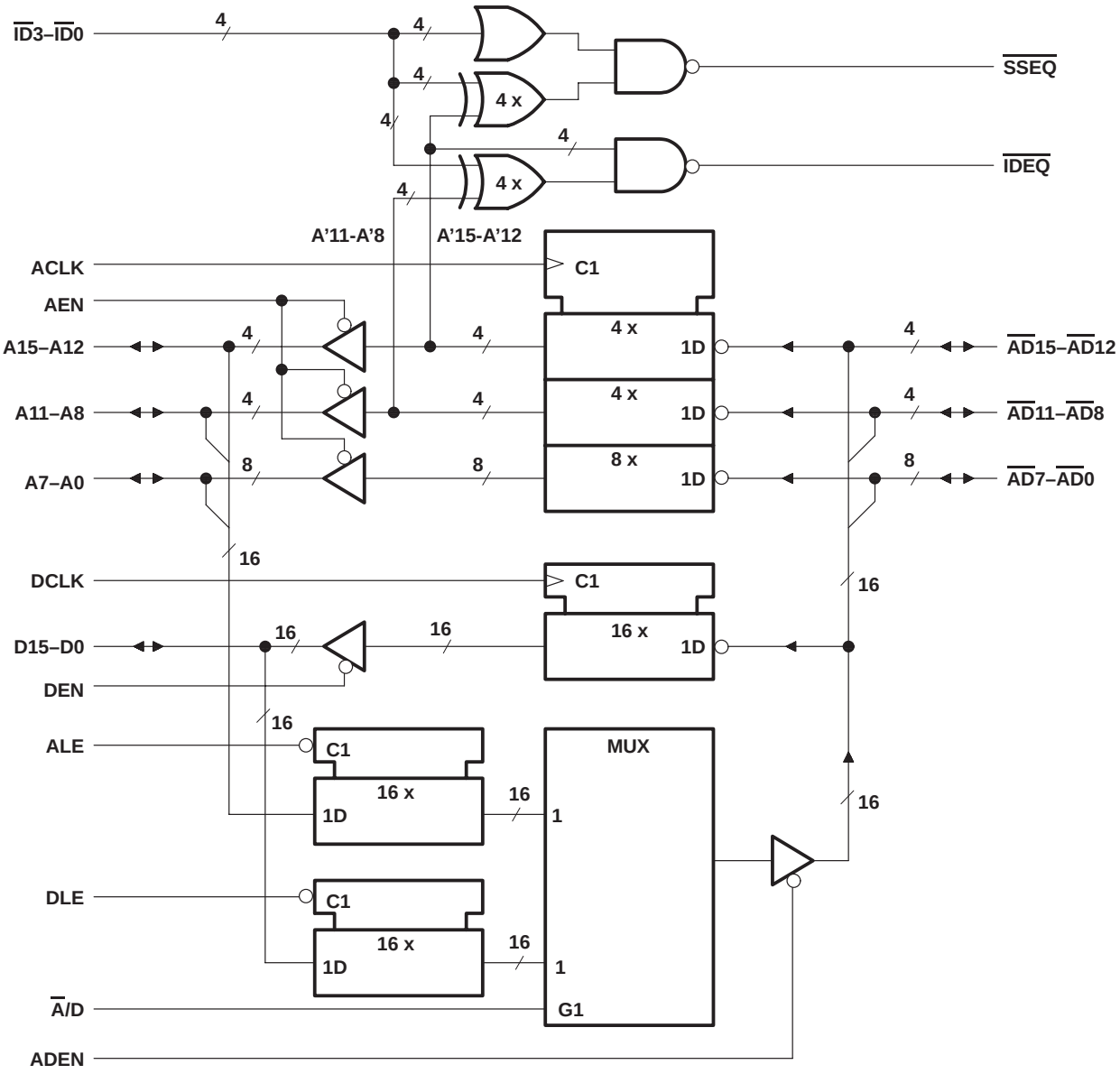
NOTE: Symbol '$Q_O$' denotes previous logic state preserved. Symbol 'Z' denotes high-impedance state.

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std. 91-1984.

## logic diagram



## Terminal Functions

| PIN NAME | DESCRIPTION |
|---|---|
| A15–A0 | Address bus. This 16-bit I/O port is connected to the local board's address bus. When information is transferred between this port and the NuBus™ port ($\overline{AD}$15–$\overline{AD}$0), the data is inverted to conform to NuBus™ specifications. |
| ACLK | Address clock. This input saves the address portion of NuBus™ read or write cycles. Data present at the $\overline{AD}$15–$\overline{AD}$0 inputs is clocked into the address register on the low-to-high transition of ACLK. |
| $\overline{A}$/D | Address/data select. This input controls the address/data multiplexer. When $\overline{A}$/D is driven low, the local address port, A15–A0, is selected as input to the $\overline{AD}$15–$\overline{AD}$0 outputs. When $\overline{A}$/D is taken high, the local data port, D15–D0, is selected as input to the $\overline{AD}$15–$\overline{AD}$0 outputs. |
| $\overline{AD}$15–$\overline{AD}$0 | Address/data port. This 16-bit active-low I/O port directly interfaces to the NuBus™ address/data lines. These lines are multiplexed to carry address information at the beginning of a NuBus™ cycle and data information later in the cycle. |
| $\overline{ADEN}$ | Address/data output enable. This active-low input enables the $\overline{AD}$15–$\overline{AD}$0 outputs. When $\overline{ADEN}$ is taken high, the $\overline{AD}$15–$\overline{AD}$0 outputs are in the high impedance state, allowing input from the NuBus™. |
| $\overline{AEN}$ | Address enable. This active-low input enables the local address outputs. A15–A0, to place data onto the local board. When $\overline{AEN}$ is taken high, the A15–A0 outputs are in the high-impedance state, allowing input from the local address bus. |
| $\overline{ALE}$ | Address latch enable. This active-low input controls the latch that holds the address received from the local address bus, A15–A0. When $\overline{ALE}$ is low, the latch is transparent. When $\overline{ALE}$ is taken high, the address present at the A15–A0 inputs is latched and remains latched while $\overline{ALE}$ is held high. |
| D15–D0 | Data bus. This 16-bit I/O port is connected to the local board's data bus. When information is transferred between this port and the NuBus™ port ($\overline{AD}$15–$\overline{AD}$0), the data is inverted to conform to NuBus™ specifications. |
| DCLK | Data clock. This input saves the data portion of NuBus™ write cycles. Data present at the $\overline{AD}$15–$\overline{AD}$0 inputs is clocked into the data register on the low-to-high transition of DCLK. |
| $\overline{DEN}$ | Data enable. This active-low input enables the local data port outputs, D15–D0, to place data onto the local board. When $\overline{DEN}$ is taken high, the D15–D0 outputs are in the high-impedance state, allowing input from the local board. |
| $\overline{DLE}$ | Data latch enable. This active-low input controls the latch that holds the data received from the local data bus, D15–D0. When $\overline{DLE}$ is low, the latch is transparent. When $\overline{DLE}$ is taken high, the data present at the D15–D0 inputs is latched and remains latched while $\overline{DLE}$ is held high. |
| $\overline{ID}$3–$\overline{ID}$0 | Card-slot identification. These four inputs accept binary-coded location information for each NuBus™ slot position on the backplane. These four lines are typically hard wired logic levels unique to each NuBus™ slot connector. For convenient implementation, the inputs have internal 10-kΩ pull up resistors that ensure the logic high level when the inputs are left open circuited. The internal comparator uses these inputs to identify when the local hardware card is being accessed. |
| $\overline{IDEQ}$ | Identification equal. This active-low output is used to signal that the board is being accessed by the NuBus™. $\overline{IDEQ}$ goes low whenever $\overline{AD}$15–$\overline{AD}$12 are low and $\overline{AD}$11–$\overline{AD}$8 match $\overline{ID}$3–$\overline{ID}$0. Since the internal comparator uses data from the address register, the address register must be clocked before the local board samples $\overline{IDEQ}$. $\overline{IDEQ}$ is valid for the entire NuBus™ cycle after ACLK. |
| $\overline{SSEQ}$ | Super-slot equal. This active-low output is used to signal the local board that super-slot addresses are being requested in the super-slot mode. $\overline{SSEQ}$ goes low when $\overline{AD}$15–$\overline{AD}$12 match $\overline{ID}$3–$\overline{ID}$0 and $\overline{ID}$3–$\overline{ID}$0 are not all low. Since the internal comparator uses data from the address register, the address register must be clocked before the local board samples $\overline{SSEQ}$. $\overline{SSEQ}$ is valid for the entire NuBus™ cycle after ACLK. |

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

### recommended operating conditions

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level input current | Ax, Dx, $\overline{ADx}$ outputs | | | –15 | mA |
| | | $\overline{SSEQ}$, $\overline{IDEQ}$ outputs | | | 2.6 | |
| $I_{OL}$ | Low-level input current | Ax, Dx, $\overline{ADx}$ outputs | | | 24 | mA |
| | | $\overline{SSEQ}$, $\overline{IDEQ}$ outputs | | | 16 | |
| $f_{clock}$ | Clock frequency | | 0 | | 40 | MHz |
| $t_w$ | Pulse duration | ACLK, DCLK high | 12.5 | | | ns |
| | | ACLK, DCLK low | 12.5 | | | |
| | | $\overline{ALE}$, $\overline{DLE}$ low | 12.5 | | | |
| $t_{su}$ | Setup time | $\overline{ADx}$ before ACLK↑, DCLK↑ | 5 | | | ns |
| | | Ax before $\overline{ALE}$↑ | 5 | | | |
| | | Dx before $\overline{DLE}$↑ | 5 | | | |
| $t_h$ | Hold time | $\overline{ADx}$ after ACLK↑, DCLK↑ | 2 | | | ns |
| | | Ax after $\overline{ALE}$↑ | 2 | | | |
| | | Dx after $\overline{DLE}$↑ | 2 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70° | °C |

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | Ax, Dx, $\overline{ADx}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –400 µA | $V_{CC}$–1.5 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.8 | 3.6 | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –15 mA | 2 | | | |
| | $\overline{SSEQ}$, $\overline{IDEQ}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –400 µA | $V_{CC}$–2 | | | |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2.6 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Ax, Dx, $\overline{ADx}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| | $\overline{SSEQ}$, $\overline{IDEQ}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 8 mA | | 0.25 | 0.4 | |
| | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 16 mA | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | 100 | µA |
| $I_{IH}$‡ | $\overline{AEN}$, $\overline{DEN}$, $\overline{ADEN}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| | $\overline{ID3}$–$\overline{ID0}$ | | | | | –400 | |
| | All other inputs | | | | | –100 | |
| $I_{IL}$‡ | $\overline{ID3}$–$\overline{ID0}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –750 | µA |
| | All other inputs | | | | | –200 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 V | –60 | | –225 | mA |
| $I_{CC}$ | Enabled | $V_{CC}$ = 5.5 V, $V_{IH}$ = 3 V, | $V_{IL}$ = 0.5 V, Outputs open | | 110 | 160 | mA |
| | Disabled | | | | 30 | 40 | |

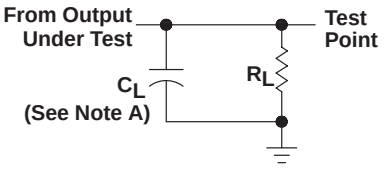
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

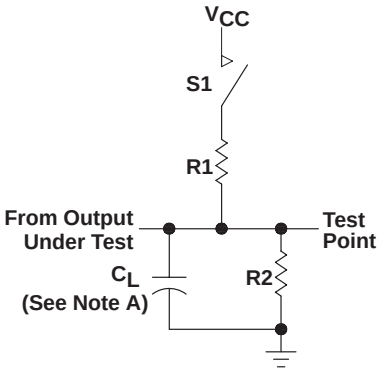
| PARAMETER | | LOAD CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | R1, R2, and $R_L$ | $C_L$ | LOAD CIRCUIT | | | | |
| $f_{max}$ | Maximum clock frequency | | | | 40 | | | MHz |
| $t_{pd}$ | Propagation time, ACLK↑ to Ax ($\overline{AEN}$ = L) | R1 = 500 Ω, R2 = 500 Ω | 50 pF | S1 Open‡ | | 9 | 16 | ns |
| $t_{pd}$ | Propagation time, DCLK↑ to Dx ($\overline{DEN}$ = L) | R1 = 500 Ω, R2 = 500 Ω | 50 pF | S1 Open‡ | | 9 | 16 | ns |
| $t_{pd}$ | Propagation time, Ax to $\overline{AD}$x ( $\overline{ALE}$ = L, $\overline{A}$/D = L) | R1 = 270 Ω, R2 = 470 Ω | 300 pF | S1 Closed§ | | 10 | 18 | ns |
| $t_{pd}$ | Propagation time, Dx to $\overline{AD}$x ( $\overline{DLE}$ = L, $\overline{A}$/D = H) | R1 = 270 Ω, R2 = 470 Ω | 300 pF | S1 Closed§ | | 11 | 18 | ns |
| $t_{pd}$ | Propagation time, $\overline{ALE}$ low to $\overline{AD}$x (A/D = L) | R1 = 270 Ω, R2 = 470 Ω | 300 pF | S1 Closed§ | | 10 | 18 | ns |
| $t_{pd}$ | Propagation time, $\overline{DLE}$ low to $\overline{AD}$x ($\overline{A}$/D = H) | R1 = 270 Ω, R2 = 470 Ω | 300 pF | S1 Closed§ | | 11 | 18 | ns |
| $t_{pd}$ | Propagation time, $\overline{A}$/D to $\overline{AD}$x | R1 = 270 Ω, R2 = 470 Ω | 300 pF | S1 Closed§ | | 10 | 16 | ns |
| $t_{pd}$ | Propagation time, ACLK to $\overline{IDEQ}$ | $R_L$ = 500 Ω | 50 pF | ¶ | | 12 | 20 | ns |
| $t_{pd}$ | Propagation time, ACLK to $\overline{SSEQ}$ | $R_L$ = 500 Ω | 50 pF | ¶ | | 12 | 18 | ns |
| $t_{pd}$ | Propagation time, $\overline{ID}$x to $\overline{IDEQ}$ | $R_L$ = 500 Ω | 50 pF | ¶ | | 12 | 22 | ns |
| $t_{pd}$ | Propagation time, $\overline{ID}$x to $\overline{SSEQ}$ | $R_L$ = 500 Ω | 50 pF | ¶ | | 12 | 22 | ns |
| $t_{en}$ | Enable time, $\overline{AEN}$ to Ax | R1 = 500 Ω, R2 = 500 Ω | 50 pF | ‡ | | 10 | 16 | ns |
| $t_{en}$ | Enable time, $\overline{DEN}$ to Dx | R1 = 500 Ω, R2 = 500 Ω | 50 pF | ‡ | | 10 | 16 | ns |
| $t_{en}$ | Enable time, $\overline{ADEN}$ to $\overline{AD}$x | R1 = 270 Ω, R2 = 470 Ω | 300 pF | § | | 10 | 18 | ns |
| $t_{dis}$ | Disable time, $\overline{AEN}$ to Ax | R1 = 500 Ω, R2 = 500 Ω | 50 pF | ‡ | | 6 | 10 | ns |
| $t_{dis}$ | Disable time, $\overline{DEN}$ to Dx | R1 = 500 Ω, R2 = 500 Ω | 50 pF | ‡ | | 6 | 10 | ns |
| $t_{dis}$ | Disable time, $\overline{ADEN}$ to $\overline{AD}$x | R1 = 270 Ω, R2 = 470 Ω | 50 pF | § | | 6 | 10 | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ See Parameter Measurement Information for load circuit (3-state outputs, A15–A0, $\overline{D15}$–D0) and voltage waveforms.
§See Parameter Measurement Information for load circuit (NuBus™ Interface, $\overline{AD15}$–$\overline{AD0}$) and voltage waveforms.
¶See Parameter Measurement Information for load circuit (bi-state totem-pole outputs, $\overline{SSEQ}$, $\overline{IDEQ}$) and voltage waveforms.

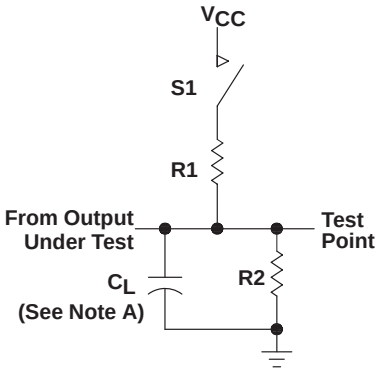
## PARAMETER MEASUREMENT INFORMATION



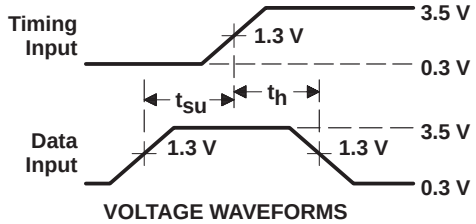

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS
SSEQ, IDEQ



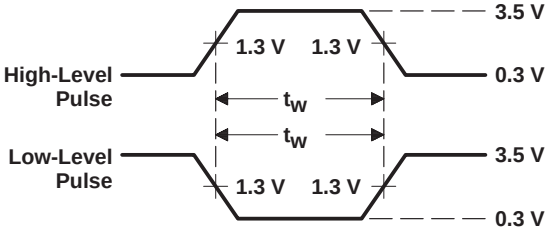

LOAD CIRCUIT FOR
NuBus™ INTERFACE
AD15–AD0



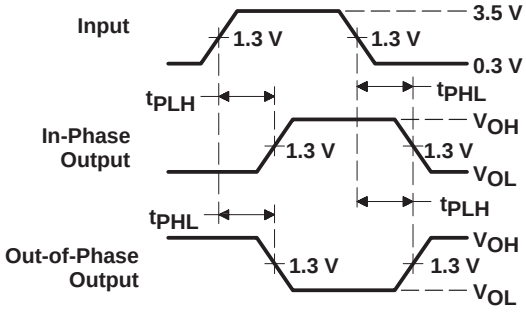

LOAD CIRCUIT FOR
3–STATE OUTPUTS
A15–A0, D15–D0



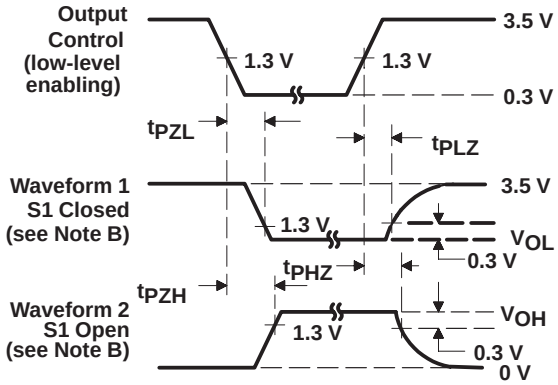

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES,3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
C. C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1**

## APPLICATION INFORMATION

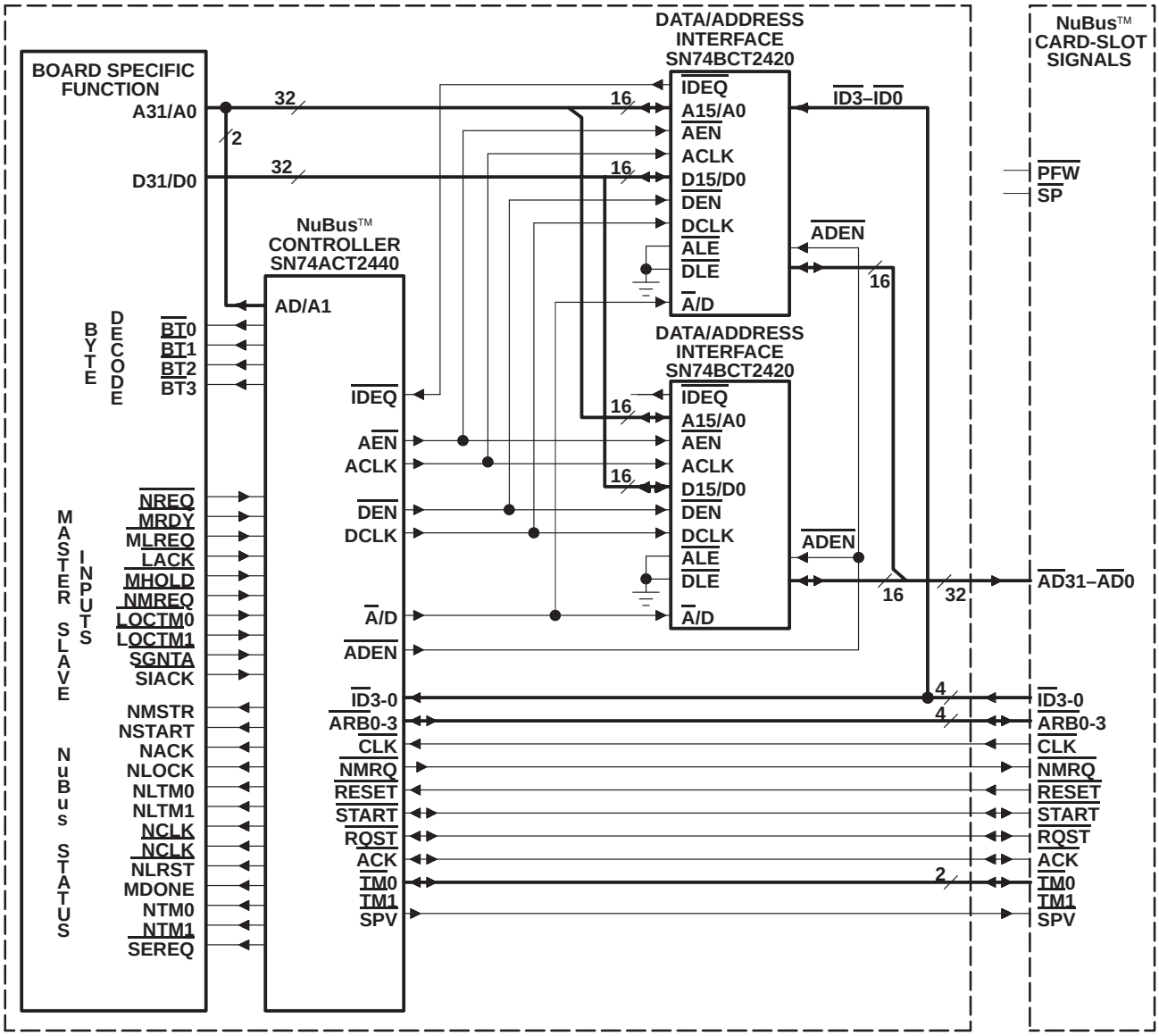



**Figure 2. Typical Nubus™ Interface**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74BCT2420FN | OBSOLETE | PLCC | FN | 68 | | TBD | Call TI | Call TI |
| SN74BCT2420FNR | OBSOLETE | PLCC | FN | 68 | | TBD | Call TI | Call TI |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265