

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (L^2 - π -MOSVI)

2SJ537

Chopper Regulator, DC-DC Converter and Motor Drive Applications

Unit: mm

- Low drain-source ON resistance : $R_{DS(ON)} = 0.16 \Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 3.5 S$ (typ.)
- Low leakage current : $I_{DSS} = -100 \mu A$ ($V_{DS} = -50 V$)
- Enhancement mode : $V_{th} = -0.8$ to $-2.0 V$ ($V_{DS} = -10 V$, $I_D = -1 mA$)

Absolute Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-50	V
Drain-gate voltage ($R_{GS} = 20 k\Omega$)		V_{DGR}	-50	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	-5	A
	Pulse (Note 1)	I_{DP}	-15	A
Drain power dissipation		P_D	0.9	W
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	-55~150	$^\circ C$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

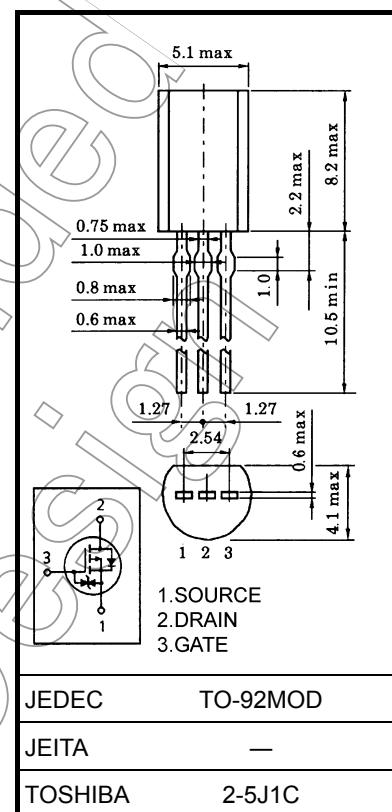
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	138	$^\circ C / W$

Note 1: Please use devices on condition that the channel temperature is below $150^\circ C$.

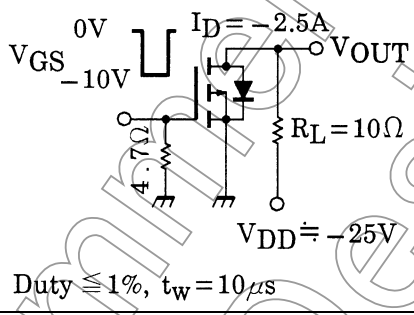
This transistor is an electrostatic sensitive device.

Please handle with caution.



Weight: 0.36 g (typ.)

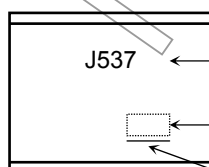
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-100	μA
Drain-source breakdown voltage		$V_{(BR) DSS}$	$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-50	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ mA}$	-0.8	—	-2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = -4 \text{ V}, I_D = -1.3 \text{ A}$	—	0.27	0.34	Ω
			$V_{GS} = -10 \text{ V}, I_D = -2.5 \text{ A}$	—	0.16	0.19	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10 \text{ V}, I_D = -2.5 \text{ A}$	1.5	3.5	—	S
Input capacitance		C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	470	—	pF
Reverse transfer capacitance		C_{rss}		—	60	—	
Output capacitance		C_{oss}		—	210	—	
Switching time	Rise time	t_r	 $I_D = -2.5 \text{ A}$ $V_{GS} = 0 \text{ V}, -10 \text{ V}$ $R_L = 10 \Omega$ $V_{DD} = -25 \text{ V}$ Duty $\leq 1\%$, $t_w = 10 \mu\text{s}$	—	25	—	ns
	Turn-on time	t_{on}		—	35	—	
	Fall time	t_f		—	20	—	
	Turn-off time	t_{off}		—	120	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} = -40 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	—	18	—	nC
Gate-source charge		Q_{gs}		—	13	—	
Gate-drain ("miller") charge		Q_{gd}		—	5	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	-5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	-15	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = -5 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	1.5	V

Marking



Part No. (or abbreviation code)

Lot No.

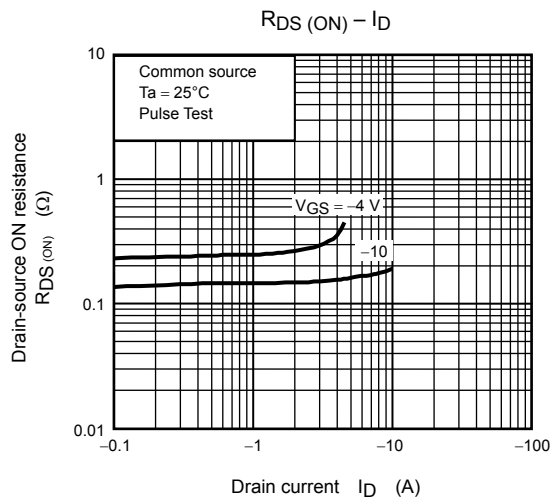
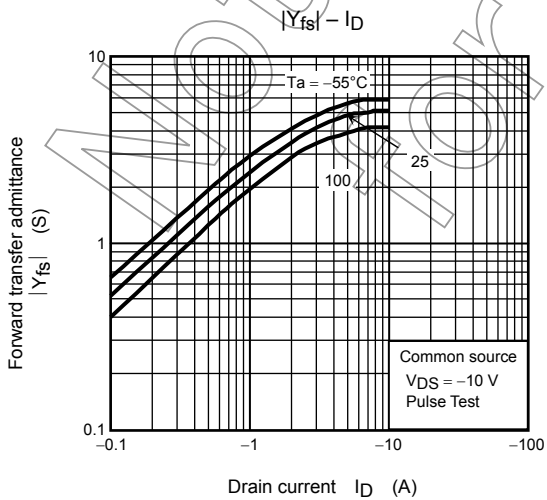
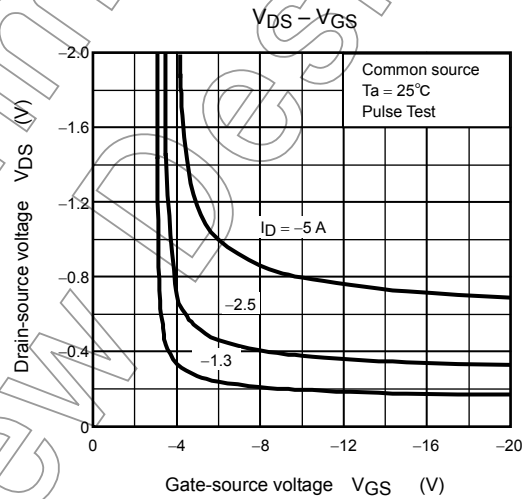
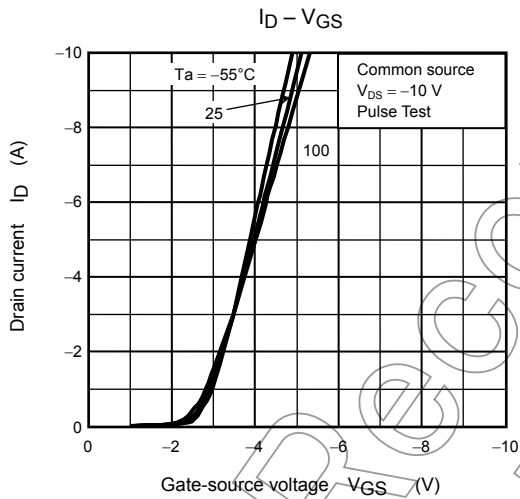
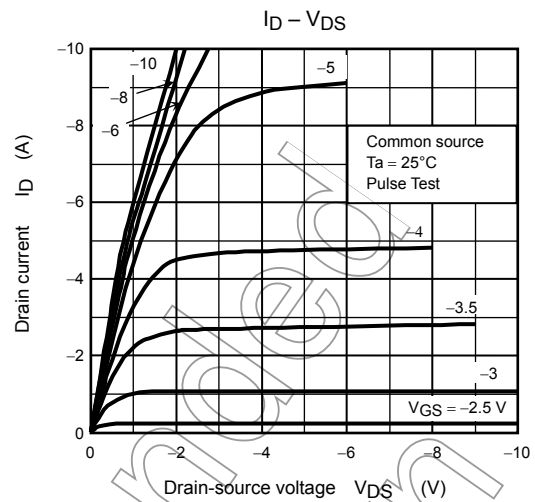
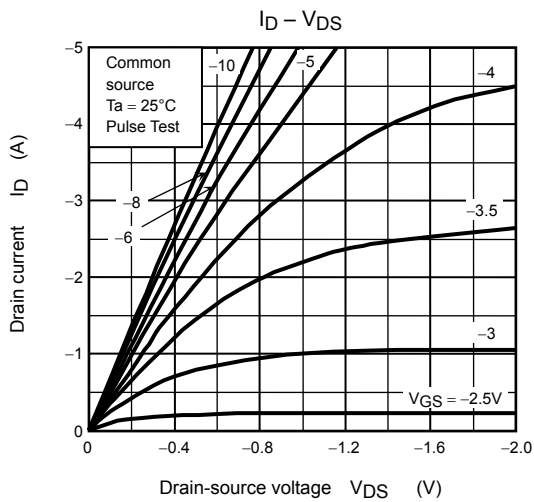
Note 2

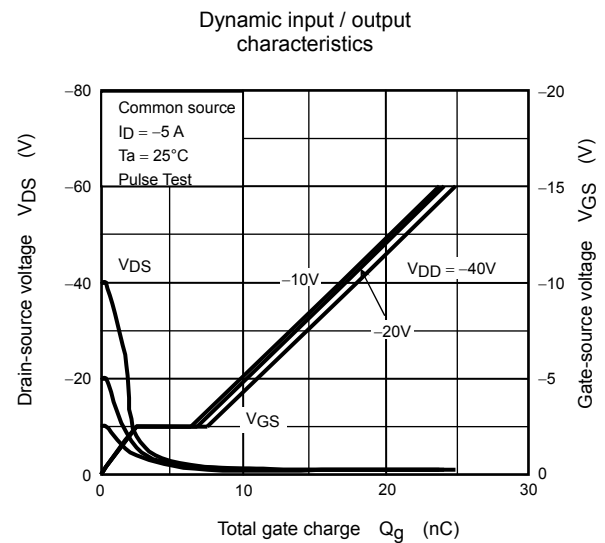
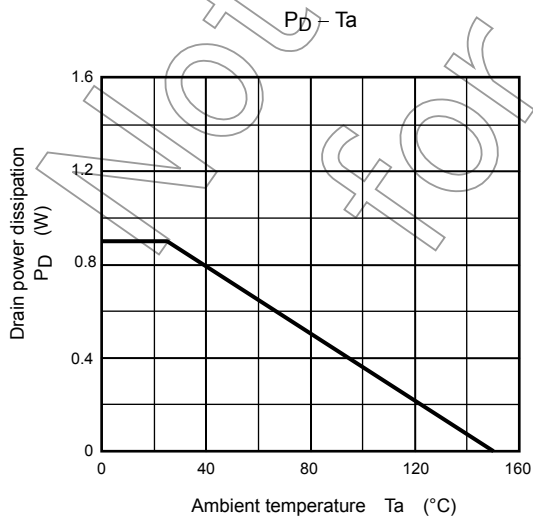
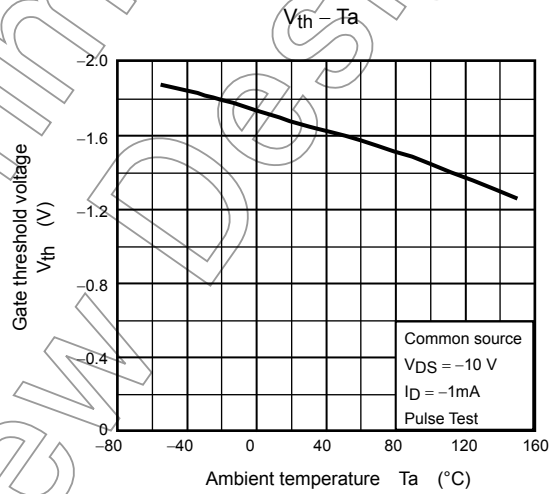
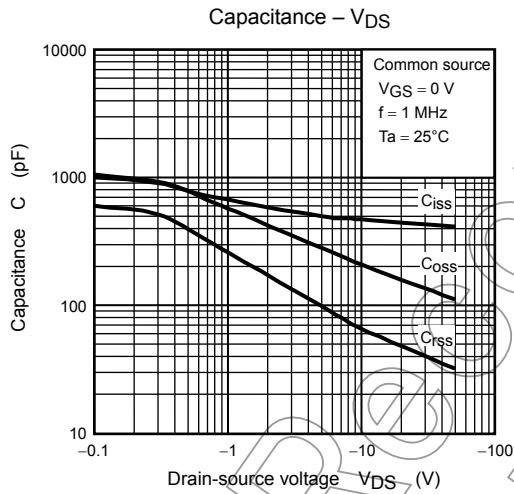
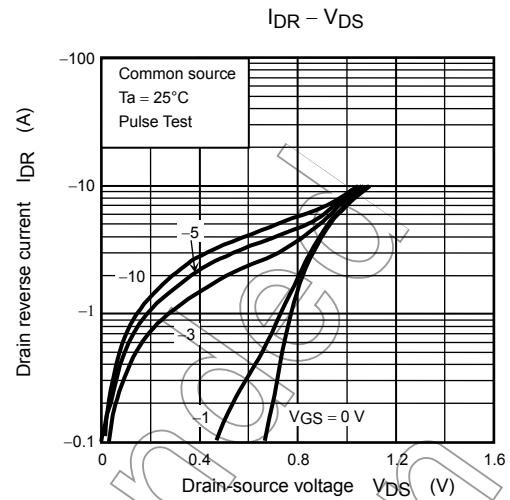
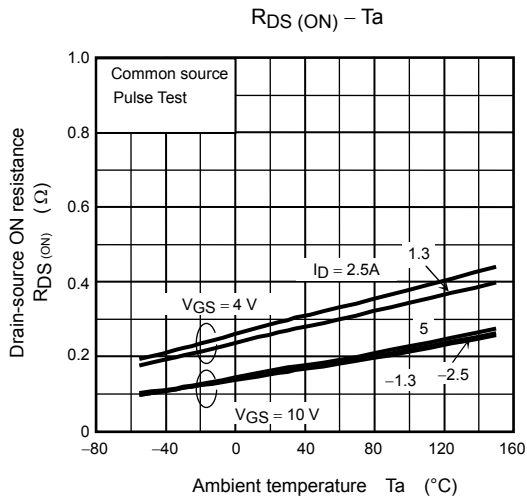
Note 2: A line under a Lot No. identifies the indication of product Labels.

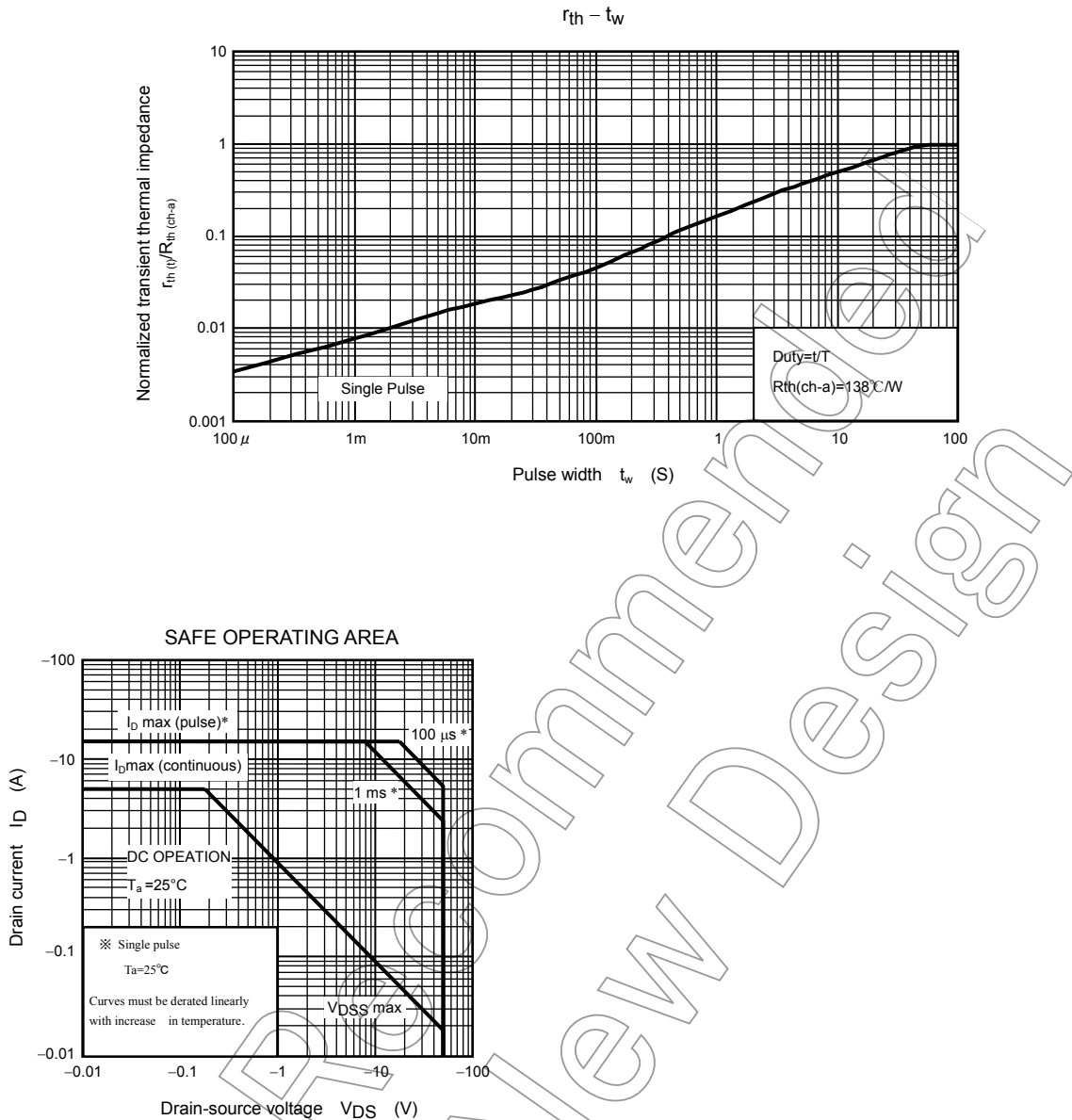
Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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