

74LVC2G53

2-channel analog multiplexer/demultiplexer

Rev. 9 — 5 April 2013

Product data sheet

1. General description

The 74LVC2G53 is a low-power, low-voltage, high-speed, Si-gate CMOS device.

The 74LVC2G53 provides one analog multiplexer/demultiplexer with a digital select input (S), two independent inputs/outputs (Y0 and Y1), a common input/output (Z) and an active LOW enable input ($\overline{E}$). When pin $\overline{E}$ is HIGH, the switch is turned off.

Schmitt trigger action at the select and enable inputs makes the circuit tolerant of slower input rise and fall times across the entire V_{CC} range from 1.65 V to 5.5 V.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - ◆ 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - ◆ 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - ◆ 6 Ω (typical) at $V_{CC} = 5$ V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low-power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD 78 Class I
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Control inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G53DP	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G53DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G53GT	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G53GF	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74LVC2G53GD	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2
74LVC2G53GM	−40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2
74LVC2G53GN	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC2G53GS	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC2G53DC	V53
74LVC2G53DP	V53
74LVC2G53GT	V53
74LVC2G53GF	V3
74LVC2G53GD	V53
74LVC2G53GM	V53
74LVC2G53GN	V3
74LVC2G53GS	V3

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

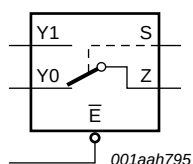


Fig 1. Logic symbol

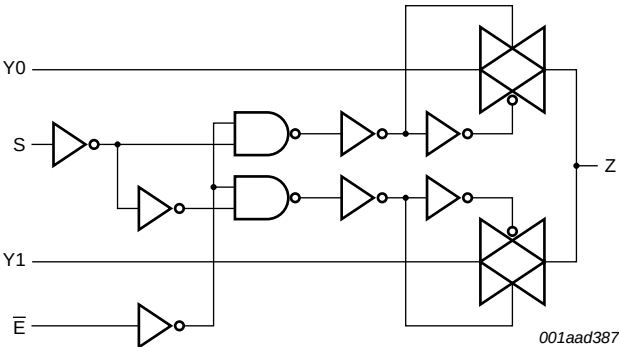


Fig 2. Logic diagram

6. Pinning information

6.1 Pinning

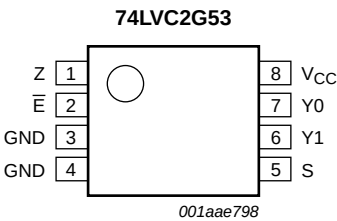


Fig 3. Pin configuration SOT505-2 and SOT765-1

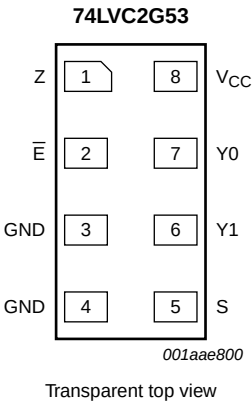
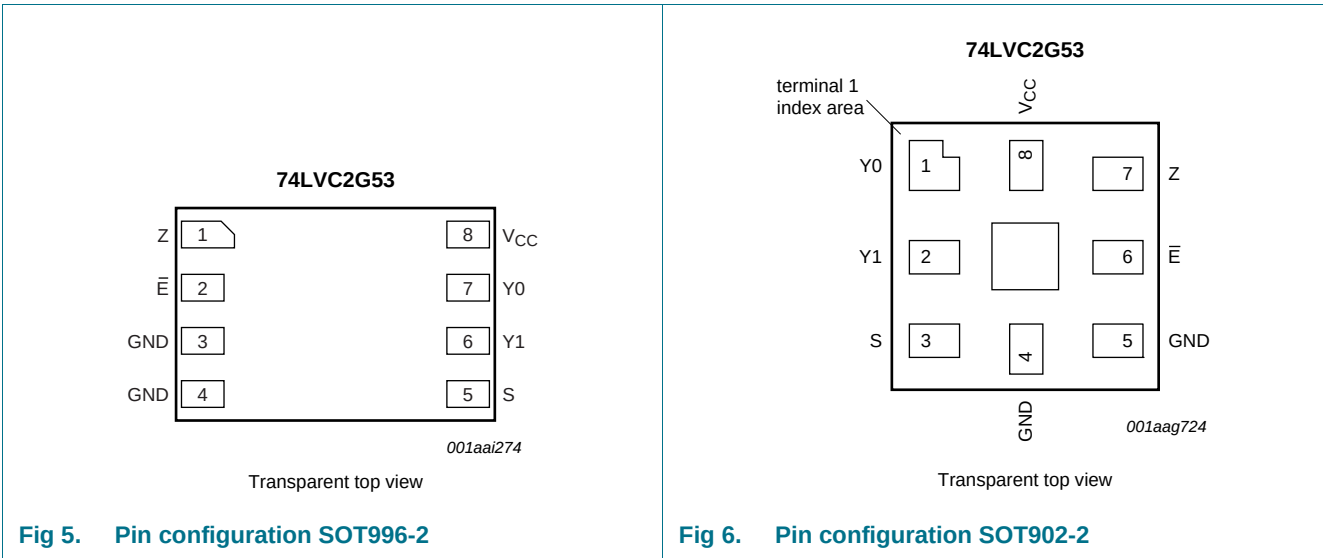


Fig 4. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203



6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-2	
Z	1	7	common output or input
$\overline{E}$	2	6	enable input (active LOW)
GND	3	5	ground (0 V)
GND	4	4	ground (0 V)
S	5	3	select input
Y1	6	2	independent input or output
Y0	7	1	independent input or output
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Channel on
S	$\overline{E}$	
L	L	Y0 to Z or Z to Y0
H	L	Y1 to Z or Z to Y1
X	H	Z (switch off)

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		[1] -0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode	[2] -0.5	$V_{CC} + 0.5$	V
I_{SW}	switch current	$V_{SW} > -0.5\text{ V}$ or $V_{SW} < V_{CC} + 0.5\text{ V}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[3] -	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.

For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_{SW}	switch voltage	enable and disable mode	[1] 0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V}$ to 2.7 V	[2] -	20	ns/V
		$V_{CC} = 2.7\text{ V}$ to 5.5 V	[2] -	10	ns/V

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

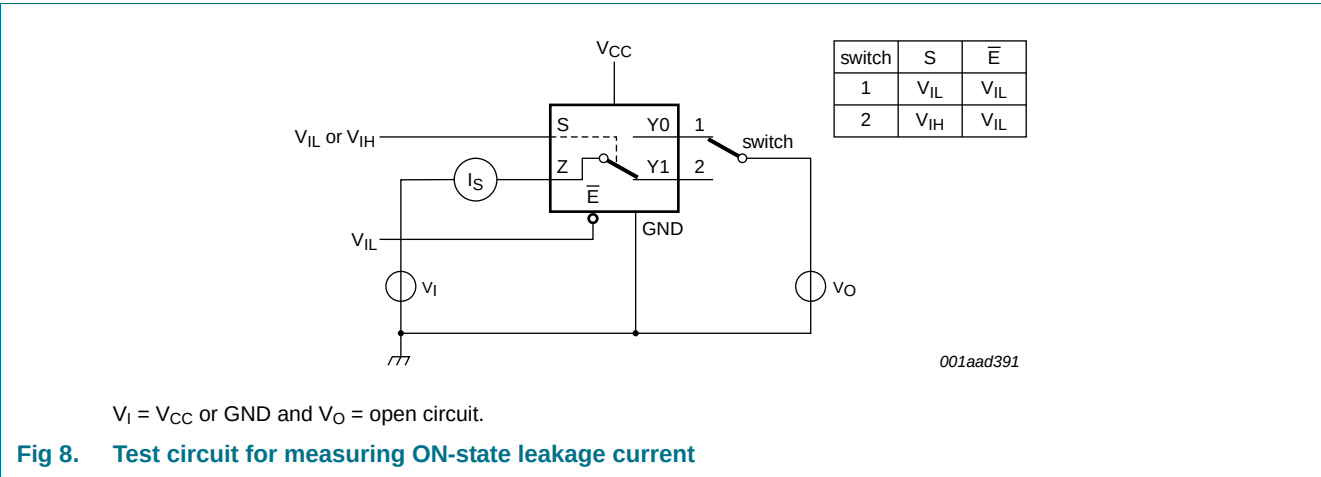
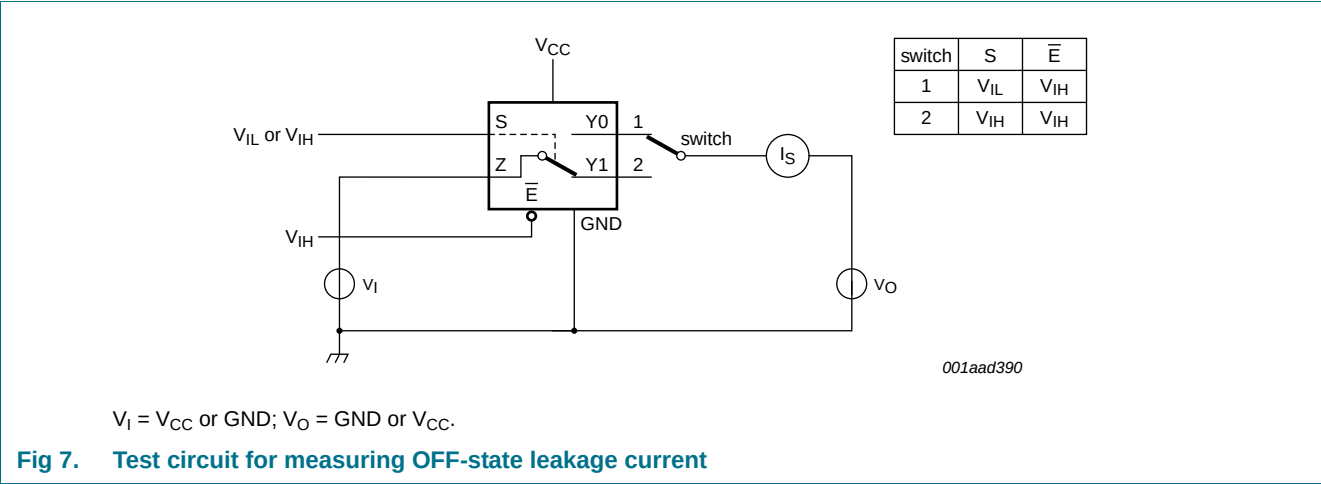
At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = −40 °C to +85 °C			T _{amb} = −40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V	
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V	
		V _{CC} = 3 V to 3.6 V	2.0	-	-	2.0	-	V	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	0.7 × V _{CC}	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V	
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V	
		V _{CC} = 3 V to 3.6 V	-	-	0.8	-	0.8	V	
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	-	0.3 × V _{CC}	V	
I _I	input leakage current	pin S and pin $\bar{E}$; V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	^[2]	-	±0.1	±2	-	±10	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 5.5 V; see Figure 7	^[2]	-	±0.1	±5	-	±20	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 5.5 V; see Figure 8	^[2]	-	±0.1	±5	-	±20	μA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{SW} = GND or V _{CC} ; V _{CC} = 1.65 V to 5.5 V	^[2]	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	pin S and pin $\bar{E}$; V _I = V _{CC} − 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 5.5 V	^[2]	-	5	500	-	5000	μA
C _I	input capacitance			-	2.5	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance			-	6.0	-	-	-	pF
C _{S(ON)}	ON-state capacitance			-	18	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

10.1 Test circuits



10.2 ON resistance

Table 8. ON resistance
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Figure 10](#) to [Figure 15](#).

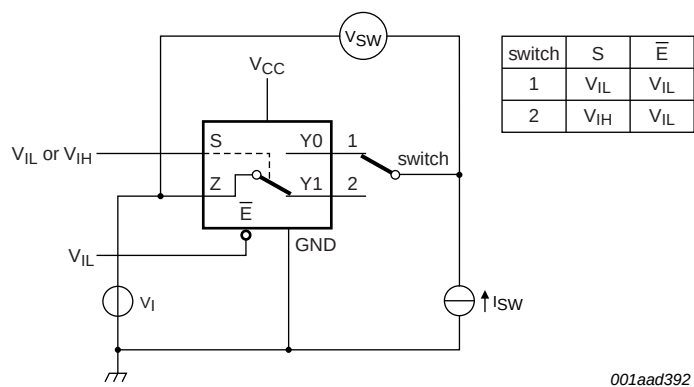
Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_I = GND$ to V_{CC} ; see Figure 9						
		$I_{SW} = 4\text{ mA}$; $V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	34.0	130	-	195	Ω
		$I_{SW} = 8\text{ mA}$; $V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	12.0	30	-	45	Ω
		$I_{SW} = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	10.4	25	-	38	Ω
		$I_{SW} = 24\text{ mA}$; $V_{CC} = 3\text{ V to }3.6\text{ V}$	-	7.8	20	-	30	Ω
		$I_{SW} = 32\text{ mA}$; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	6.2	15	-	23	Ω

Table 8. ON resistance ...continuedAt recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Figure 10](#) to [Figure 15](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see Figure 9						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.5	12	-	18	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V _I = V _{CC} ; see Figure 9						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.1	15	-	23	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} ^[2]						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	2.0	-	-	-	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

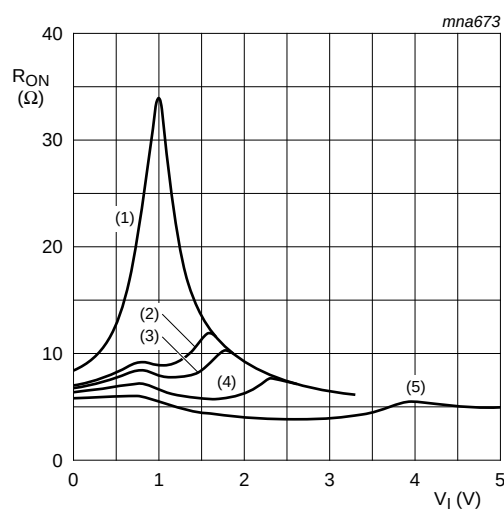
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and graphs



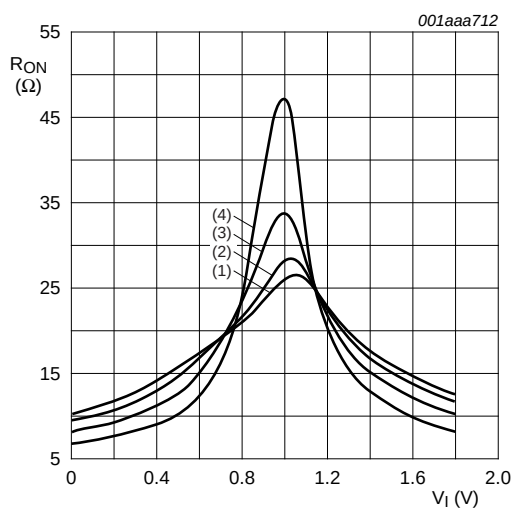
$$R_{ON} = V_{SW} / I_{SW}$$

Fig 9. Test circuit for measuring ON resistance



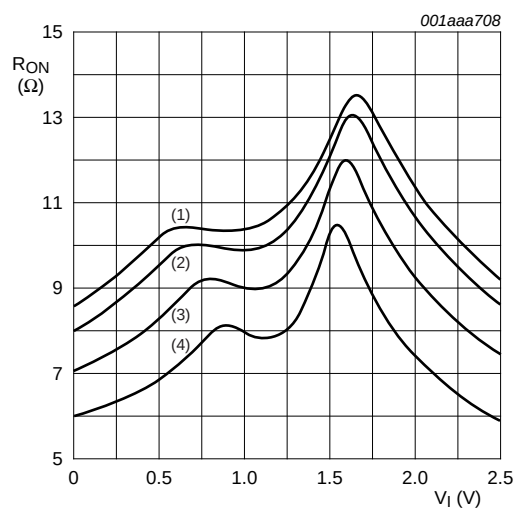
- (1) $V_{CC} = 1.8 \text{ V}$.
- (2) $V_{CC} = 2.5 \text{ V}$.
- (3) $V_{CC} = 2.7 \text{ V}$.
- (4) $V_{CC} = 3.3 \text{ V}$.
- (5) $V_{CC} = 5.0 \text{ V}$.

Fig 10. Typical ON resistance as a function of input voltage; $T_{amb} = 25 \text{ }^{\circ}\text{C}$



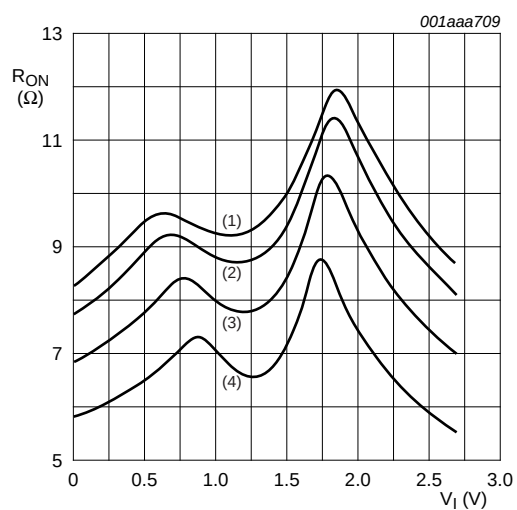
- (1) $T_{amb} = 125 \text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85 \text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

Fig 11. ON resistance as a function of input voltage;
 $V_{CC} = 1.8 \text{ V}$



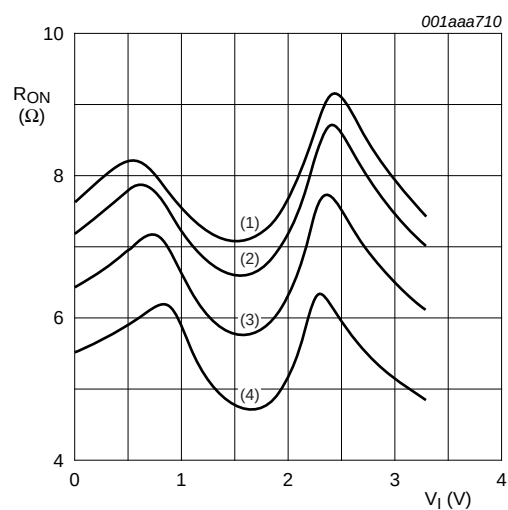
- (1) $T_{amb} = 125 \text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85 \text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

Fig 12. ON resistance as a function of input voltage;
 $V_{CC} = 2.5 \text{ V}$



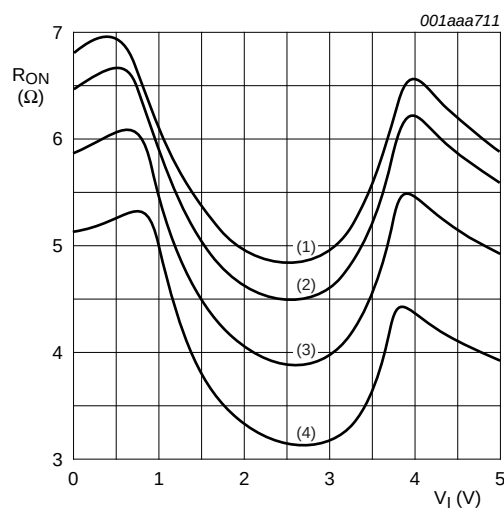
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C.}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C.}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C.}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C.}$

Fig 13. ON resistance as a function of input voltage;
 $V_{CC} = 2.7\text{ V}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C.}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C.}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C.}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C.}$

Fig 14. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C.}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C.}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C.}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C.}$

Fig 15. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 18](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	Z to Yn or Yn to Z; see Figure 16 ^{[2][3]}						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	2	-	2.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	1.2	-	1.5	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	1.0	-	1.25	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	1.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.6	-	0.8	ns
t_{en}	enable time	S to Z or Yn; see Figure 17 ^[4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.6	6.7	10.3	2.6	12.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.9	4.1	6.4	1.9	8.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.9	4.0	5.5	1.8	7.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.8	3.4	5.0	1.8	6.3	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.3	2.6	3.8	1.3	4.8	ns
		$\bar{E}$ to Z or Yn; see Figure 17 ^[4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.9	4.0	7.3	1.9	9.2	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.4	2.5	4.4	1.4	5.5	ns
		$V_{CC} = 2.7 \text{ V}$	1.1	2.6	3.9	1.1	4.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.2	2.2	3.8	1.2	4.8	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	1.7	2.6	1.0	3.3	ns
t_{dis}	disable time	S to Z or Yn; see Figure 17 ^[5]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.1	6.8	10.0	2.1	12.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.4	3.7	6.1	1.4	7.7	ns
		$V_{CC} = 2.7 \text{ V}$	1.4	4.9	6.2	1.4	7.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.1	4.0	5.4	1.1	6.8	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	2.9	3.8	1.0	4.8	ns
		$\bar{E}$ to Z or Yn; see Figure 17 ^[5]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.3	5.6	8.6	2.3	11.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.2	3.2	4.8	1.2	6.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.4	4.0	5.2	1.4	6.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	3.7	5.0	2.0	6.3	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.3	2.9	3.8	1.3	4.8	ns

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and nominal V_{CC} .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

11.1 Waveforms and test circuits

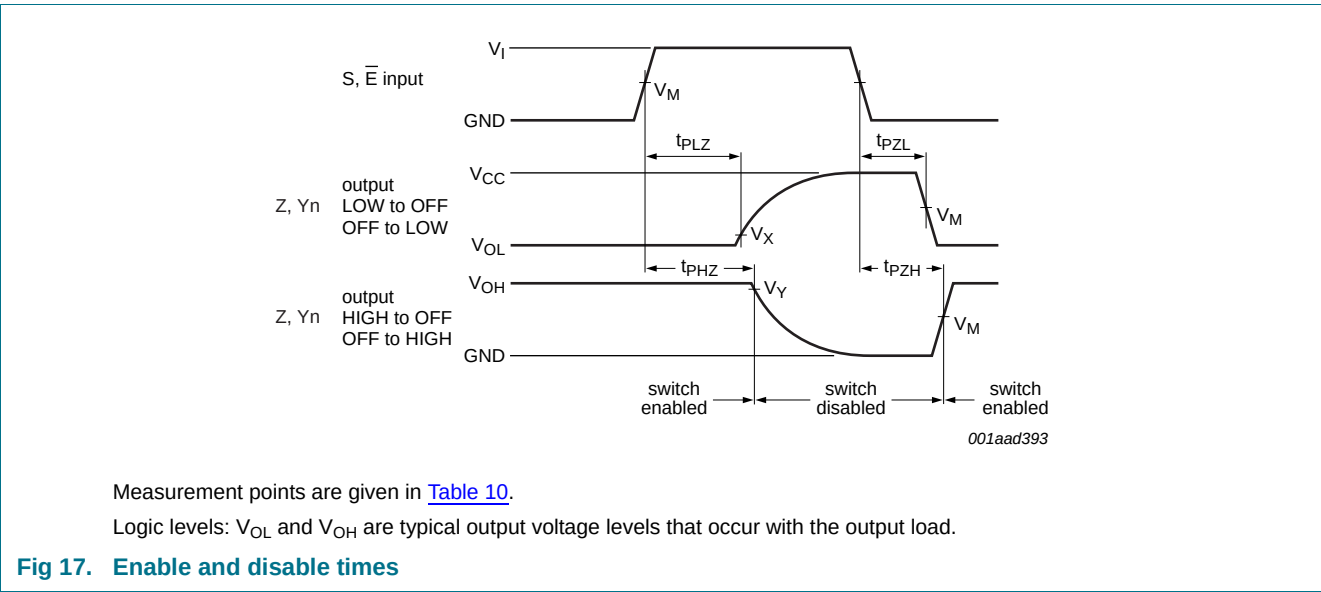
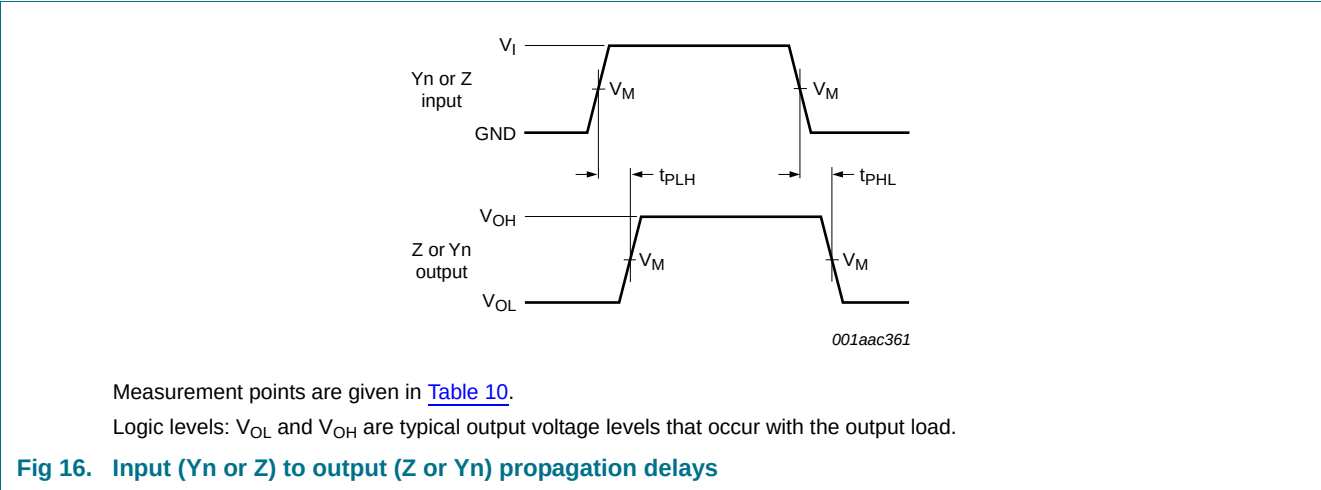
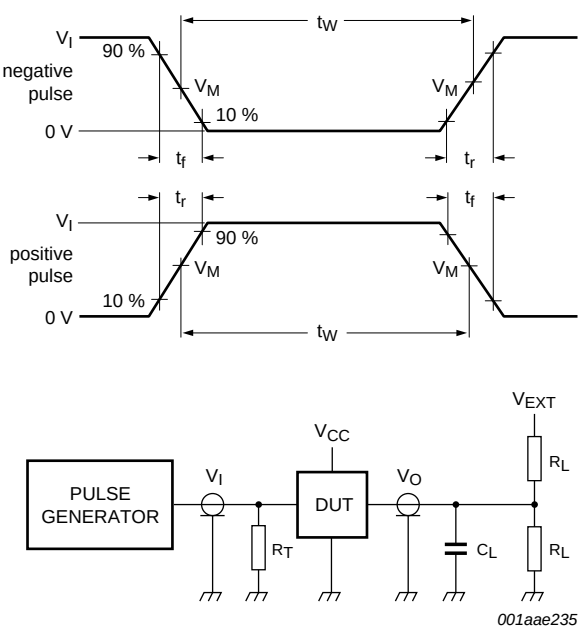


Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
2.7 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 11](#).
Definitions for test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = Test voltage for switching times.

Fig 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$
3 V to 3.6 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 600 \text{ Hz}$ to 20 kHz ; $R_L = 600 \text{ }\Omega$; $C_L = 50 \text{ pF}$; $V_i = 0.5 \text{ V}$ (p-p); see Figure 19				
		$V_{CC} = 1.65 \text{ V}$	-	0.260	-	%
		$V_{CC} = 2.3 \text{ V}$	-	0.078	-	%
		$V_{CC} = 3.0 \text{ V}$	-	0.078	-	%
		$V_{CC} = 4.5 \text{ V}$	-	0.078	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50 \text{ }\Omega$; $C_L = 5 \text{ pF}$; see Figure 20				
		$V_{CC} = 1.65 \text{ V}$	-	200	-	MHz
		$V_{CC} = 2.3 \text{ V}$	-	300	-	MHz
		$V_{CC} = 3.0 \text{ V}$	-	300	-	MHz
		$V_{CC} = 4.5 \text{ V}$	-	300	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 50 \text{ }\Omega$; $C_L = 5 \text{ pF}$; $f_i = 10 \text{ MHz}$; see Figure 21				
		$V_{CC} = 1.65 \text{ V}$	-	-42	-	dB
		$V_{CC} = 2.3 \text{ V}$	-	-42	-	dB
		$V_{CC} = 3.0 \text{ V}$	-	-40	-	dB
		$V_{CC} = 4.5 \text{ V}$	-	-40	-	dB
Q_{inj}	charge injection	$C_L = 0.1 \text{ nF}$; $V_{\text{gen}} = 0 \text{ V}$; $R_{\text{gen}} = 0 \text{ }\Omega$; $f_i = 1 \text{ MHz}$; $R_L = 1 \text{ M}\Omega$; see Figure 22				
		$V_{CC} = 1.8 \text{ V}$	-	3.3	-	pC
		$V_{CC} = 2.5 \text{ V}$	-	4.1	-	pC
		$V_{CC} = 3.3 \text{ V}$	-	5.0	-	pC
		$V_{CC} = 4.5 \text{ V}$	-	6.4	-	pC
		$V_{CC} = 5.5 \text{ V}$	-	7.5	-	pC

11.3 Test circuits

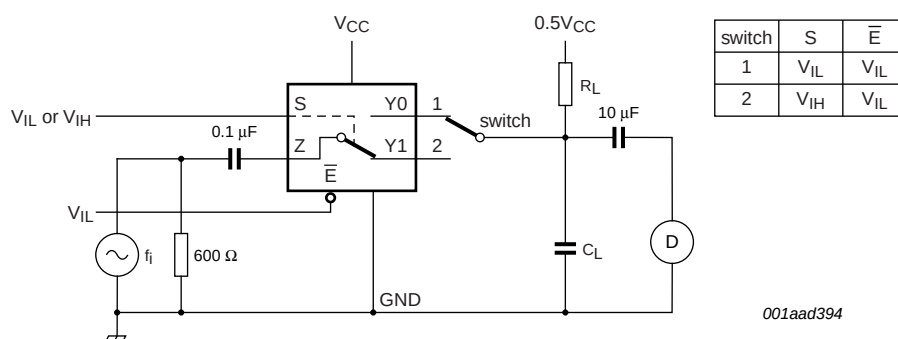
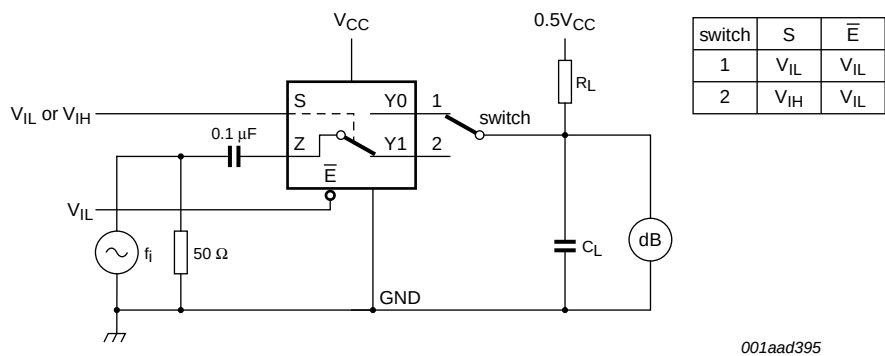
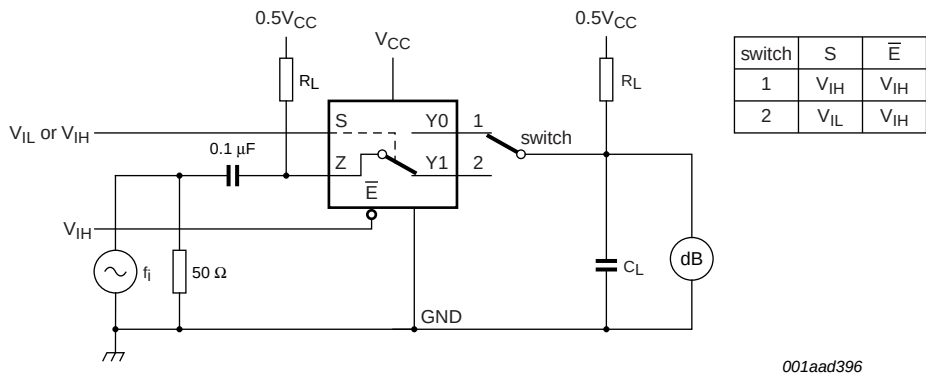


Fig 19. Test circuit for measuring total harmonic distortion



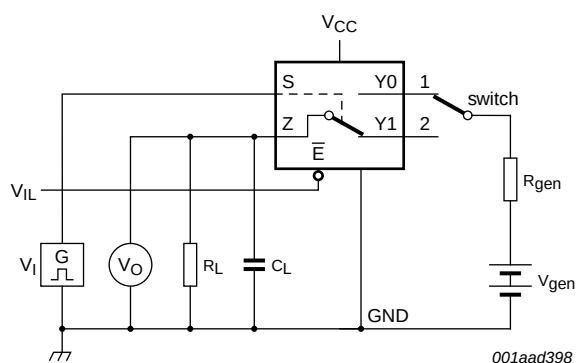
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig 20. Test circuit for measuring the frequency response when switch is in ON-state

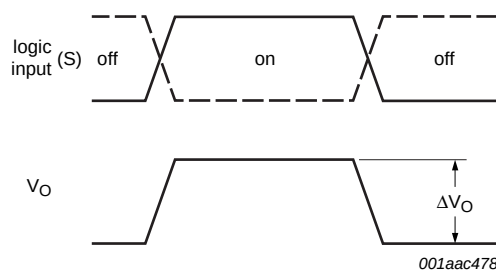


Adjust f_i voltage to obtain 0 dBm level at input.

Fig 21. Test circuit for measuring isolation (OFF-state)



a. Test circuit



b. Input and output pulse definitions

$$Q_{inj} = \Delta V_O \times C_L$$

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 22. Test circuit for measuring charge injection

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

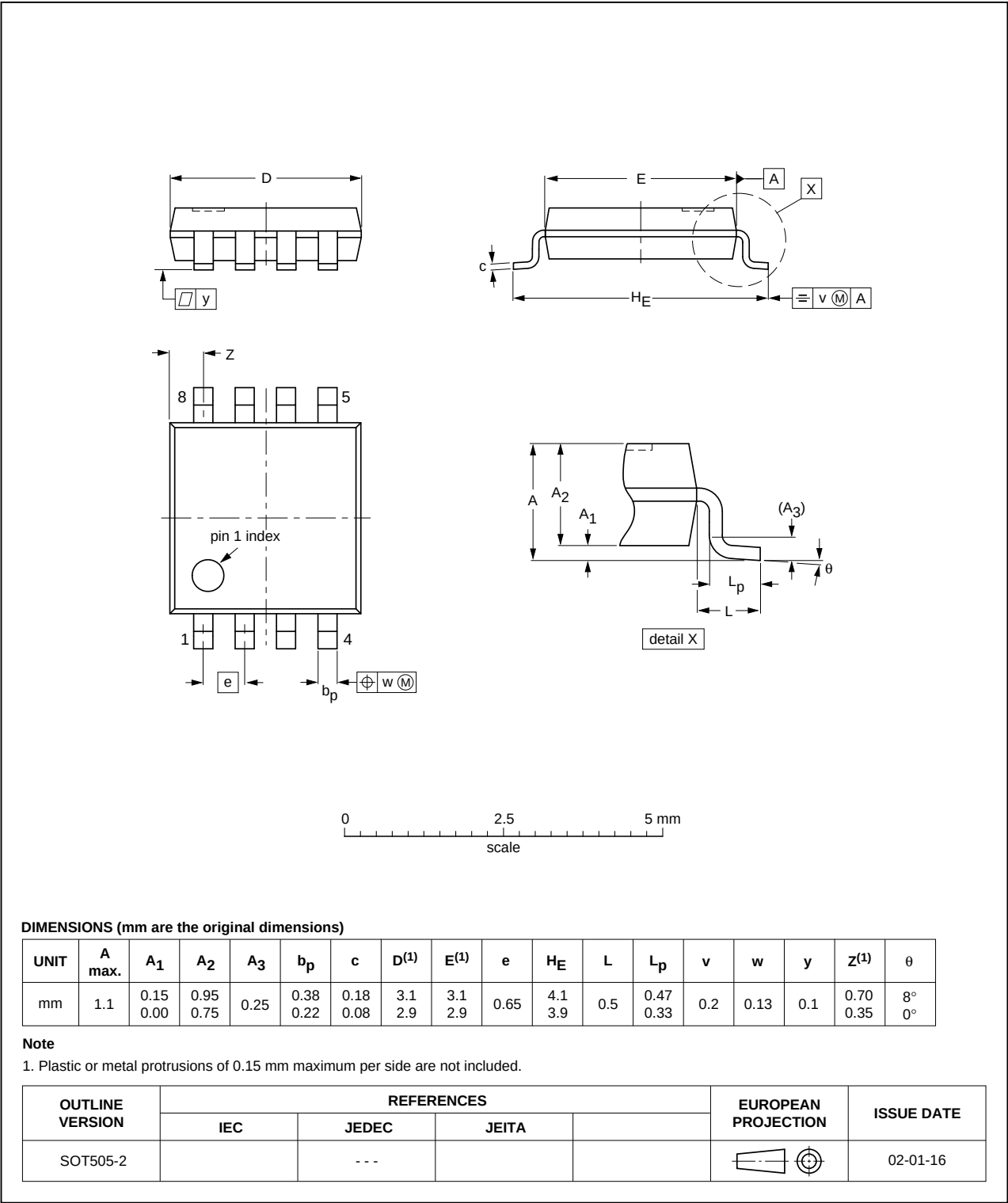


Fig 23. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

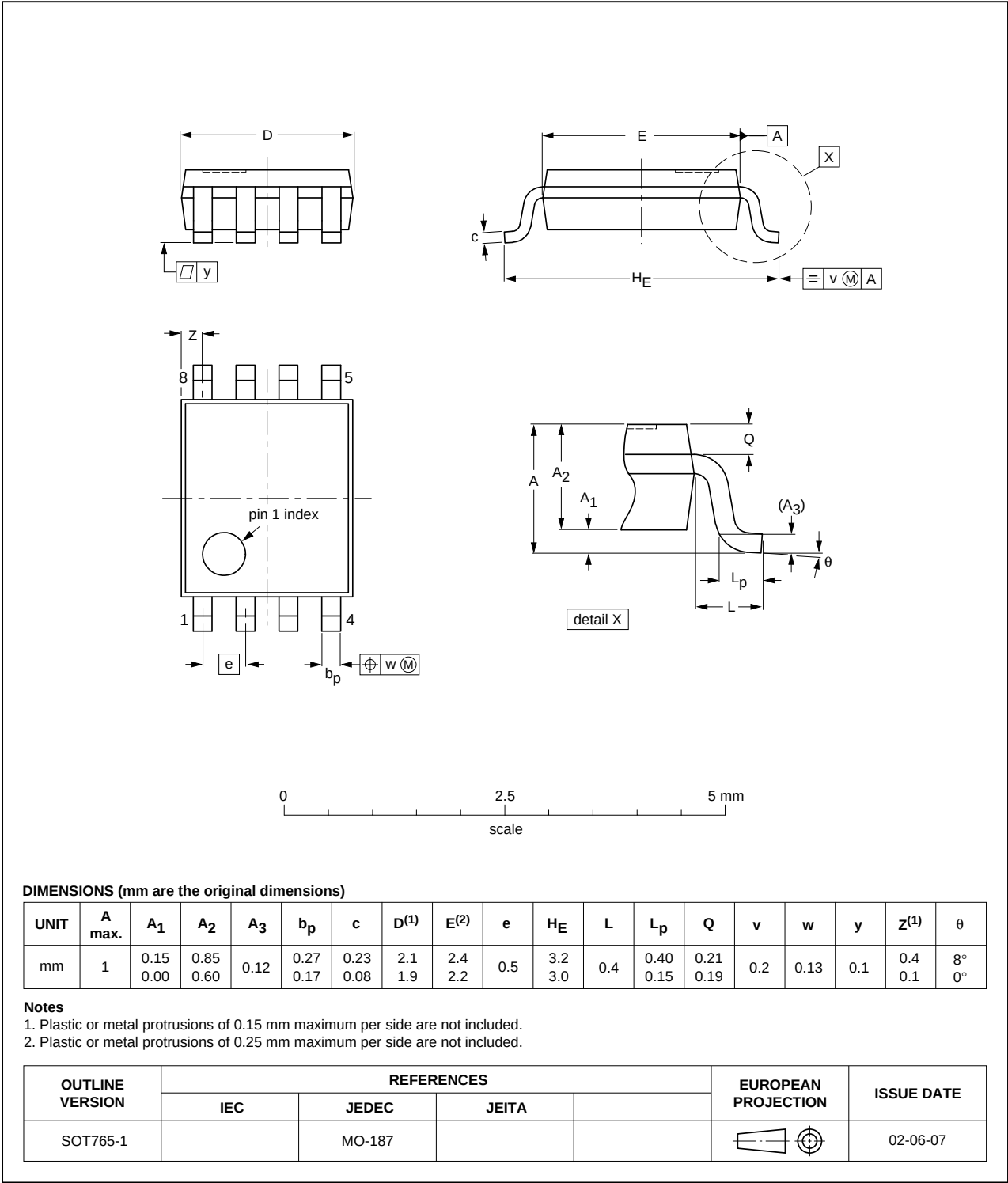


Fig 24. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

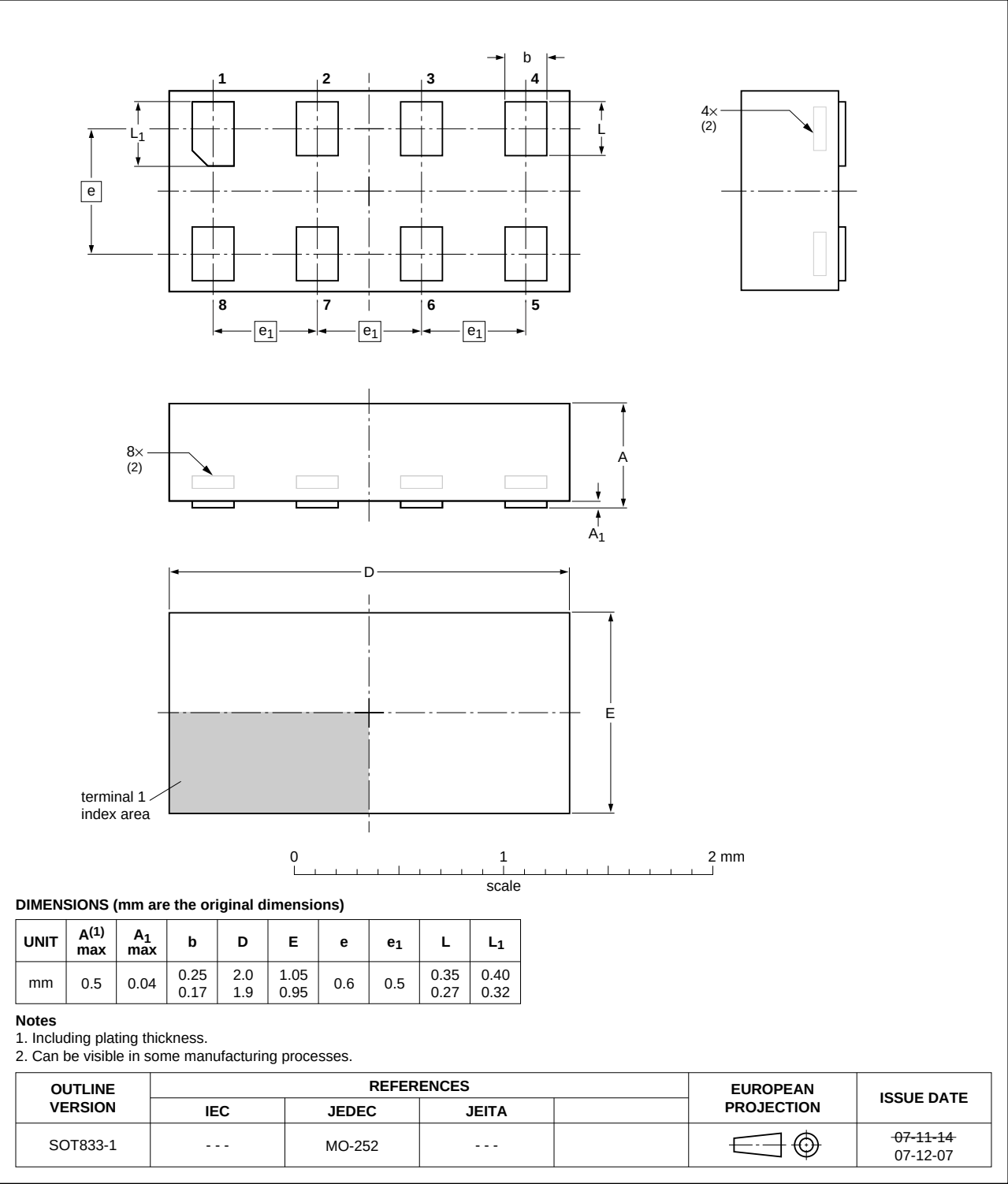


Fig 25. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

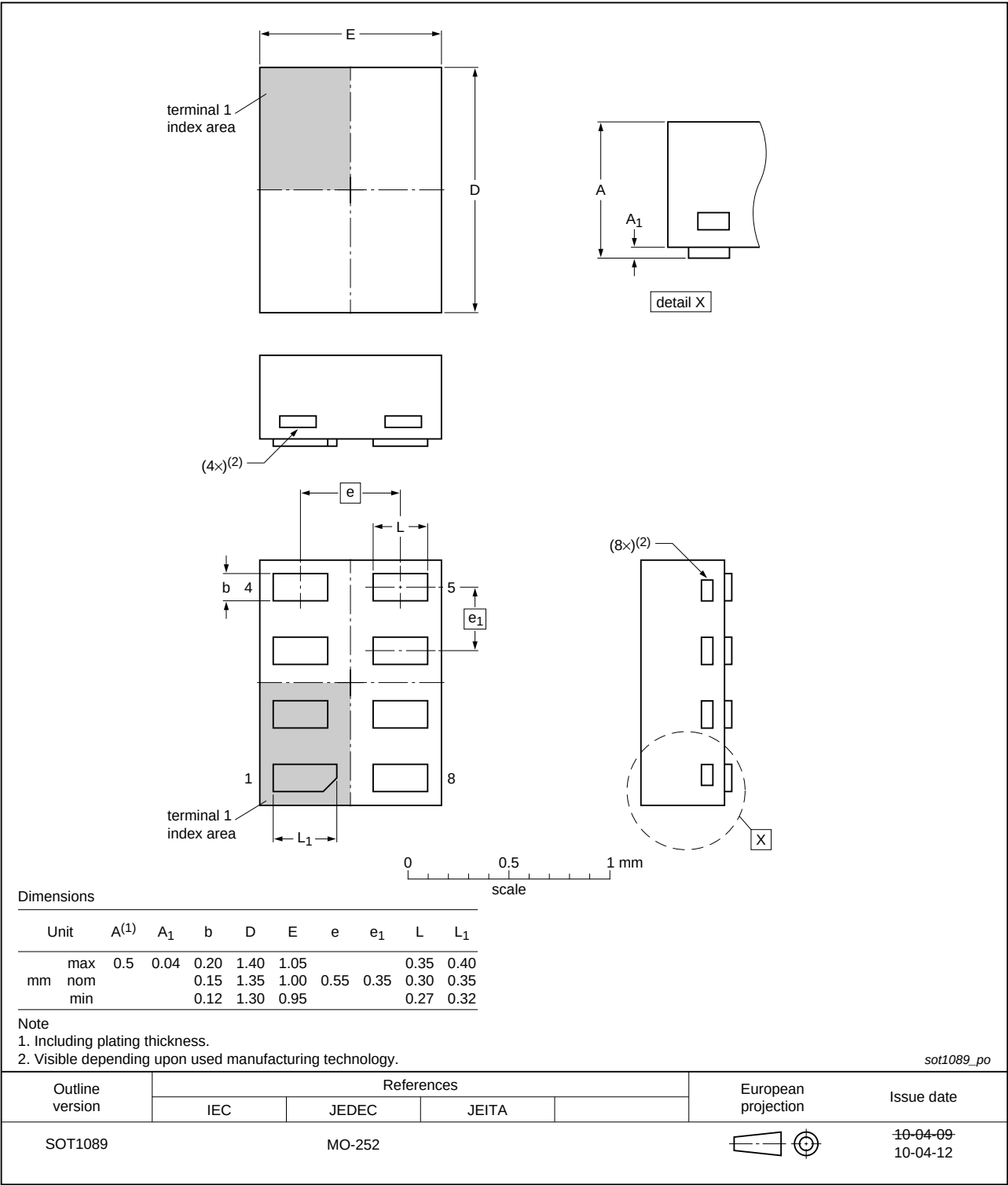


Fig 26. Package outline SOT1089 (XSON8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

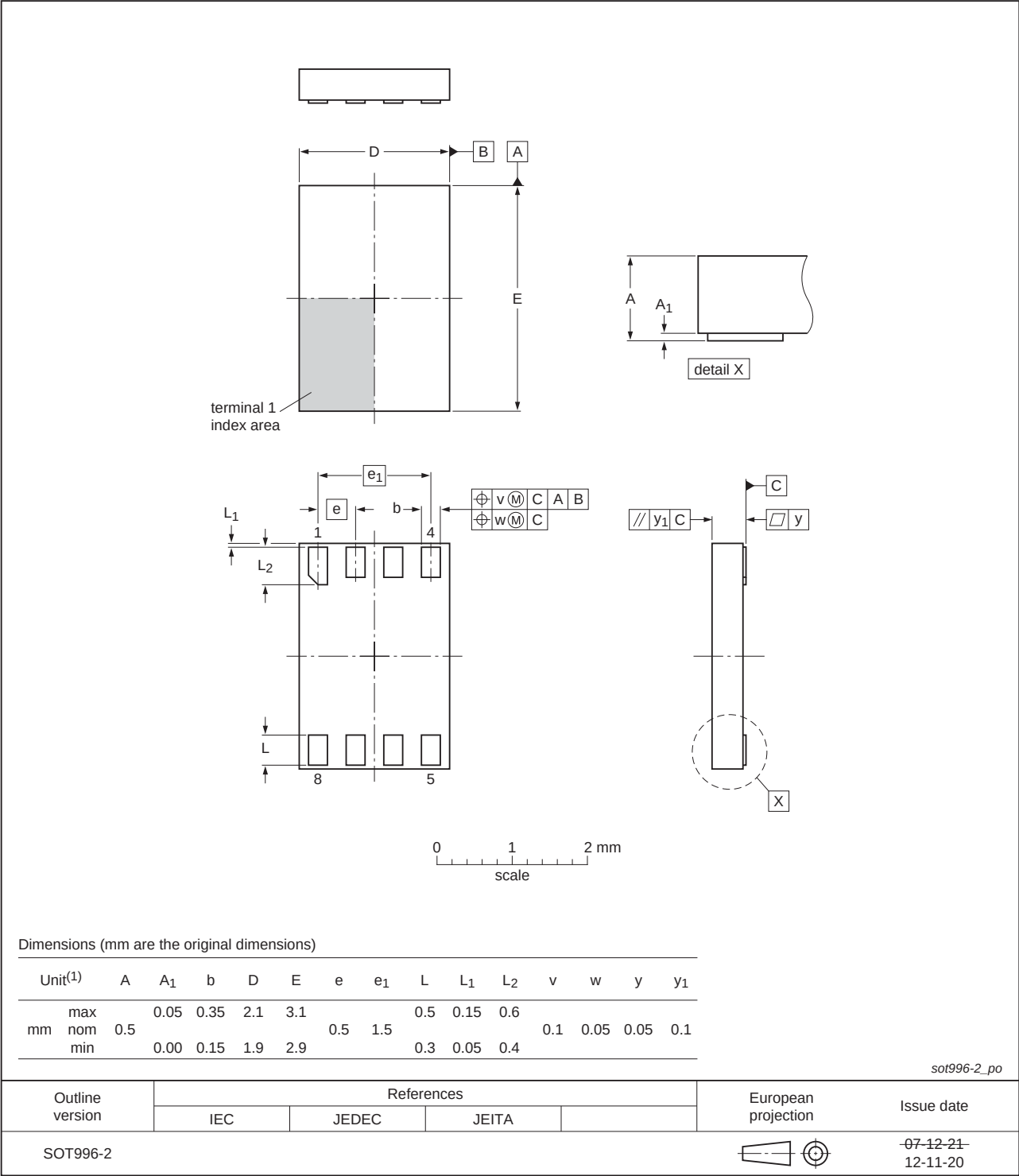


Fig 27. Package outline SOT996-2 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

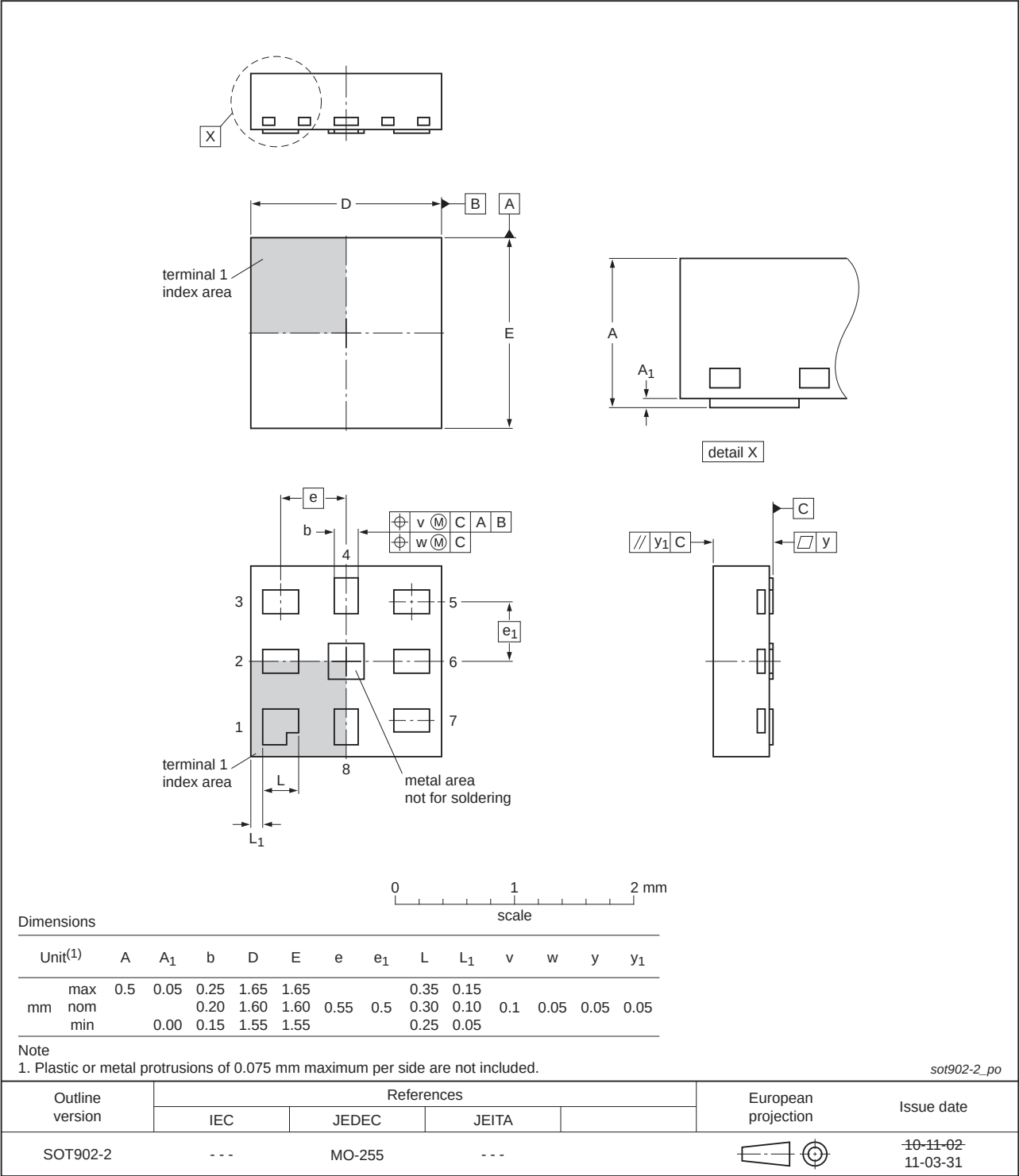


Fig 28. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

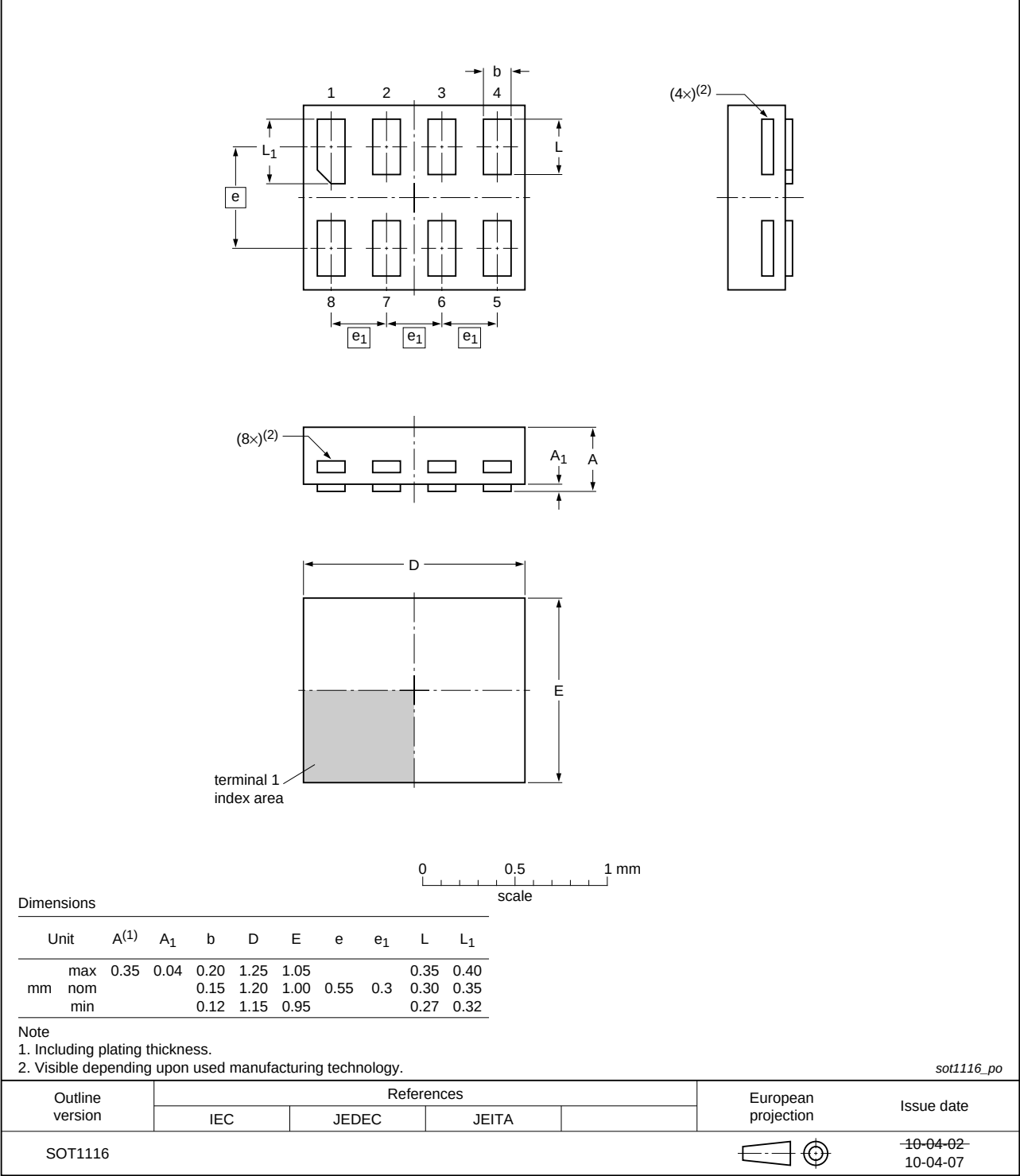


Fig 29. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

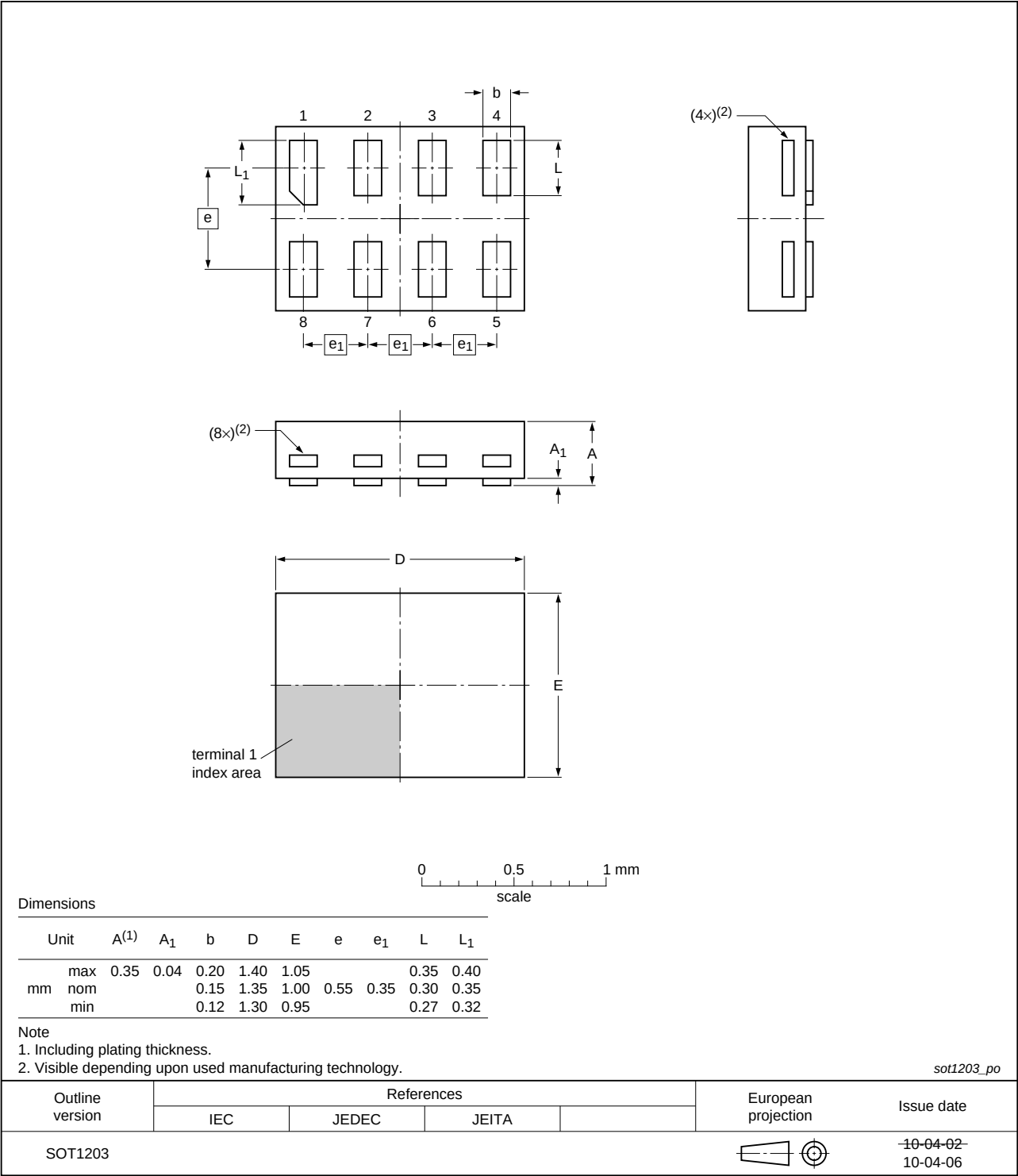


Fig 30. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
TTL	Transistor-Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
CDM	Charged Device Model
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G53 v.9	20130405	Product data sheet	-	74LVC2G53 v.8
Modifications:	For type number 74LVC2G53GD XSON8U has changed to XSON8.			
74LVC2G53 v.8	20120622	Product data sheet	-	74LVC2G53 v.7
Modifications:	For type number 74LVC2G53GM the SOT code has changed to SOT902-2.			
74LVC2G53 v.7	20111125	Product data sheet	-	74LVC2G53 v.6
Modifications:	Legal pages updated.			
74LVC2G53 v.6	20100927	Product data sheet	-	74LVC2G53 v.5
74LVC2G53 v.5	20080618	Product data sheet	-	74LVC2G53 v.4
74LVC2G53 v.4	20080228	Product data sheet	-	74LVC2G53 v.3
74LVC2G53 v.3	20070828	Product data sheet	-	74LVC2G53 v.2
74LVC2G53 v.2	20060331	Product data sheet	-	74LVC2G53 v.1
74LVC2G53 v.1	20060110	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	4
8	Limiting values	5
9	Recommended operating conditions	5
10	Static characteristics	6
10.1	Test circuits	7
10.2	ON resistance	7
10.3	ON resistance test circuit and graphs	8
11	Dynamic characteristics	11
11.1	Waveforms and test circuits	12
11.2	Additional dynamic characteristics	14
11.3	Test circuits	14
12	Package outline	17
13	Abbreviations	25
14	Revision history	25
15	Legal information	26
15.1	Data sheet status	26
15.2	Definitions	26
15.3	Disclaimers	26
15.4	Trademarks	27
16	Contact information	27
17	Contents	28

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Date of release: 5 April 2013

Document identifier: 74LVC2G53