March 1997
Revision 2.1

FUJITSU

DATA SHEET

SOB2UV6412-(67/84/100/125)T-S

16MByte (2M x 64) CMOS Synchronous DRAM Module

General Description

The SOB2UV6412-(67/84/100/125)T-S is a high performance, 16-megabtye synchronous, dynamic RAM module organized as 2M words by 64 bits, in a 144-pin, small outline dual-in-line memory module (SODIMM) package.

The module utilizes eight Fujitsu MB811171622A-(67/84/100/125) PFTN CMOS 1Mx16 synchronous dynamic RAMs in surface mount package (TSOP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

A 256 Byte Serial EEPROM contains the module configuration information.

Features

- High Density 16MByte
- Cycle Time: 8ns (125 MHz), 10ns (100 MHz), 12ns (84 MHz), 15ns (67 MHz)
- Low Power: Active 2.9W (125 MHz), 2.7W (100 MHz), 2.5W (84 MHz), 2.4W (67 MHz)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.000 inch

ABSOLUTE MAXIMUM RATINGS

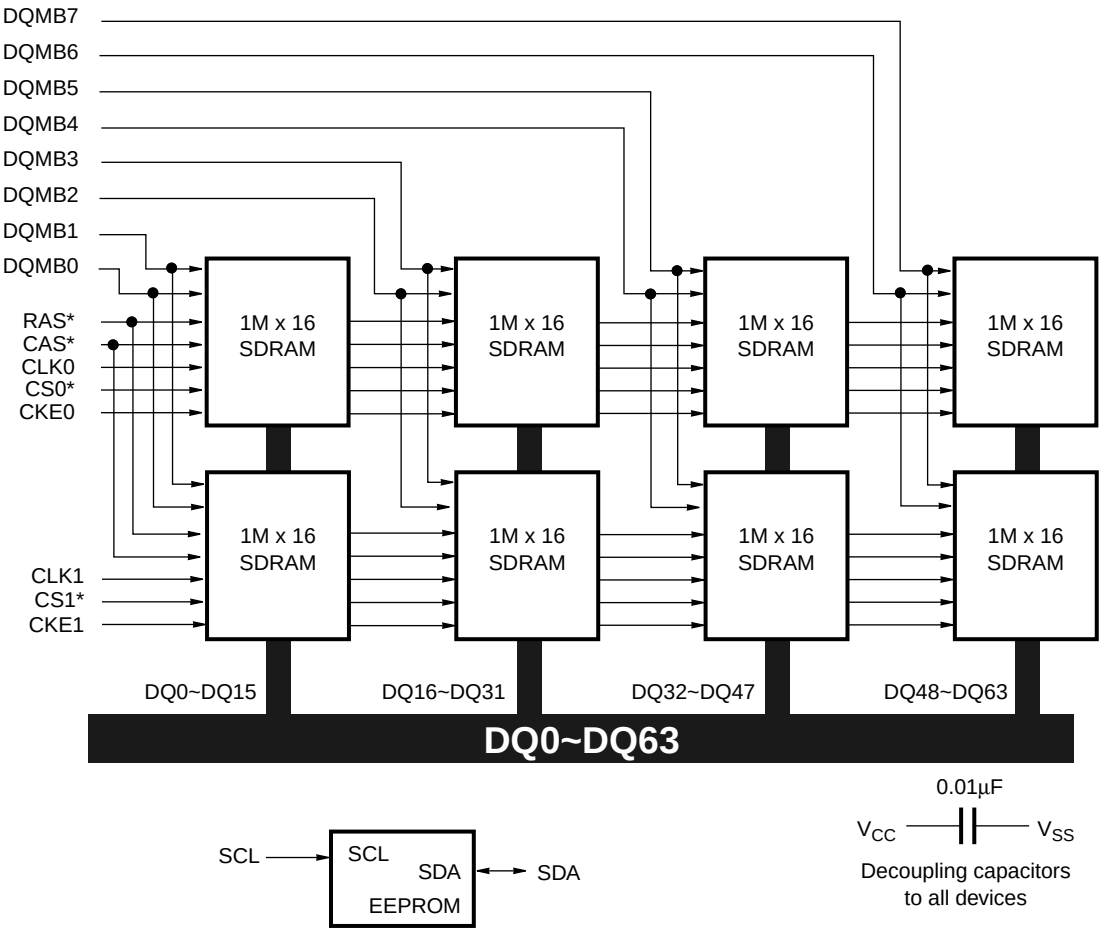
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	10.4	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	±50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.5	V
V_{IL}	Input Low voltage	-0.5	-	0.8	V

Functional Diagram

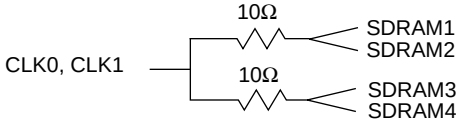


(All specifications of the device are subject to change without notice.)

Notes:
1. WE* and Addresses A~A10, BA0 to all the devices.
2. CLKs are terminated using 10 ohm series resistors.
3. A0~A2 of serial PD EEPROM are grounded.
4. DQMs vs Data I/Os

DQMB0 controls	DQ0 ~ DQ7
DQMB1 controls	DQ8 ~ DQ15
DQMB2 controls	DQ16 ~ DQ23
DQMB3 controls	DQ24 ~ DQ31
DQMB4 controls	DQ32 ~ DQ39
DQMB5 controls	DQ40 ~ DQ47
DQMB6 controls	DQ48 ~ DQ55
DQMB7 controls	DQ56 ~ DQ63

5. Clock Wiring



Pin Name

A0~A10/AP	Row Addresses	DQMB0-DQMB7	DQ Mask Enables
A0~A7	Column Addresses	CS0*, CS1*	Chip Select
BA0	Bank Select Address	WE*	Write Enable
DQ0~DQ63	Data Inputs/Outputs	SCL	Serial Clock
CLK0, CLK1	Clock Inputs	SDA	Serial Data Input/Output
RAS*	Row Address Strobes	V_{CC}	Power Supply
CAS*	Column Address Strobes	V_{SS}	Ground
CKE0, CKE1	Clock Enables	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	2	V_{SS}	73	NC	74	CLK1
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{CC}	82	V_{CC}
11	V_{CC}	12	V_{CC}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	V_{CC}	28	V_{CC}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{CC}	102	V_{CC}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0 (Note)
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	NC
39	DQ9	40	DQ41	111	A10/AP (Note)	112	NC
41	DQ10	42	DQ42	113	V_{CC}	114	V_{CC}
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	V_{CC}	46	V_{CC}	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V_{SS}	56	V_{SS}	127	DQ27	128	DQ59
57	NC	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	V_{CC}	64	V_{CC}	135	DQ30	136	DQ62
65	RAS*	66	CAS*	137	DQ31	138	DQ63
67	WE*	68	CKE1	139	V_{SS}	140	V_{SS}
69	CS0*	70	NC	141	SDA	142	SCL
71	CS1*	72	NC	143	V_{CC}	144	V_{CC}

Notes: 1. Address A10 : Initiates Auto-Precharge
2. Address BA0 : Bank select within the SDRAM devices.

SERIAL PD INFORMATION

Byte#	Function Described	Function Supported	Hex Value
0	# Bytes Written into serial memory at module mfr	128 bytes	80h
1	Total # bytes of SPD memory device	256 bytes	08h
2	Fundamental memory type	SDRAM	04h
3	# Row Address on this assembly	11	0Bh
4	# Column Addresses on this assembly	8	08h
5	# Module Banks on this assembly	2	02h
6	Data Width of this assembly	64 bits	40h
7	Data Width of this assembly (continued)		00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM cycle time at CL=3 (tCLK)	8ns	80h
		10ns	A0h
		12ns	C0h
		15ns	F0h
10	SDRAM Access from Clock at CL=3 (tAC)	7.5ns	75h
		8.5ns	85h
		8.5ns	85h
		9.0ns	90h
11	DIMM configuration type	Non-Parity	00h
12	Refresh Rate/Type	S/R, Normal 15.6 µs	80h
13	SDRAM Width Primary DRAM	x16	10h
14	ECC SDRAM Data Width	N/A	00h
15	Min. clock delay, Back to Back Random Column Addresses (ICCD)	1CLK	01h
16	Burst Length Supported	1, 2, 4, 8 & Full	8Fh
17	# Banks on each SDRAM device	2	02h
18	CAS# Latency	2, 3	06h
19	CS# Latency	0	01h
20	Write Latency	0	01h
21	SDRAM Module Attribute	Non-Buffered/Registered	00h
22	SDRAM Device Attribute	Vcc, B/R, S/W, P/A, A/P	0Eh
23	Min Clock cycle Time at CL=2 (tCLK)	12ns	C0h
		15ns	F0h
		17ns	20h
24	Max. Data Access Time from clock at CL=2 (tAC)	9.0ns	90h
		9.0ns	90h
		9.0ns	90h
		10.0ns	A0h
25	Min Clock cycle Time at CL=1 (tCLK)	N/A	00h
26	Max. Data Access Time from clock at CL=1 (tAC)	N/A	00h
27	Min. Row Precharge Time (tRP)	27ns	1Bh
		30ns	1Eh
		35ns	23h
		40ns	28h
28	Min. Row Active Delay (tRRD)	24ns	18h
		30ns	1Eh
		30ns	1Eh
		30ns	1Eh
29	Min. RAS to CAS Delay (tRCD)	24ns	18h
		30ns	1Eh
		30ns	1Eh
		30ns	1Eh
30	Min. RAS Pulse Width (tRAS)	48ns	30h
		60ns	3Ch
		65ns	41h
		70ns	46h
31	Module Bank Density	8MB	02h
32-61	Superset Information		00h
62	SPD Revision	Rev. 1	01h
63	Checksum for bytes 0-62		
64-127	Manufacturer's Information		
128+	Unused Storage Locations		

DC CHARACTERISTICS

(V_{CC} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70 °)

Parameter	Symbol	Test Condition	125		100		84		67		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	No Burst, t_{CK} = min. t_{RC} = min.	-	560	-	540	-	520	-	500	mA	1, 2
		No Burst, t_{CK} = min., t_{RC} = min. All Banks Active	-	760	-	720	-	680	-	640	mA	1, 2
Precharge Standby Current	I_{CC2}	CKE -V_{IL}, t_{CK} = min. All Banks Idle	-	16	-	16	-	16	-	16	mA	1, 2
		CKE = V_{IH}, t_{CK} = min. All Banks Idle	-	240	-	240	-	240	-	240	mA	1.2
Active Standby Current	I_{CC3}	CKE = V_{IL}, t_{CK} = min. Any Bank Active	-	240	-	240	-	240	-	240	mA	1, 2
		CKE = V_{IH}, t_{CK} = min. Any Bank Active	-	400	-	400	-	400	-	400	mA	1, 2
Burst Mode Current	I_{CC4}	t_{CK} = min.	-	800	-	740	-	700	-	660	mA	1, 2
Refresh Current	I_{CC5}	t_{CK} = min., t_{RC} = min., t_{RRD} = min. Auto Refresh	-	680	-	640	-	600	-	560	mA	1, 2
Self Refresh Current	I_{CC6}	CKE - V_{IL}	-	16	-	16	-	16	-	16	mA	1, 2
Input Leakage	I_{LI}	0V ≤ V_{in} ≤ V_{CC}	-80	80	-80	80	-80	80	-80	80	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ V_{CC} D_{out} = Disable	-10	10	-10	10	-10	10	-10	10	µA	
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	2.4	-	2.4	-	2.4	-	V	
Output Low Voltage	V_{OL}	Low I_{out} = 2 mA	-	0.4	-	0.4	-	0.4	-	0.4	V	

†CL = CAS* Latency

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max.) is specified at the output open condition.

2. An initial pulse of 200µs is required after power-up followed by a minimum of eight Auto-Refresh-Cycles.

CAPACITANCE

(TA =+25°C, VCC = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, WE*, RAS*, CAS*)	C_{I1}	37	pF	1
Input Capacitance (DQMBs)	C_{I2}	13	pF	1
Input Capacitance (CS0*, CS1*)	C_{I3}	21	pF	1
Input Capacitance (CLK0, CLK1, CKE0, CKE1)	C_{I4}	21	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	12	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.

2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTICS

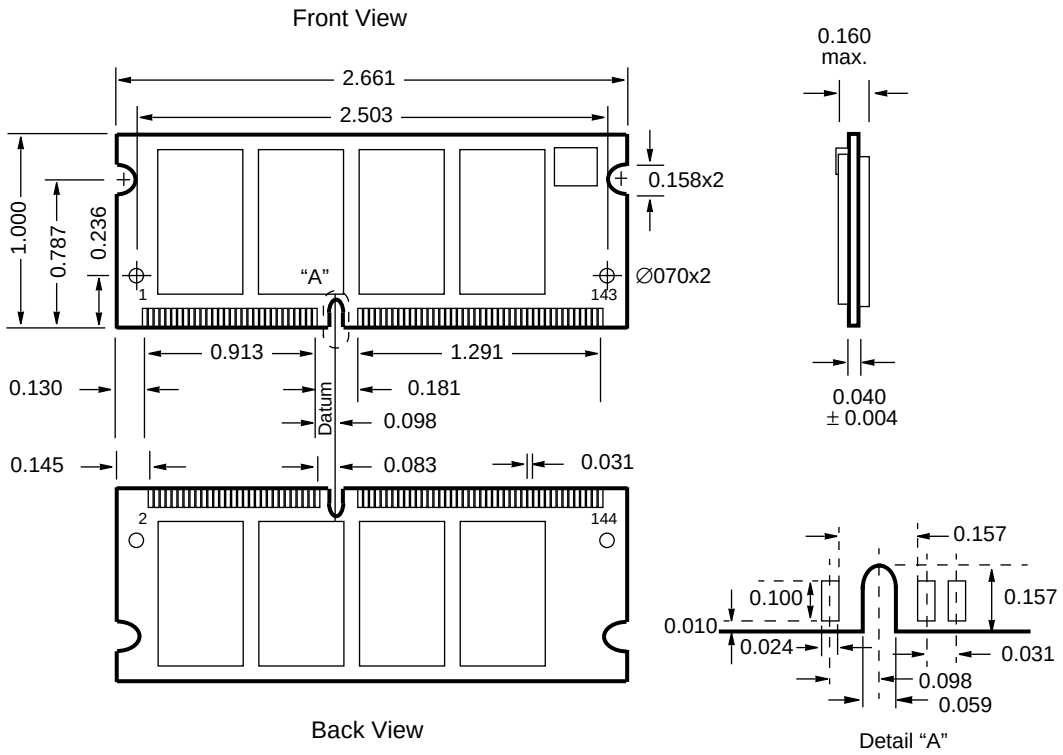
(TA = 0 to +70°C, V_{CC} = 3.3V±0.3V, V_{SS} = 0V)

Parameter		Symbol	Unit	125		100		84		67		Notes
Clock Period	CL=3	t_{CLK}	ns	8	-	10	-	12	-	15	-	1, 2, 3, 6
	CL=2			12	-	15	-	17	-	20	-	
Transition Time		t_T	ns	0.5	2	0.5	2	0.5	2	0.5	2	1, 2, 3
Clock High Time		t_{CH}	ns	3.5	-	4	-	4	-	4	-	1, 2, 3
Clock Low Time		t_{CL}	ns	3.5	-	4	-	4	-	4	-	1, 2, 3
CS Setup Time		t_{SC}	ns	3.0	-	3.0	-	3.0	-	3.0	-	1, 2, 3
CS Hold Time		t_{HC}	ns	1.0	-	1.0	-	1.0	-	1.0	-	1, 2, 3
Input Setup Time		t_{SI}	ns	3.0	-	3.0	-	3.0	-	3.0	-	1, 2, 3
Input Hold Time		t_{HI}	ns	1.0	-	1.0	-	1.0	-	1.0	-	1, 2, 3
Output Valid from Clock	CL=3	t_{AC}	ns	-	7.5	-	8.5	-	8.5	-	9.0	1, 2, 3
	CL=2			-	9	-	9	-	9	-	10	
Output In Low-Z		t_{OLZ}	ns	2	-	3	-	3	-	3	-	1, 2, 3
Output in High-Z		t_{OHZ}	ns	2	-	3	-	3	-	3	-	1, 2, 3, 4
Output Hold Time		t_{OH}	ns	2	-	3	-	3	-	3	-	1, 2, 3
Time between Refresh		t_{REF}	ms	-	32.8	-	32.8	-	32.8	-	32.8	1, 2, 3
RAS Cycle Time		t_{RC}	ns	75	-	90	-	100	-	110	2	1, 2, 3, 5
RAS Access Time		t_{RAC}	ns	-	45	-	54	-	56	-	60	1, 2, 3
CAS Access Time		t_{CAC}	ns	-	21	-	24	-	26	-	30	1, 2, 3
RAS Precharge Time		t_{RP}	ns	27	-	30	-	35	-	40	-	1, 2, 3
RAS Active Time		t_{RAS}	ns	48	10000	60	10000	65	-	70	10000	1, 2, 3
RAS to CAS Delay Time		t_{RCD}	ns	24	-	30	-	30	-	30	-	1, 2, 3
Write Recovery Time		t_{WR}	ns	8	-	10	-	12	-	15	-	1, 2, 3
Write to Precharge Lead Time		t_{RWL}	ns	8	-	10	-	12	-	15	-	1, 2, 3
RAS to RAS Delay Time		t_{RRD}	ns	24	-	30	-	30	-	30	-	1, 2, 3
Power-down Exit Time		t_{PDE}	ns	3	-	3	-	4	-	5	-	1, 2, 3
CKE to Clock Disable		l_{CKE}	cycle	1		1		1		1		
DQM to Output in High-Z		l_{DQZ}	cycle	2		2		2		2		
DQM to Input Data Delay		l_{DQD}	cycle	0		0		0		0		
Last Output to Write Command Delay		l_{OWD}	cycle	2		2		2		2		
Write Command to Input Data Delay		l_{DWD}	cycle	0		0		0		0		
Precharge to Output in High-Z Delay	CL=3	l_{ROH}	cycle	3		3		3		3		
	CL=2			2		2		2		2		
Mode Register Access to Bank Active (min.)		l_{MRD}	cycle	2		2		2		2		
CAS to CAS Delay		l_{CCD}	cycle	1		1		1		1		
CAS Bank Delay		l_{CBD}	cycle	1		1		1		1		

Notes:
1. An initial pulse of at least 200µs is required after power-up followed by a minimum of eight auto refresh cycles.
2. AC characteristics assume t_T = 1ns and 50pF capacitive load. If t_T is longer than 1ms, reference level for measuring time of input signal is V_{IH} (min.) and V_{IL} (max.).
3. 1.4V is the reference level for measuring timing of input signals.
4. t_{HZ} and t_{OH} defines the time at which the outputs achieve ±200mV.
5. Actual clock output of t_{RC} will be sum clock of t_{RAS} and t_{RP}.
6. 20ns is not supported in SPD.

Physical Dimensions

144-pin (72x2) DIMM



(All dimensions are in inches with 0.005" tolerance unless otherwise specified)

Notes: 1. All dimensions are in inches.

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